M61047FP

Battery Protection Analog Front End (AFE) IC

REJ03F0005-0200
Rev.2.00
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Description

The M61047FP is intended to be used as SB: Smart Battery. All functions needed for SB are packed to this M61047FP. The combination use with microcomputer such as M37517 will give various functions such as a detection of SB Remaining Capacity. The reset circuit and the linear regulator for Vcc/Vref of microcomputer are dedicated in M61047FP. So this will help easy design of power circuit design of SB.

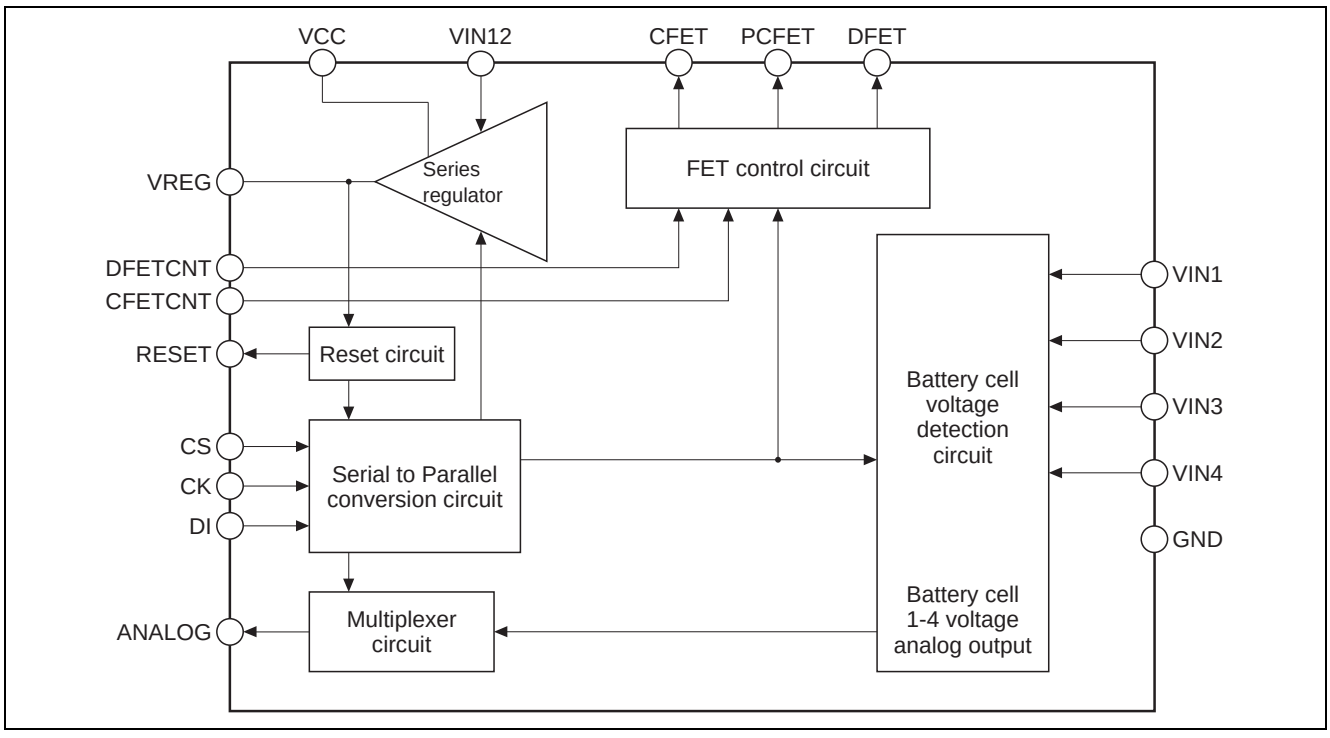
Features

- All FETs are controlled by microcomputer
- Built-in low dropout series regulator for microcomputer
- Built-in battery voltage monitor circuit of each battery cell
- Built-in output selector, which outputs the voltage each selected battery cell
- Built-in discharge circuit of each battery cell
- Built-in voltage detection circuit of each battery cell
- Built-in FET OFF function controlled by microcomputer
- Various powers saving function to reduce total power dissipation
- 3-wire serial data transfer system for communication from microcomputer
- High Input Voltage Device (Absolute Maximum Rating: 33 V)
- CMOS monolithic IC

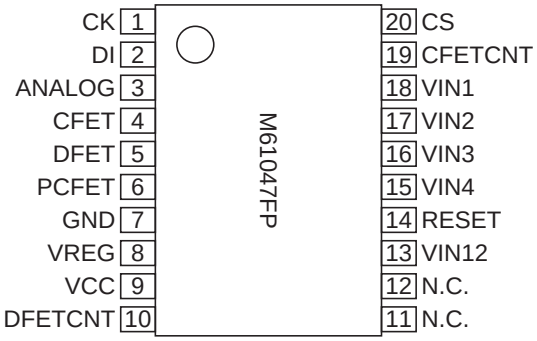
Application

- Smart Battery System

Block Diagram



Pin Arrangement



(Top view)

Package: PLSP0020JB-A (20P2F-A)

Pin Description

Pin No.	Pin Name	Function
9	VCC	Power source pin. Power from charger or battery
8	VREG	Linear-Regulator output for microcomputer
13	VIN12	Monitoring charger is connected or not
18	VIN1	Battery 1 + voltage input
17	VIN2	Battery 1 – voltage and Battery 2 + voltage input
16	VIN3	Battery 2 – voltage and Battery 3 + voltage input
15	VIN4	Battery 3 – voltage and Battery 4 + voltage input
7	GND	Ground and Battery 4 - voltage input
5	DFET	Discharge FET-Drive Output. The Driver is turned off by Microcomputer
4	CFET	Charge FET-Drive Output. The Driver is turned off by Microcomputer
6	PCFET	Pre-charge FET-Drive Output. The Driver is turned off by Microcomputer
14	RESET	Reset signal output to RESET of Microcomputer
3	ANALOG	Various Analog signal outputs to AD-input of Microcomputer
19	CFETCNT	Input of CFET and PCFET control signal from Microcomputer
10	DFETCNT	Input of DFET control signal from Microcomputer
20	CS	During low signal input to this CS, data input to DI is enabled
1	CK	Input of shift clock from Microcomputer. DI's input data is latched by low-to-high edge of this CK
2	DI	Input of 6-bit length serial data from Microcomputer

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Condition
Absolute maximum rating	Vabs	33	V	
Supply voltage	Vcc	30	V	
Power dissipation	PD	800	mW	
Operating temperature range	Topr1	–20 to +85	°C	
Storage temperature range	Tstg	–40 to +125	°C	

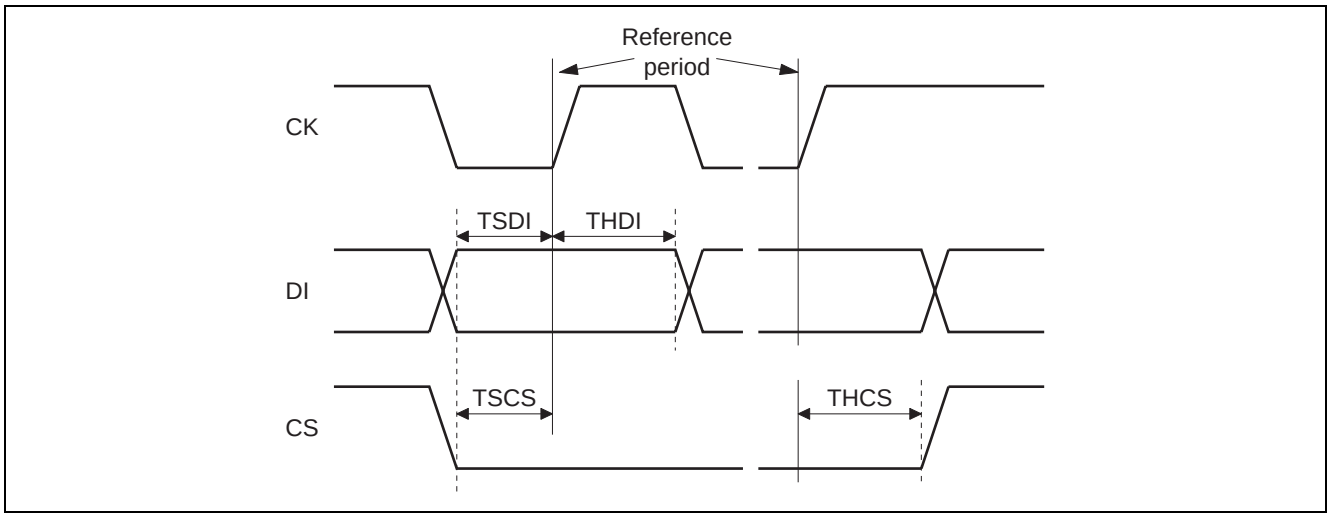


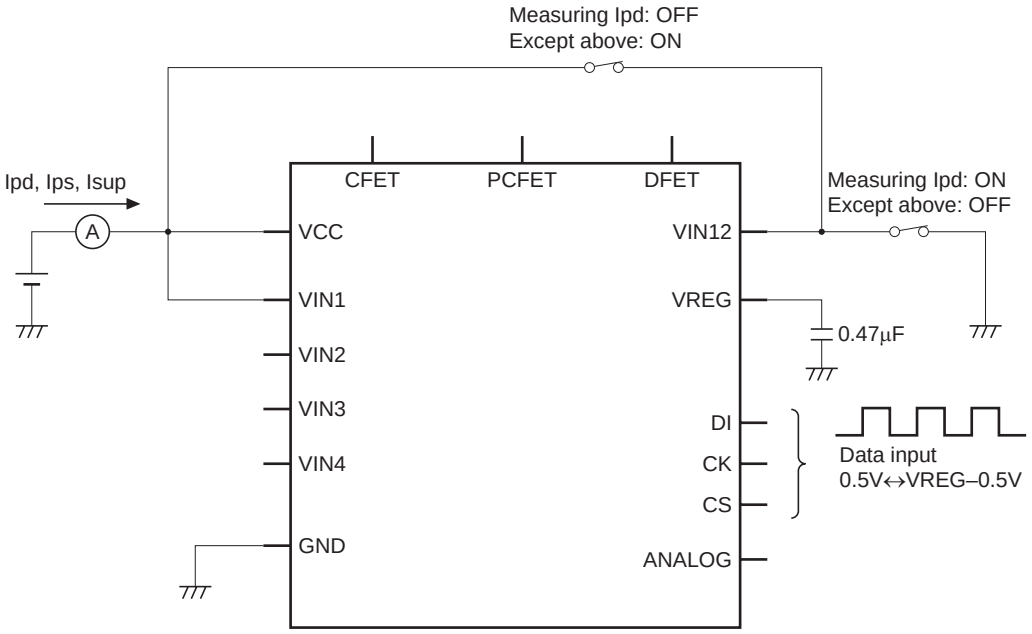
Figure 1 Interface Timing

Electrical Characteristics

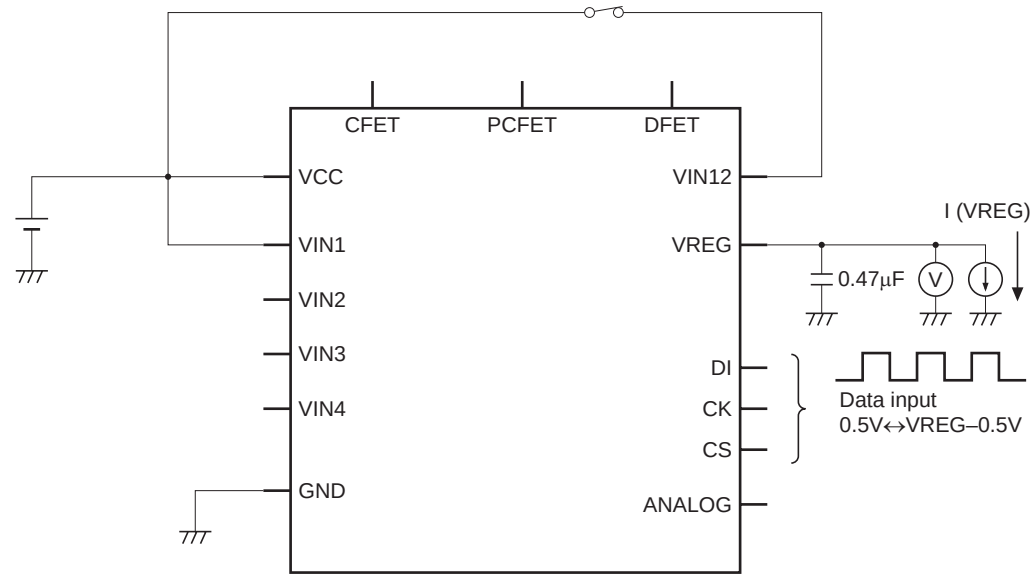
(Ta = 25°C, Vcc = 14 V, unless otherwise noted)

Block	Item	Symbol	Min.	Typ.	Max.	Unit	Circuit	Condition
Total	Supply voltage	Vsup	—	—	30	V	1	
	Supply current 1	Isup	35	75	115	µA	1	
	Supply current 2	Ips	20	45	70	µA	1	Power save mode (Battery voltage detection: OFF)
	Supply current 3	Ipd	—	—	0.5	µA	1	Power down mode
Regulator	Output voltage	Vreg	3.276	3.3	3.333	V	2	VCC = 14V, Iout = 10mA
			4.75	5.0	5.25	V	2	VCC = 14V, Iout = 10mA
	Linear regulation	ΔVline	—	2	10	mV	2	VREG = 3.3V VCC = 6.0V to 24V, Iout = 10mA
			—	4	100	mV	2	VREG = 5.0V VCC = 7.5V to 24V, Iout = 10mA
	Load regulation	ΔVload	—	3	15	mV	2	VREG = 3.3V VCC = 6.0V, Iout = 50µA to 10mA
			—	5	150	mV	2	VREG = 5.0V VCC = 7.5V, Iout = 50µA to 50mA
Reset	Detection voltage	Vdet–	2.6	2.75	2.9	V	3	VREG = 3.3V
	Release voltage	Vdet+	2.9	2.975	3.05	V	3	VREG = 3.3V
Battery voltage detection	Input offset voltage	Voff	31	206	385	mV	4	
	Voltage gain	Gamp	0.594	0.600	0.606	—	4	VREG = 3.3V
	Output source current	Isource	75	—	—	µA	5	
	Output sink current	Isink	150	—	—	µA	5	
	Detection voltage of battery cell	Vmo_max	4.7	—	—	V	2, 4	(Vreg–Voff1)/Gamp
Interface	DI input H voltage	VDIH	Vreg–0.5	—	Vreg	V	6	
	DI input L voltage	VDIL	0	—	0.5	V	6	
	CS input H voltage	VCSH	Vreg–0.5	—	Vreg	V	6	
	CS input L voltage	VCSL	0	—	0.5	V	6	
	CK input H voltage	VCKH	Vreg–0.5	—	Vreg	V	6	
	CK input L voltage	VCKL	0	—	0.5	V	6	
	DI set-up time	TSDI	600	—	—	ns	6	
	DI hold time	THDI	600	—	—	ns	6	
	CS set-up time	TSCS	600	—	—	ns	6	
	CS hold time	THCS	600	—	—	ns	6	
	DFETCNT input H voltage	VDCH	Vreg–0.5	—	Vreg	V	6	
	DFETCNT input L voltage	VDCL	0	—	0.5	V	6	
	CFETCNT input H voltage	VCCH	Vreg–0.5	—	Vreg	V	6	
	CFETCNT input L voltage	VCCL	0	—	0.5	V	6	
	CFETCNT sink current	ICCH	0.3	1	2	µA	6	CFETCNT = 3.3V
Conditio-ning circuit	VIN1 resistor	RON1	250	500	1000	Ω	7	
	VIN2 resistor	RON2	250	500	1000	Ω	7	
	VIN3 resistor	RON3	250	500	1000	Ω	7	
	VIN4 resistor	RON4	250	500	1000	Ω	7	

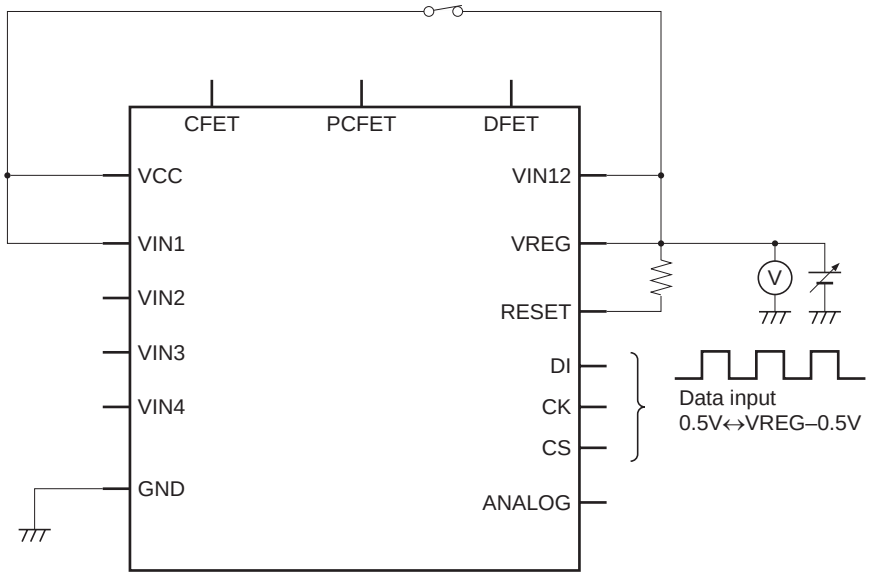
Measurement Circuit



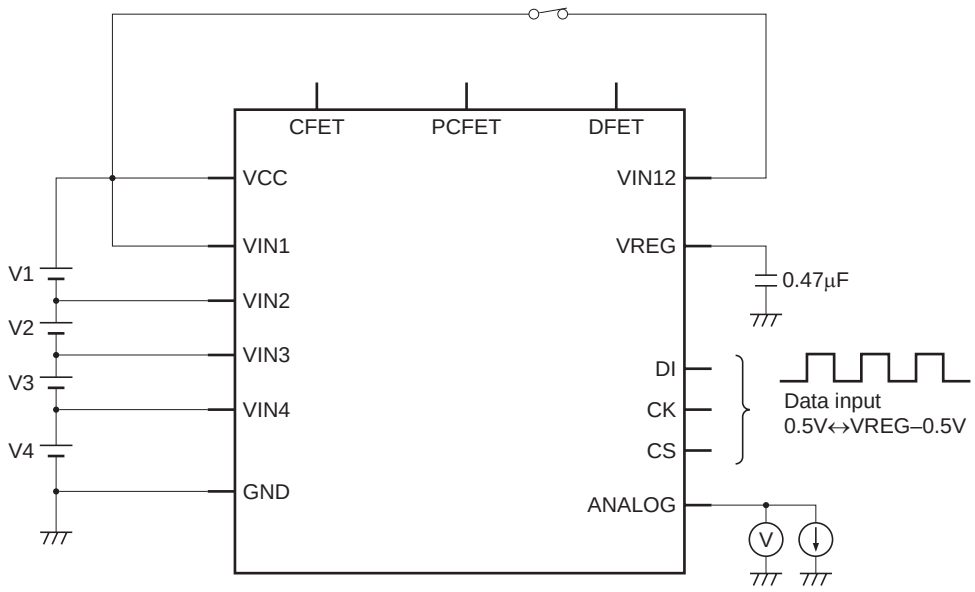
Measurement circuit 1



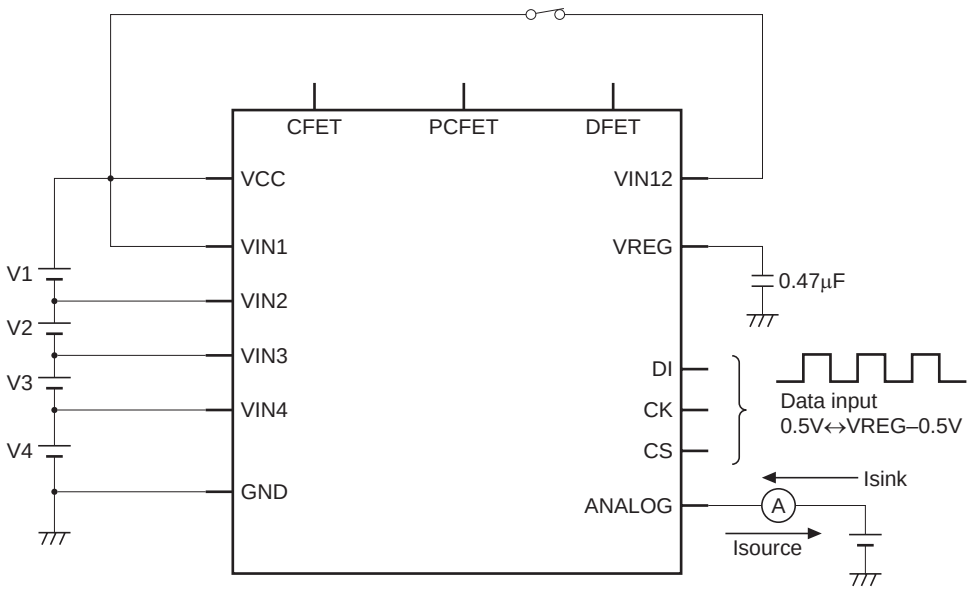
Measurement circuit 2



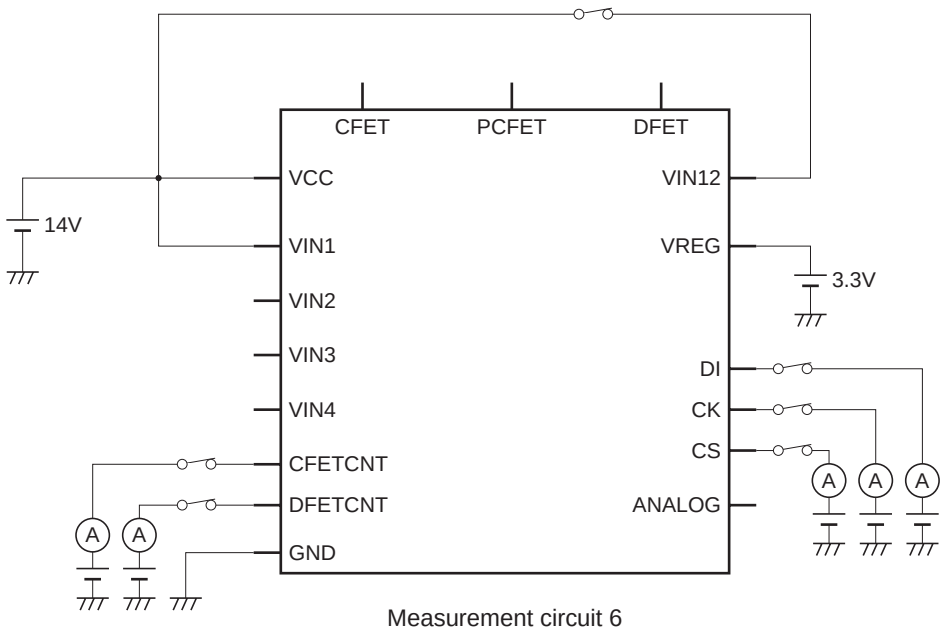
Measurement circuit 3



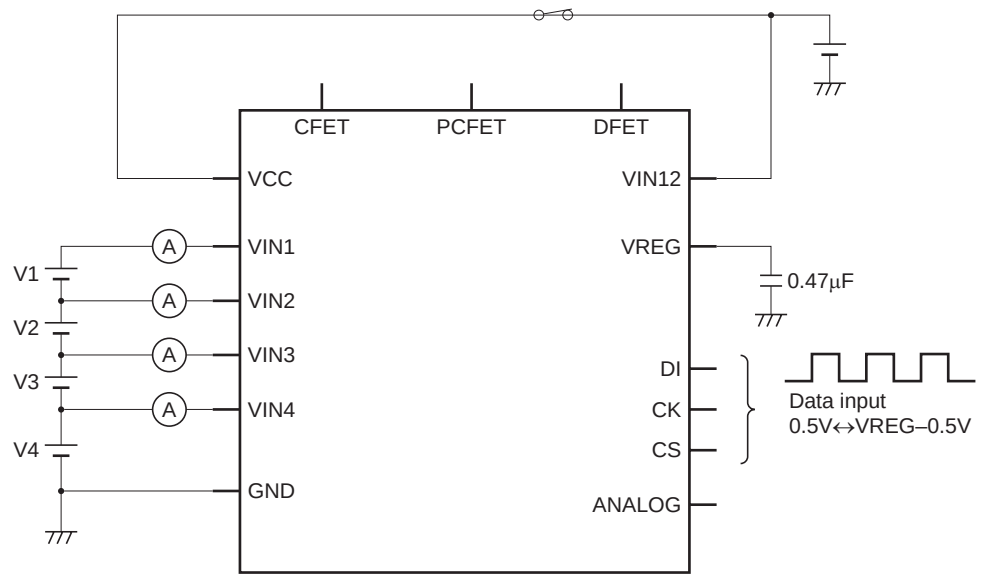
Measurement circuit 4



Measurement circuit 5



Measurement circuit 6



Measurement circuit 7

Operation Description

M61047FP is developed for intelligent Li-ion battery pack such as SB in SBS. M61047FP is suitable for Smart Battery.

Pair using with Microcomputer such as M37517 and small additional parts will give various functions such as battery remaining capacity detection. All functions are described as follows.

Note: SBS: Smart Battery System introduced by Intel and Duracell
SB: Smart Battery, which contains 3 or 4 series Li-ion battery cells.

Voltage Detection Circuit of Each Li-ion Battery Cell

M61047FP can output each battery cell's voltage of 3 or 4 series connection. Built-in buffer amplifier is monitoring each battery voltage.

Series Regulator

M61047FP contains low drop out series regulator. Microcomputer in SB does not need any additional voltage regulator.

Usually, although series regulator is 3.3 V output, it is possible to change to 5 V output by register setup at the time of flash memory rewriting of microcomputer.

Reset Circuit

Vreg output voltage is checked by Reset circuit of M61047FP. Therefore, lower voltage of Vreg issues RESET signal to stop mull-function of microcomputer. Also, lower voltage after long time's left issues RESET signal to stop mull-function of microcomputer. This function is useful for safety of long time's left battery.

When charger is connected to SB, this circuit will check Vreg voltage, so if Vreg voltage is NOT enough high, this circuit remains low as for RESET signal to microcomputer.

Conditioning Circuit

M61047FP have a discharge circuit of each cells. It is available for drop of cell voltage for safety purpose. And to shorten the difference voltage among the cells. It can extend the battery pack life.

Power Save Function

M61047FP contains power save function to control several supply current. It can operate in the three state, usual mode, power save mode, and power down mode. These three modes can be changed by the command from a microcomputer, and can control the consumption current in each mode.

1. Usual mode
   It is in the state where all circuits are operating.
2. Power save mode
   In power save mode, consumption current is reduced by stopping voltage detection circuit, and outputting ALALOG output with GND level. If ANALOG output is changed to the battery voltage output or offset voltage output of each cell by the command from a microcomputer, it will change to usual mode. In addition, the regulator circuit is operating in a power save mode.
3. Power down mode
   In power down mode, all circuits will be stopped.

The shift to power down mode and operation at the time of resume from power down mode are explained below using Figure 2.

- Enter Power Down Mode
  Microcomputer issues power down command to M61047FP after microcomputer detects that battery voltage is too low. After this command, the DFET pin is set to 'high' and the VIN12 pin is pulled down by internal resistor to be set 'low' and series regulator are turned off.
  In the power down mode, the M61047FP operation is impossible. And CFET, DFET and PCFET are set to 'high'. (In this situation, discharging is forbidden.) At this time, supply current becomes max. 0.5 µA, so drops of battery voltage is prevented.
- Resume from Power Down Mode
  After entering Power Down mode, the series regulator will begin operation when charger is connected (VIN12 pin is high). The RESET will output low to high signal when Vreg is over reset level voltage. Microcomputer will begin operation and send command to resume M61047FP from power down mode.

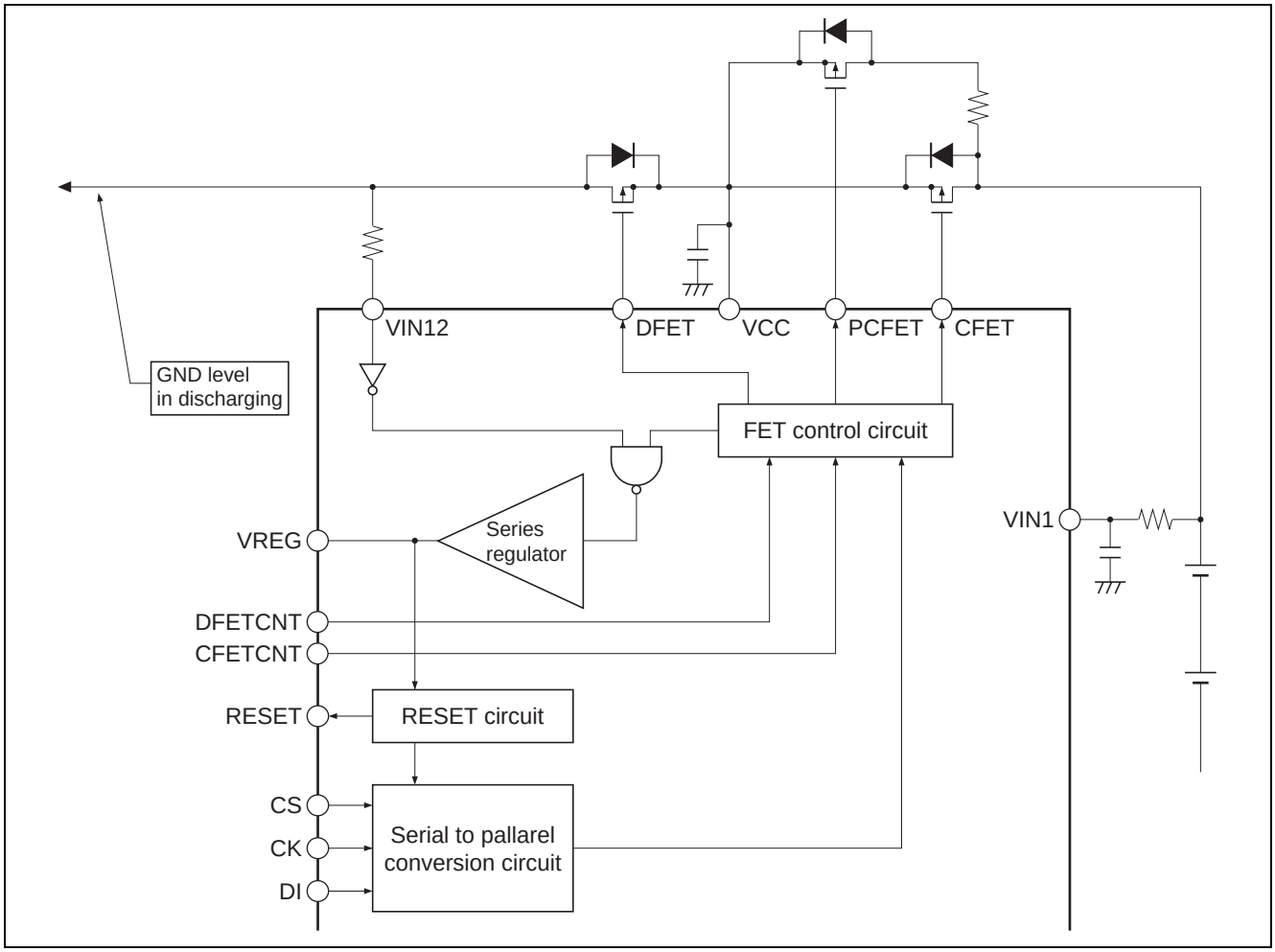


Figure 2 Function After Detecting Over-Discharge

Block Diagram Description

Battery Voltage Detection Circuit

The M61047FP battery voltage detection circuit is shown in Figure 3. This circuit is composed of switch, buffer amplifier, reference voltage section and logic circuit.

Microcomputer selects detecting voltage before logic circuit controls the connection of switches. This connection decides which cell voltage (Vbat1, Vbat2, Vbat3, Vbat4) should be output from Analog out pin. Besides offset voltage can be output.

In Power Down mode, supply current in this block is close to zero because all switches are off.

Note: Regard 100 µs as the standard of settling time by voltage change in this block.

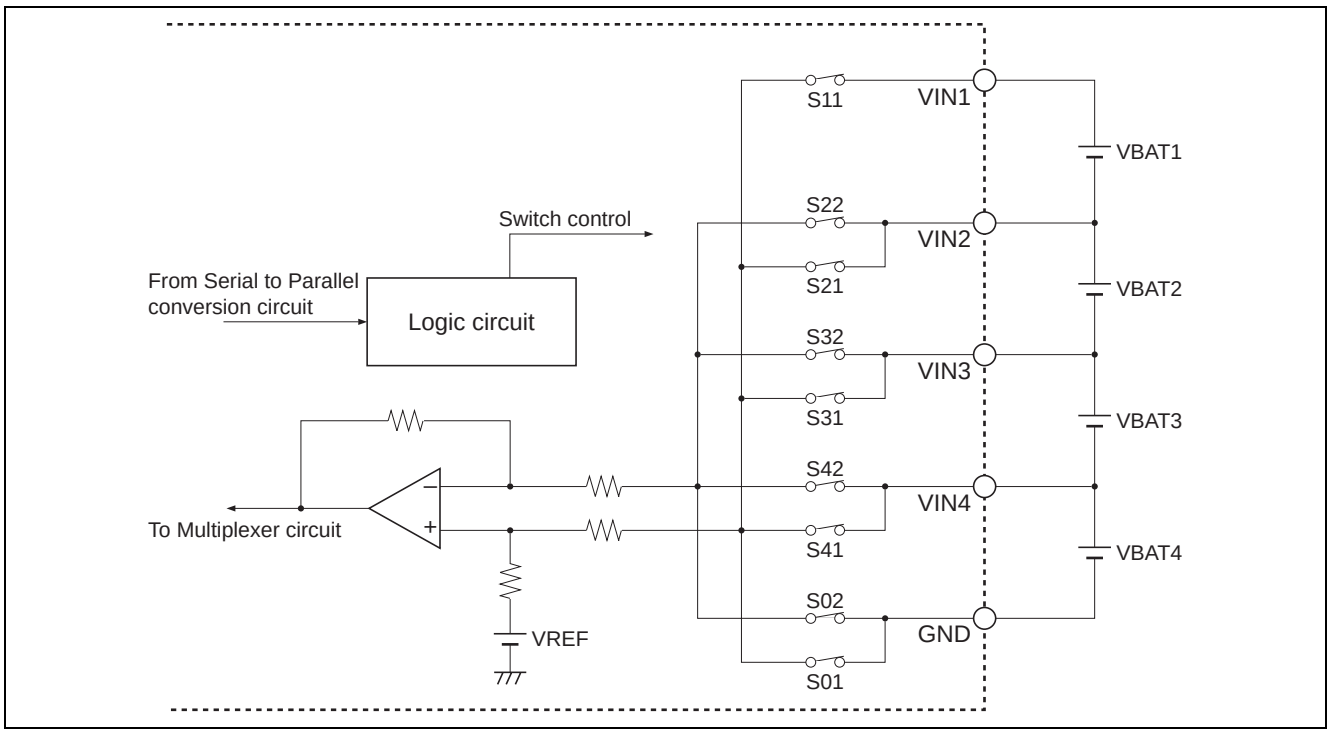


Figure 3 Battery Voltage Detection Circuit

Table 1 Turned on Switches

Function	Turn on Switch (refer to Figure 3)
VBAT1_OUTPUT	S11, S22
VBAT2_OUTPUT	S21, S32
VBAT3_OUTPUT	S31, S42
VBAT4_OUTPUT	S41, S02
VBAT1_OFFSET	S21, S22
VBAT2_OFFSET	S31, S32
VBAT3_OFFSET	S41, S42
VBAT4_OFFSET	S01, S02

Analog Output Selector

Analog output selector block is shown in Figure 4. The command from microcomputer determines whether GND is outputted to an analog terminal, or the voltage chosen in the battery voltage detection circuit is outputted.

At the time of GND output, since the battery voltage detection circuit stops, M61047FP goes into power save mode.

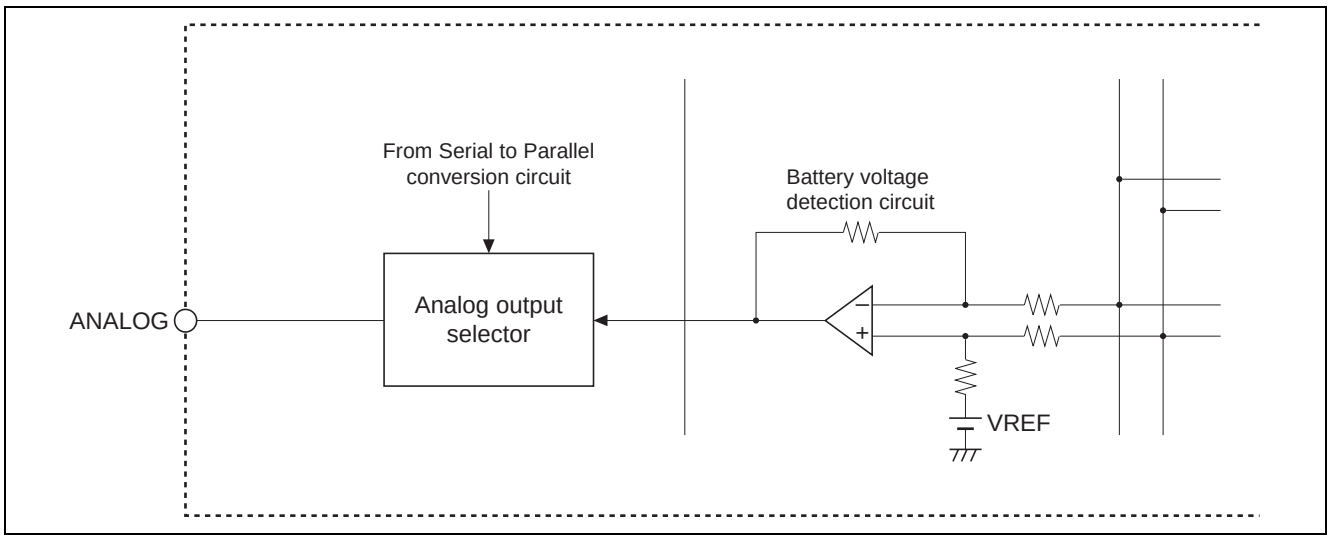


Figure 4 Analog Output Selector

Series Regulator

Series regulator is shown in Figure 5. Pch MOS transistor is used for output driver.

The output voltage can be adjusted by M61047FP itself. So the external resistor is not required.

Usually, although series regulator is 3.3 V output, it is possible to change to 5 V output by register setup at the time of flash memory rewriting of microcomputer.

Note: There is a diode put between Vcc and Vreg terminal to prevent the invert current from damaging this IC when Vcc Voltage is higher than Vreg voltage. So please always keep Vreg voltage lower than Vcc+0.3 V. Set a condenser on output to suppress input changes or load changes.
In order to suppress input change and load change, please attach a 0.47 µF capacitor to VREG output. Regard 10 ms as the standard of settling time by input change/load change/output change.

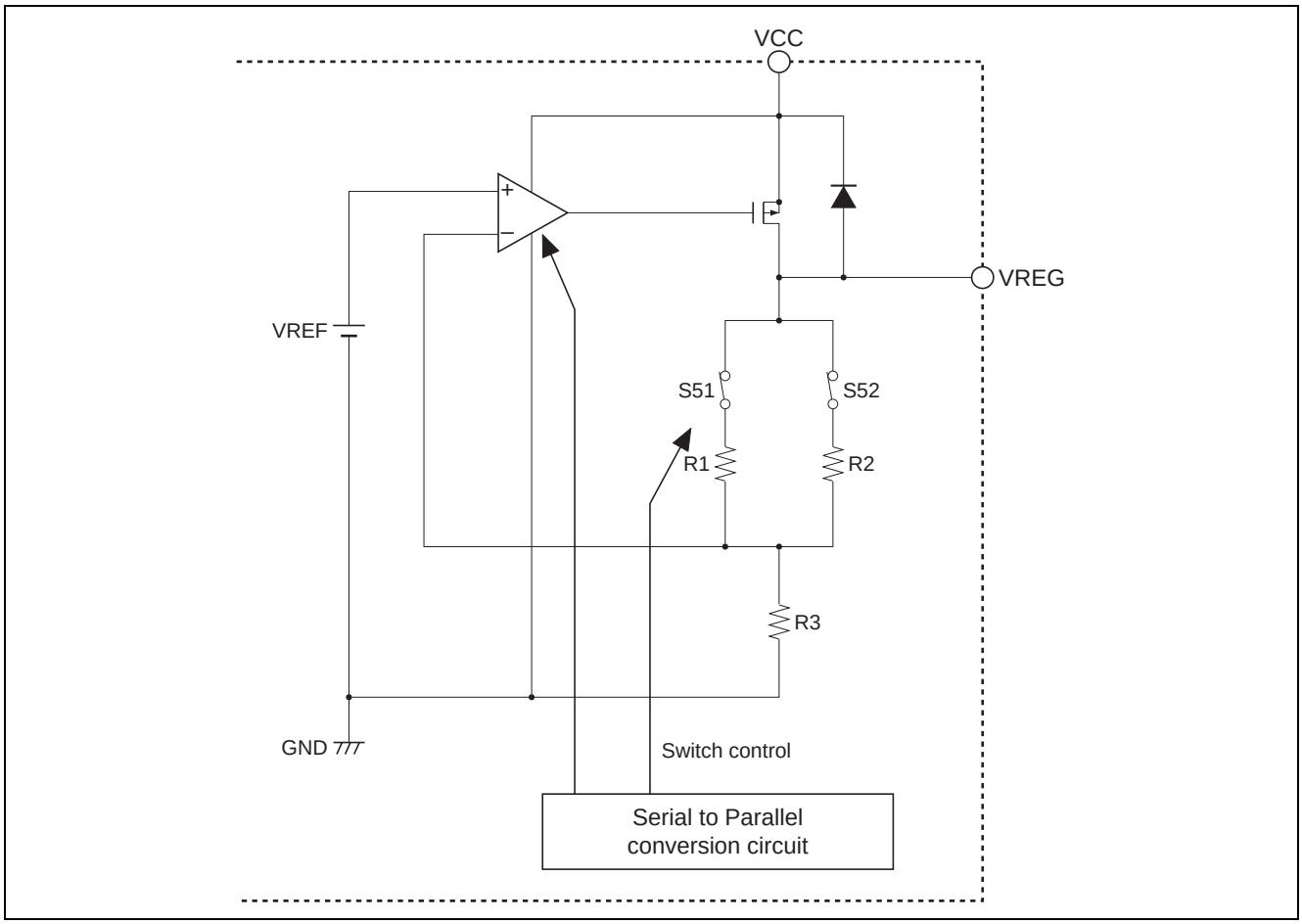


Figure 5 Series Regulator

Reset Circuit

The M61047FP reset circuit is shown in Figure 6. This circuit is composed of comparator, reference voltage section and breeder resistor. Hysterics is given to detection voltage and release voltage.

The reset output is Nch open drain structure so the reset delay time depends on external CR value.

The reset circuit monitoring Vreg output to prevent microcomputer abnormal operation when Vcc voltage goes down abnormally.

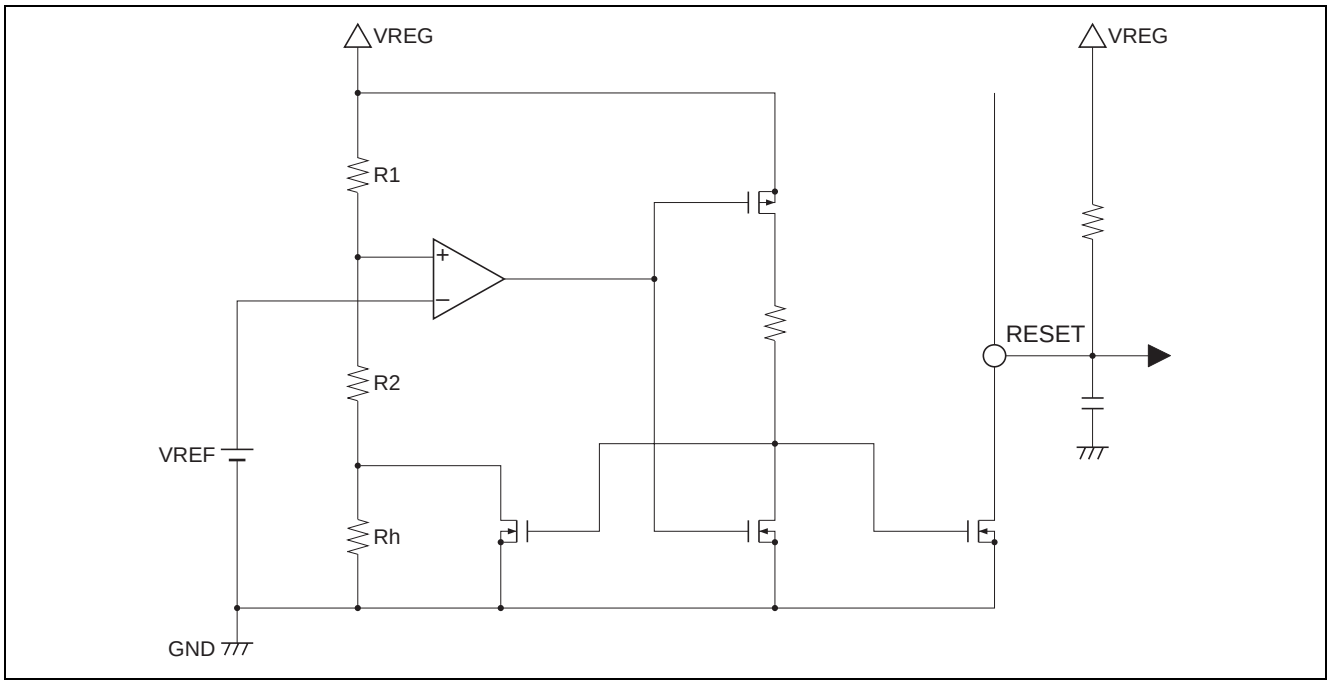


Figure 6 Reset Circuit

Conditioning Circuit

The M61047FP conditioning circuit is shown in Figure 7. This circuit is composed of switch, resistor and logic circuit.

According to the serial data from microcomputer, the logic circuit can individually control the switches (S61, S62 … etc.) to do individual cell discharge.

Moreover, it is possible to also make from 1 cell to 4 cells discharge similarly by sending serial data two or more times.

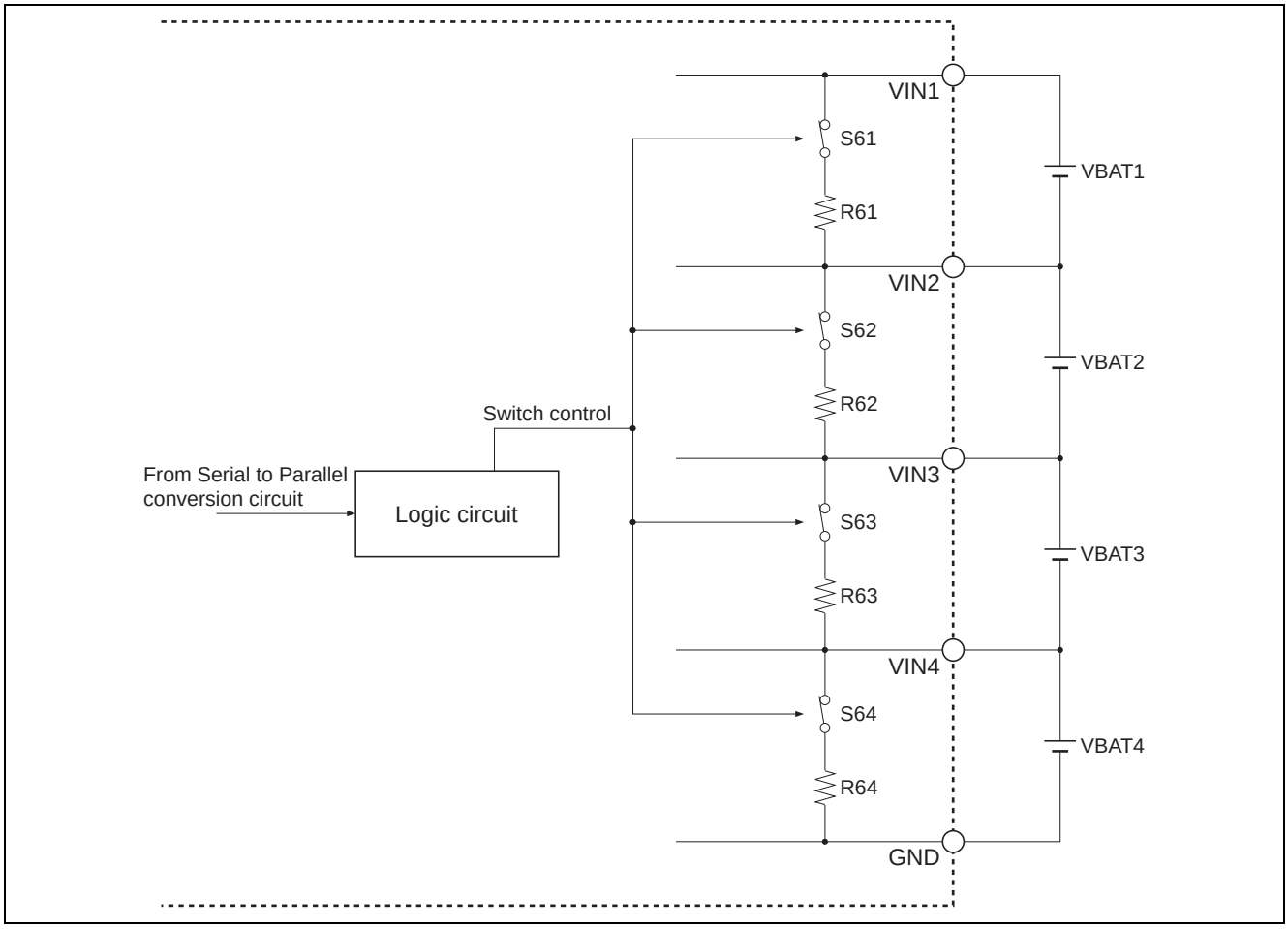


Figure 7 Conditioning Circuit

Resister Map

Address

Table 2

Establishment Data	Address			Data			Contents
	D5	D4	D3	D2	D1	D0	
Reset	0	0	0	—	—	—	—
Battery voltage output	0	0	1	—	—	—	Refer to table 3
FET control	0	1	0	—	—	—	Refer to table 4
Multiplexer select	0	1	1	—	—	—	Refer to table 5
Regulator	1	0	0	—	—	—	Refer to table 6
Conditioning circuit	1	0	1	—	—	—	Refer to table 7
Don't care	1	1	0	—	—	—	—
Don't care	1	1	1	—	—	—	—

Data

Table 3 Battery Voltage Output

D2	D1	D0	Name	Function
0	0	0	VBAT1_OUTPUT	BAT1 voltage monitor
0	0	1	VBAT2_OUTPUT	BAT2 voltage monitor
0	1	0	VBAT3_OUTPUT	BAT3 voltage monitor
0	1	1	VBAT4_OUTPUT	BAT4 voltage monitor
1	0	0	VBAT1_OFFSET	Offset voltage output at BAT1 monitor
1	0	1	VBAT2_OFFSET	Offset voltage output at BAT2 monitor
1	1	0	VBAT3_OFFSET	Offset voltage output at BAT3 monitor
1	1	1	VBAT4_OFFSET	Offset voltage output at BAT4 monitor

Note: Analog terminal output GND level when system reset.
(All switches for battery voltage detect circuit are turned off.) Regard 100µs as the standard of settling time by each change of ANALOG output.

Table 4 FET Control

D2	D1	D0	Name	Function		
				CFET	DFET	PCFET
0	0	0	FCNT_AH	High	High	High
0	0	1	FCNT_PL	High	High	Low
0	1	0	FCNT_DL	High	Low	High
0	1	1	FCNT_CH	High	Low	Low
1	0	0	FCNT_CL	Low	High	High
1	0	1	FCNT_DH	Low	High	Low
1	1	0	FCNT_PH	Low	Low	High
1	1	1	FCNT_AL	Low	Low	Low

Note: CFET, DFET and PCFET terminal are high when system reset.

Table 5 Multiplexer Control (Analog Output Control)

D2	D1	D0	Name	Function	Notes
0	0	0	MP_GND1	GND output	BAT1 voltage monitor
0	0	1	MP_RUN	Battery voltage output select	
0	1	0	MP_GND2	GND output	All switches for battery voltage detect are OFF.
0	1	1	MP_GND3	GND output	BAT4 offset voltage
1	0	0	—	Don't care	
1	0	1	—	Don't care	
1	1	0	—	Don't care	
1	1	1	—	Don't care	

Note: Analog terminal output GND level when system reset.
Regard 100μs as the standard of settling time by each change of ANALOG output.

Table 6 Regulator

D2	D1	D0	Name	Function	Notes
0	0	0	VREG_33	VREG = 3.3 V	
0	0	1	VREG_OFF	VREG = 0 V (Regulator turned off)	Power Down Command
0	1	0	VREG_50	VREG = 5.0 V	
0	1	1	VREG_33	VREG = 3.3 V	
1	0	0	Don't care		
1	0	1	Don't care		
1	1	0	Don't care		
1	1	1	Don't care		

Note: The regulator output 3.3 V when system reset.
All functions of M61047FP are stopped. But if the charger is connected then M61047FP will not enter power down mode.
Regard 20 ms as the standard of settling time by change of VREG output.

Table 7 Conditioning Circuit

				Function			
D2	D1	D0	Name	BAT1_SW	BAT2_SW	BAT3_SW	BAT4_SW
0	0	0	CD_OFF	OFF	OFF	OFF	OFF
0	0	1	CD_RON11	ON	Don't care	Don't care	Don't care
0	1	0	CD_RON21	Don't care	ON	Don't care	Don't care
0	1	1	CD_RON31	Don't care	Don't care	ON	Don't care
1	0	0	CD_RON41	Don't care	Don't care	Don't care	ON
1	0	1	CD_RON12	ON	Don't care	Don't care	Don't care
1	1	0	CD_RON22	Don't care	ON	Don't care	Don't care
1	1	1	CD_RON32	Don't care	Don't care	ON	Don't care

Note: Conditioning circuit is floating when system reset.
By transmitting data two or more times, BAT1 to BAT4 arbitrary cells can be turned on simultaneously.

Digital Data Format

The block diagram of the serial to parallel conversion circuit of serial data transmission is shown in Figure 8, and a timing chart is shown in Figure 9, respectively. After setting CS terminal to Low, serial data is read into the inside of IC in an order from LSB (D0) synchronizing with the stand-up of CK terminal. If CS terminal is set to High when it inputs by 6 bits, the contents of a 6-bit shift register are latched to an internal latch circuit after serial to parallel conversion.

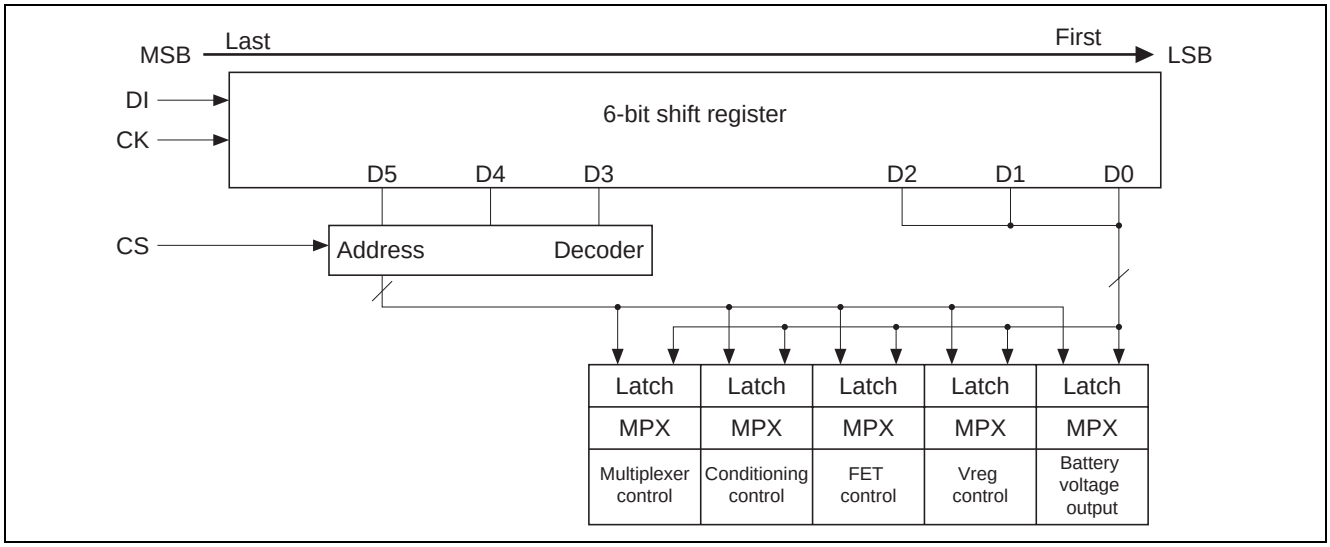


Figure 8 Serial to Parallel Conversion Circuit

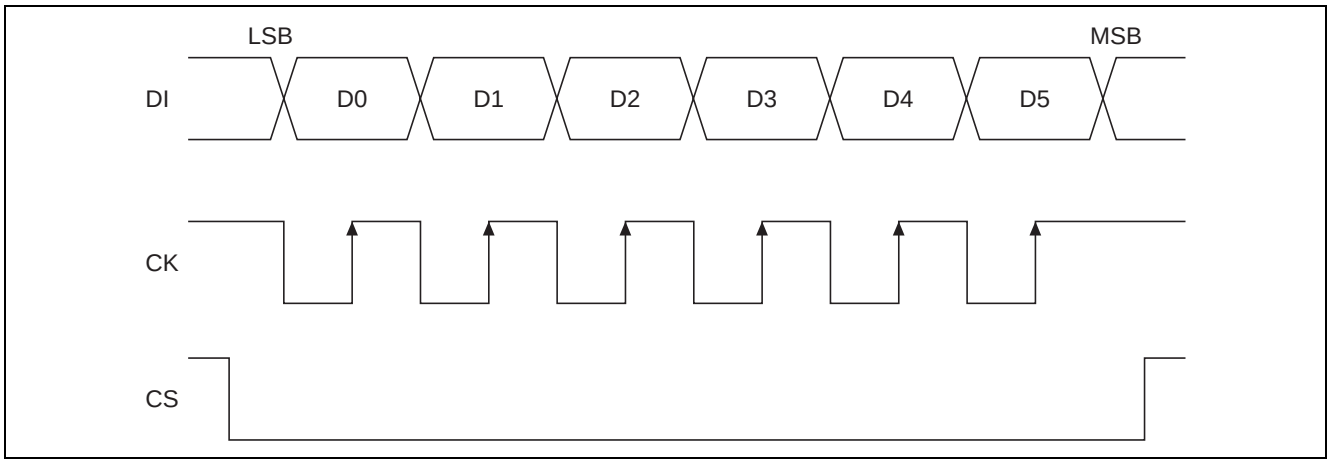


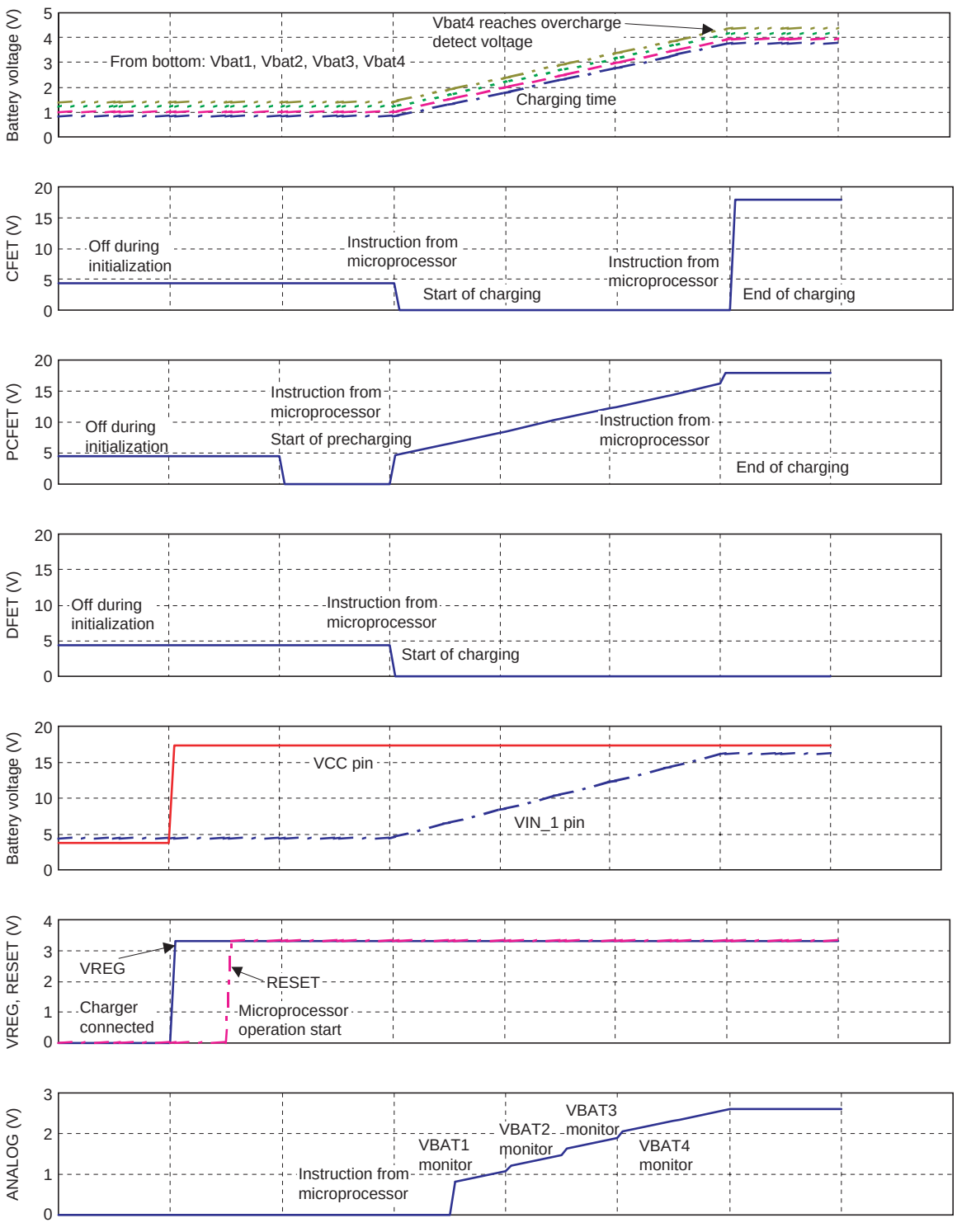
Figure 9 Timing Chart

Direct FET Control

It is possible to control direct FET by sending a signal to DFETCNT terminal or CFETCNT terminal other than serial data transmission from a microcomputer. If DFETCNT terminal is set to high, DFET terminal will be set to high, and if CFETCNT terminal is set to high, CFET terminal and PCFET terminal will be set to high. Priority is given to this function regardless of serial data communications.

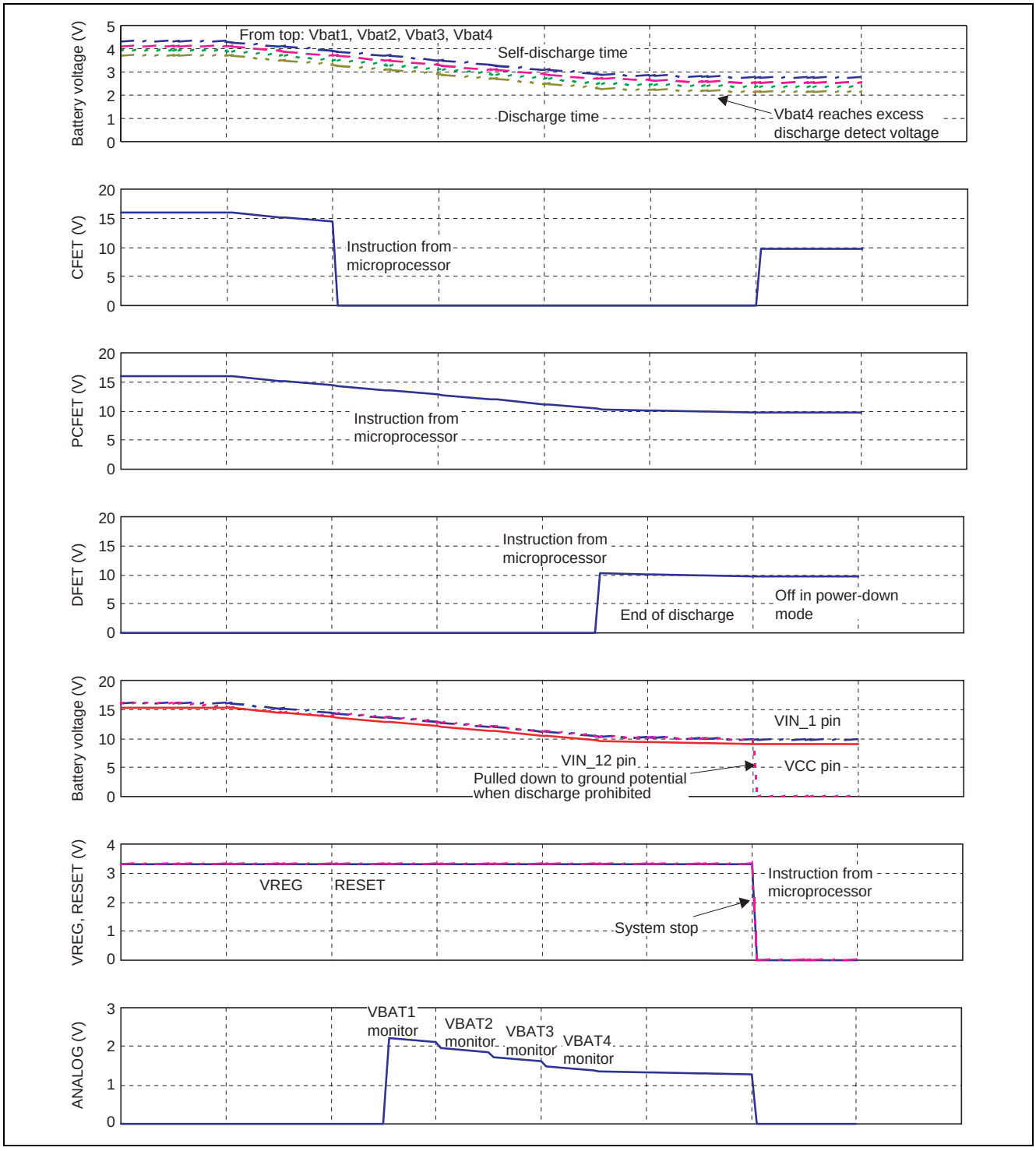
Timing Chart

Charging Sequence



Note: A constant voltage battery charger is used.

Discharge Sequence



Application Circuit

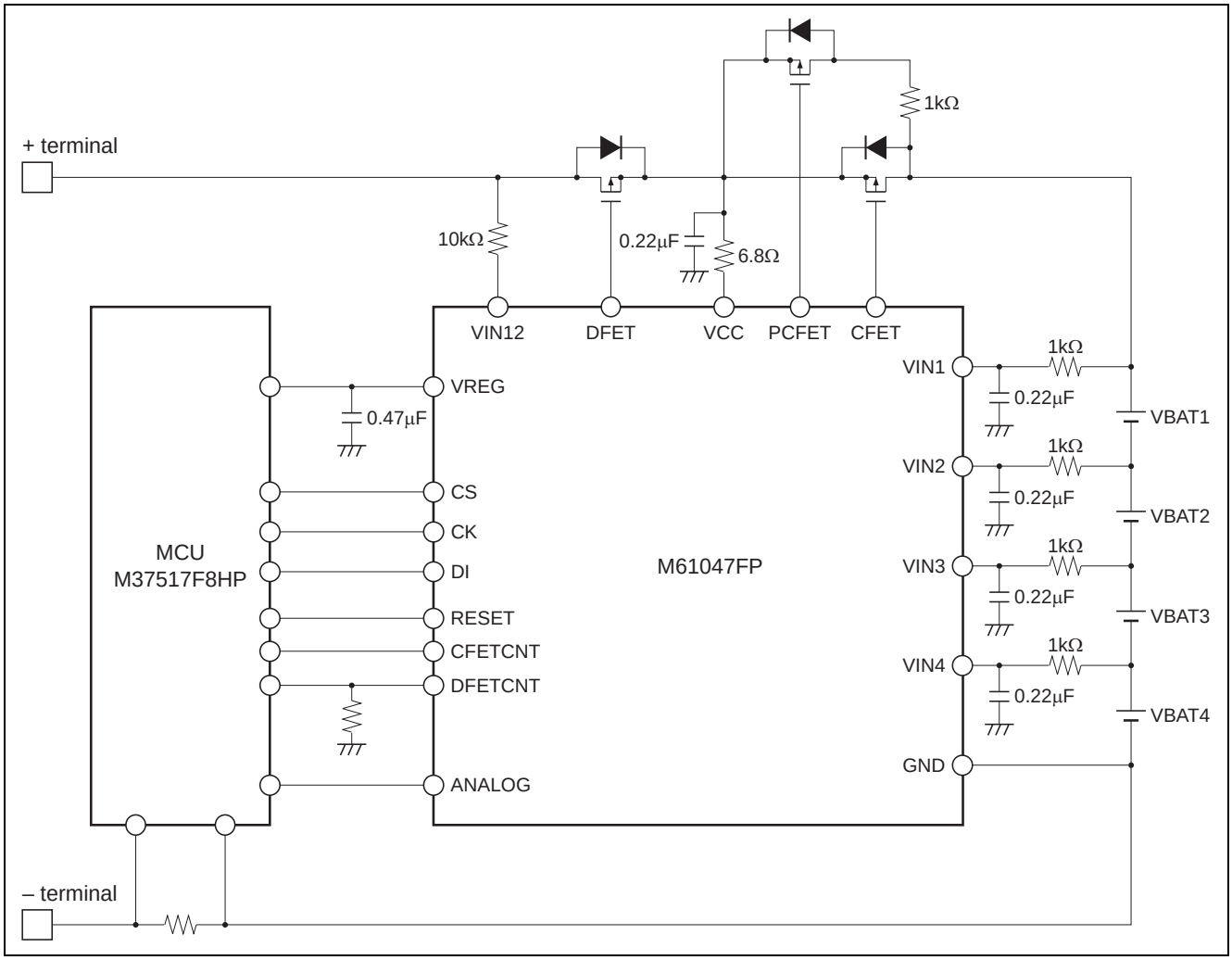


Figure 10 Application Circuit for 4 Cell Battery

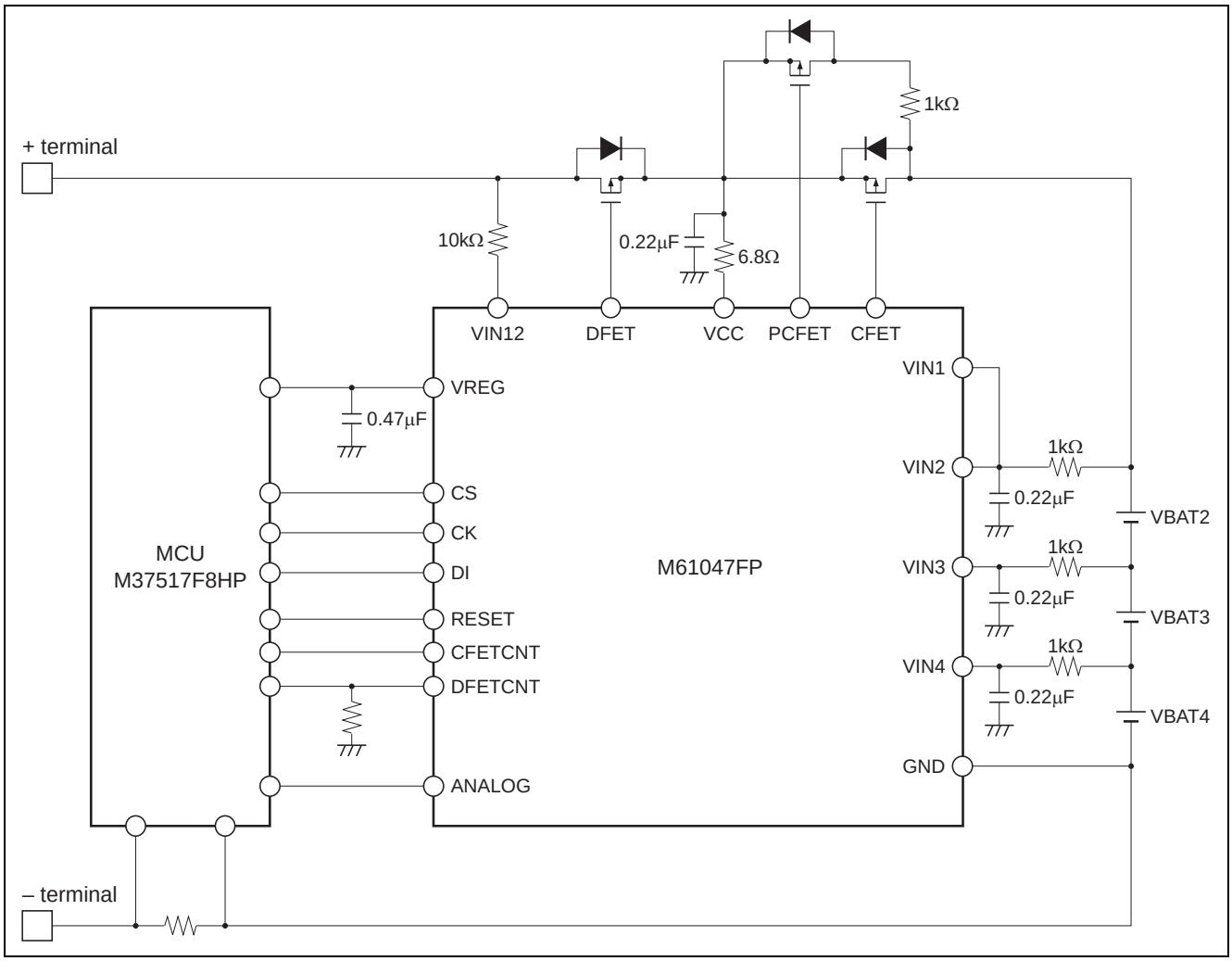
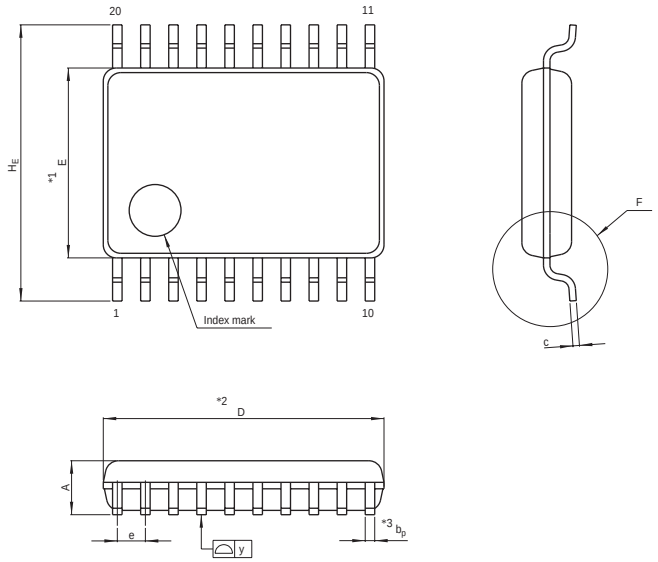


Figure 11 Application Circuit for 3 Cell Battery

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LSSOP20-4.4x6.5-0.65	PLSP0020JB-A	20P2F-A	0.1g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.4	6.5	6.6
E	4.3	4.4	4.5
A_2	——	1.15	——
A	——	——	1.45
A_1	0	0.1	0.2
b_p	0.17	0.22	0.32
c	0.13	0.15	0.2
θ	0°	——	10°
H_E	6.2	6.4	6.6
e	0.53	0.65	0.77
y	——	——	0.10
L	0.3	0.5	0.7

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http://www.renesas.com

Refer to "**http://www.renesas.com/en/network**" for the latest and detailed information.

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Colophon 2.0