

# DATA SHEET

**74ABT16373B**

16-bit transparent latch (3-State)

Product data

2004 Feb 27

Replaces 74ABT16373B/74ABTH16373B of 1998 Feb 27

## 16-bit transparent latch (3-State)

## 74ABT16373B

## FEATURES

- 16-bit transparent latch
- Multiple  $V_{CC}$  and GND pins minimize switching noise
- Power-up 3-State
- Live insertion/extraction permitted
- Power-up reset
- 3-State output buffers
- Output capability: +64 mA/-32 mA
- $I_{CCL}$  -19 mA maximum
- Latch-up protection exceeds 500 mA per JEDEC Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

## DESCRIPTION

The 74ABT16373B high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

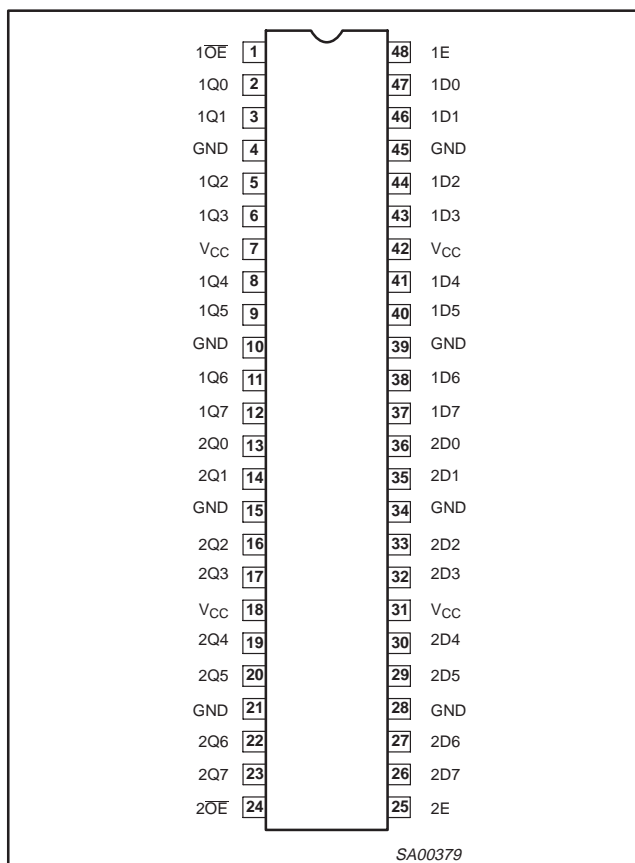
The 74ABT16373B device is a dual octal transparent latch coupled to two sets of eight 3-State output buffers. The two sections of the device are controlled independently by Enable (nE) and Output Enable (nOE) control gates.

The data on each set of D inputs are transferred to the latch outputs when the Latch Enable (nE) input is HIGH. The latch remains transparent to the data inputs while nE is HIGH, and stores the data that is present one set-up time before the HIGH-to-LOW enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. Each active-LOW Output Enable (nOE) controls eight 3-State buffers independent of the latch operation.

When nOE is LOW, the latched or transparent data appears at the outputs. When nOE is HIGH, the outputs are in the high-impedance "OFF" state, which means they will neither drive nor load the bus.

## PIN CONFIGURATION



## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25\text{ }^{\circ}\text{C}; \text{GND} = 0\text{ V}$	TYPICAL	UNIT
$t_{PLH}$ $t_{PHL}$	Propagation delay Dn to Qn	$C_L = 50\text{ pF}; V_{CC} = 5\text{ V}$	2.5 2.0	ns
$C_{IN}$	Input capacitance	$V_I = 0\text{ V or } V_{CC}$	4	pF
$C_{OUT}$	Output capacitance	$V_O = 0\text{ V or } V_{CC}; \text{3-State}$	7	pF
$I_{CCZ}$	Quiescent supply current	Outputs disabled; $V_{CC} = 5.5\text{ V}$	500	$\mu\text{A}$
$I_{CCL}$		Outputs low; $V_{CC} = 5.5\text{ V}$	8	mA

## ORDERING INFORMATION

$T_{amb} = -40\text{ }^{\circ}\text{C to } +85\text{ }^{\circ}\text{C}$

Type number	Package		Version
	Name	Description	
74ABT16373BDL	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm	SOT370-1
74ABT16373BDGG	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1

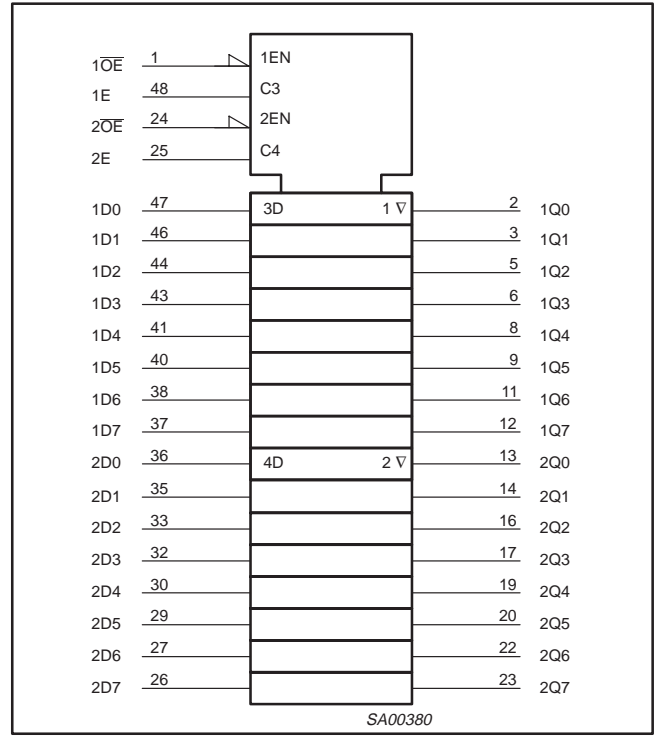
# 16-bit transparent latch (3-State)

## 74ABT16373B

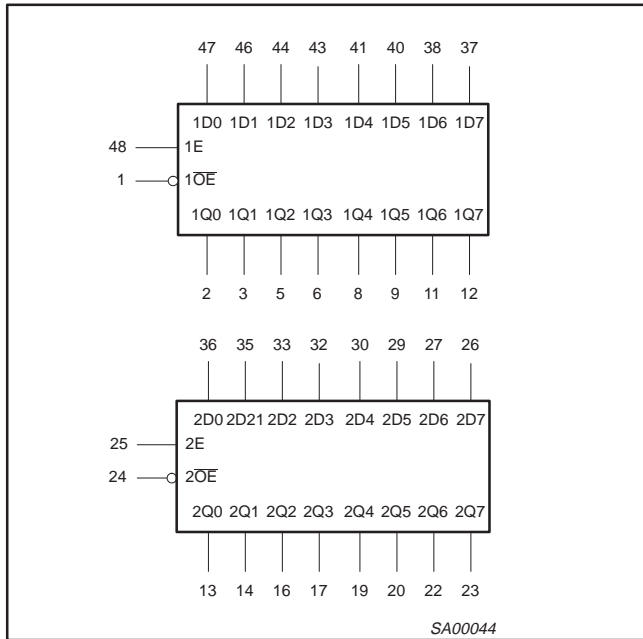
### PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1D0 – 1D7 2D0 – 2D7	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	1Q0 – 1Q7 2Q0 – 2Q7	Data outputs
1, 24	1OE, 2OE	Output enable inputs (active-LOW)
48, 25	1E, 2E	Enable inputs (active-HIGH)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0 V)
7, 18, 31, 42	V <sub>CC</sub>	Positive supply voltage

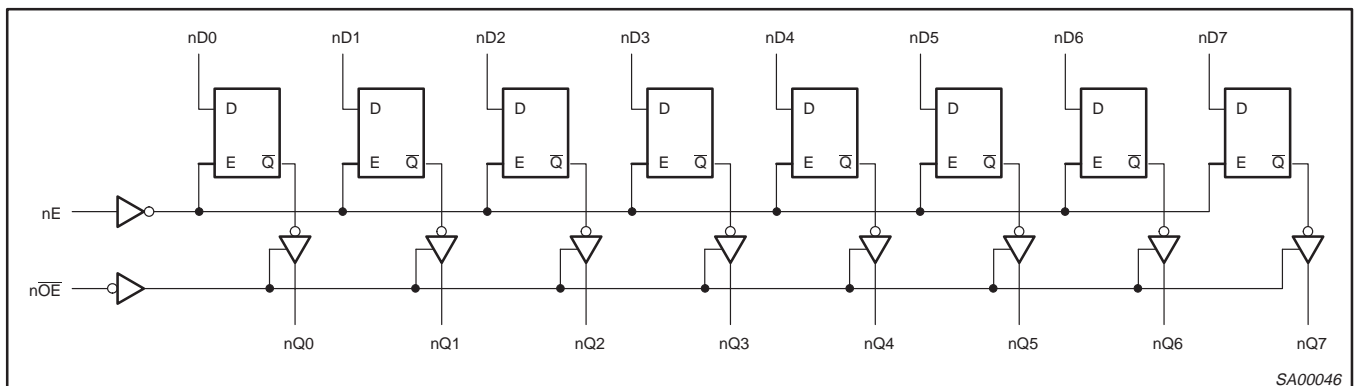
### LOGIC SYMBOL (IEEE/IEC)



### LOGIC SYMBOL



### LOGIC DIAGRAM



## 16-bit transparent latch (3-State)

74ABT16373B

## FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
nOE	nE	nDx		nQ0 – nQ7	
L L	H H	L H	L H	L H	Enable and read register
L L	↓ ↓	i h	L H	L H	Latch and read register
L	L	X	NC	NC	Hold
H H	L H	X Dn	NC Dn	Z Z	Disable outputs

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the HIGH-to-LOW E transition

L = LOW voltage level

l = LOW voltage level one set-up time prior to the HIGH-to-LOW E transition

NC= No change

X = Don't care

Z = High-impedance "off" state

↓ = HIGH-to-LOW E transition

ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V <sub>CC</sub>	DC supply voltage		-0.5 to +7.0	V
I <sub>IK</sub>	DC input diode current	V <sub>I</sub> < 0 V	-18	mA
V <sub>I</sub>	DC input voltage <sup>3</sup>		-1.2 to +7.0	V
I <sub>OK</sub>	DC output diode current	V <sub>O</sub> < 0 V	-50	mA
V <sub>OUT</sub>	DC output voltage <sup>3</sup>	output in Off or HIGH state	-0.5 to +5.5	V
I <sub>OUT</sub>	DC output current	output in LOW state	128	mA
		output in HIGH state	-64	
T <sub>stg</sub>	Storage temperature range		-65 to 150	°C

## NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V <sub>CC</sub>	DC supply voltage	4.5	5.5	V
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	V
V <sub>IH</sub>	HIGH-level input voltage	2.0	-	V
V <sub>IL</sub>	LOW-level Input voltage	-	0.8	V
I <sub>OH</sub>	HIGH-level output current	-	-32	mA
I <sub>OL</sub>	LOW-level output current	-	64	mA
Δt/Δv	Input transition rise or fall rate	0	10	ns/V
T <sub>amb</sub>	Operating free-air temperature range	-40	+85	°C

## 16-bit transparent latch (3-State)

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## DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T <sub>amb</sub> = +25 °C			T <sub>amb</sub> = -40 °C to +85 °C		
			MIN	TYP	MAX	MIN	MAX	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = 4.5 V; I <sub>IK</sub> = -18 mA	-	-0.9	-1.2		-1.2	V
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = 4.5 V; I <sub>OH</sub> = -3 mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	2.5	2.9	-	2.5	-	V
		V <sub>CC</sub> = 5.0 V; I <sub>OH</sub> = -3 mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	3.0	3.4	-	3.0	-	V
		V <sub>CC</sub> = 4.5 V; I <sub>OH</sub> = -32 mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	2.0	2.4	-	2.0	-	V
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = 4.5 V; I <sub>OL</sub> = 64 mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	-	0.42	0.55	-	0.55	V
V <sub>RST</sub>	Power-up output voltage <sup>3</sup>	V <sub>CC</sub> = 5.5 V; I <sub>O</sub> = 1 mA; V <sub>I</sub> = GND or V <sub>CC</sub>	-	0.13	0.55	-	0.55	V
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = V <sub>CC</sub> or GND	-	±0.01	±1	-	±1	µA
I <sub>OFF</sub>	Power-off leakage current	V <sub>CC</sub> = 0.0 V; V <sub>O</sub> or V <sub>I</sub> ≤ 4.5 V	-	±5.0	±100	-	±100	µA
I <sub>PU</sub> /I <sub>PD</sub>	Power-up/down 3-State output current <sup>4</sup>	V <sub>CC</sub> = 2.1 V; V <sub>O</sub> = 0.5 V; V <sub>I</sub> = GND or V <sub>CC</sub> ; V <sub>OE</sub> = GND	-	±5.0	±50	-	±50	µA
I <sub>OZH</sub>	3-State output HIGH current	V <sub>CC</sub> = 5.5 V; V <sub>O</sub> = 5.5 V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	-	0.5	10	-	10	µA
I <sub>OZL</sub>	3-State output LOW current	V <sub>CC</sub> = 5.5 V; V <sub>O</sub> = 0.0 V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	-	-0.5	-10		-10	µA
I <sub>O</sub>	Output current <sup>1</sup>	V <sub>CC</sub> = 5.5 V; V <sub>O</sub> = 2.5 V	-50	-70	-180	-50	-180	mA
I <sub>CEX</sub>	Output HIGH leakage current	V <sub>CC</sub> = 5.5 V; V <sub>O</sub> = 5.5 V; V <sub>I</sub> = GND or V <sub>CC</sub>	-	0.1	50	-	50	µA
I <sub>CCH</sub>	Quiescent supply current	V <sub>CC</sub> = 5.5 V; Outputs HIGH; V <sub>I</sub> = GND or V <sub>CC</sub>	-	0.5	2	-	2	mA
I <sub>CCL</sub>		V <sub>CC</sub> = 5.5 V; Outputs Low; V <sub>I</sub> = GND or V <sub>CC</sub>	-	8	19	-	19	mA
I <sub>CCZ</sub>		V <sub>CC</sub> = 5.5 V; Outputs 3-State; V <sub>I</sub> = GND or V <sub>CC</sub>	-	0.5	2	-	2	mA
ΔI <sub>CC</sub>	Additional supply current per input pin <sup>2</sup>	V <sub>CC</sub> = 5.5 V; one input at 3.4 V, other inputs at V <sub>CC</sub> or GND	-	5	100	-	100	µA

## NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4 V.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
- This parameter is valid for any V<sub>CC</sub> between 0 V and 2.1 V, with a transition time of up to 10 msec. From V<sub>CC</sub> = 2.1 to V<sub>CC</sub> = 5 V ± 10% a transition time of up to 100 µsec is permitted.
- Unused pins at V<sub>CC</sub> or GND.

# 16-bit transparent latch (3-State)

# 74ABT16373B

## AC CHARACTERISTICS

GND = 0 V,  $t_R = t_F = 2.5$  ns,  $C_L = 50$  pF,  $R_L = 500$   $\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			$T_{amb} = +25$ °C $V_{CC} = +5.0$ V			$T_{amb} = -40$ °C to $+85$ °C $V_{CC} = +5.0$ V $\pm$ 0.5 V		
			MIN	TYP	MAX	MIN	MAX	
$t_{PLH}$ $t_{PHL}$	Propagation delay nDx to nQx	2	1.5 1.1	2.5 2.0	3.8 3.1	1.5 1.1	4.4 3.8	ns
$t_{PLH}$ $t_{PHL}$	Propagation delay nE to nQx	1	1.6 1.3	2.5 2.1	3.8 3.1	1.6 1.3	4.4 3.6	ns
$t_{PZH}$ $t_{PZL}$	Output enable time to HIGH and LOW level	4 5	1.2 1.3	2.3 2.3	3.5 3.5	1.2 1.3	4.6 4.5	ns
$t_{PHZ}$ $t_{PLZ}$	Output disable time from HIGH and LOW level	4 5	1.9 1.7	3.1 2.6	4.5 3.8	1.9 1.7	5.3 4.2	ns

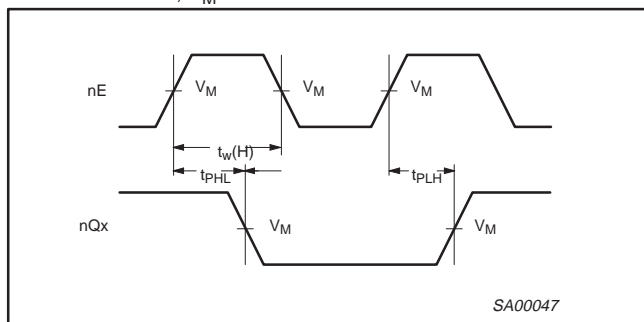
## AC SET-UP REQUIREMENTS

GND = 0 V,  $t_R = t_F = 2.5$  ns,  $C_L = 50$  pF,  $R_L = 500$   $\Omega$

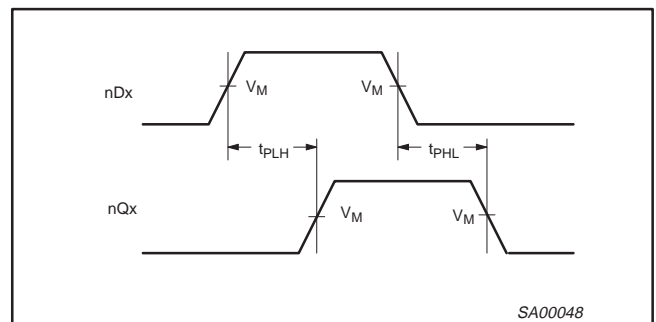
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$T_{amb} = +25$ °C $V_{CC} = +5.0$ V		$T_{amb} = -40$ °C to $+85$ °C $V_{CC} = +5.0$ V $\pm$ 0.5 V	
			MIN	TYP	MIN	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW nDx to nE	3	1.0 1.0	0.0 0.3	1.0 1.0	ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW nDx to nE	3	0.5 0.5	-0.2 0.0	0.5 0.5	ns
$t_w(H)$	Enable pulse width HIGH	1	2.5	1.0	2.5	ns

## AC WAVEFORMS

For all waveforms,  $V_M = 1.5$  V.



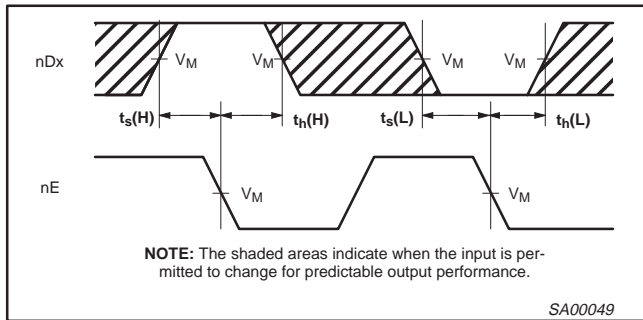
Waveform 1. Propagation Delay, Enable to Output, and Enable Pulse Width



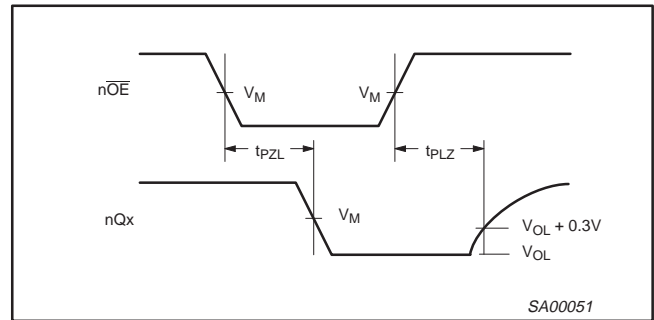
Waveform 2. Propagation Delay for Data to Outputs

# 16-bit transparent latch (3-State)

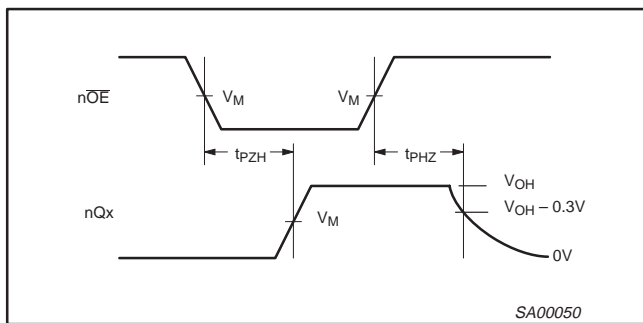
# 74ABT16373B



**Waveform 3. Data Set-up and Hold Times**



**Waveform 5. 3-State Output Enable Time to LOW Level and Output Disable Time from LOW Level**



**Waveform 4. 3-State Output Enable Time to HIGH Level and Output Disable Time from HIGH Level**

## TEST CIRCUIT AND WAVEFORM

**Test Circuit for 3-State Outputs**

**Input Pulse Definition**

$V_M = 1.5\text{ V}$

**SWITCH POSITION**

TEST	SWITCH
$t_{PLZ}$	closed
$t_{PZL}$	closed
All other	open

**DEFINITIONS**

$R_L$  = Load resistor; see AC CHARACTERISTICS for value.

$C_L$  = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

$R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	$t_w$	$t_R$	$t_F$
74ABT	3.0 V	1 MHz	500 ns	2.5 ns	2.5 ns

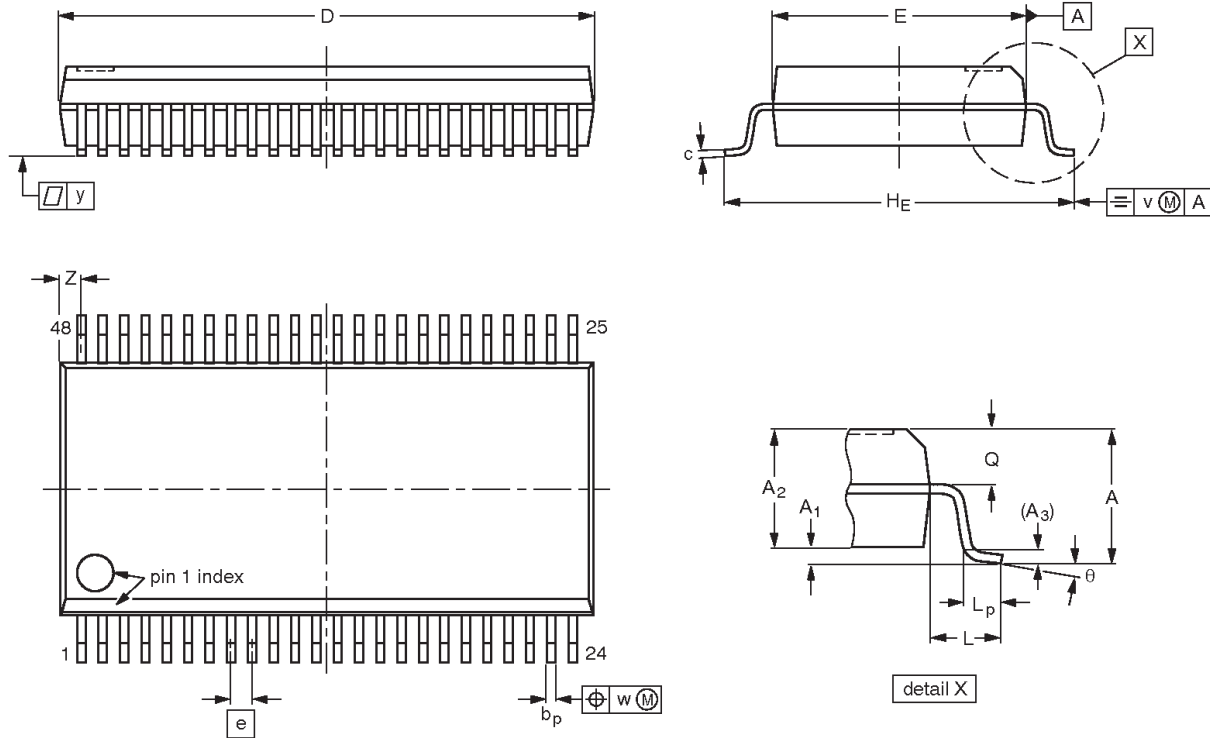
SA00654

# 16-bit transparent latch (3-State)

# 74ABT16373B

**SSOP48:** plastic shrink small outline package; 48 leads; body width 7.5 mm

**SOT370-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT370-1		MO-118				99-12-27 03-02-19

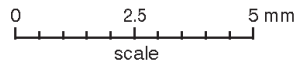
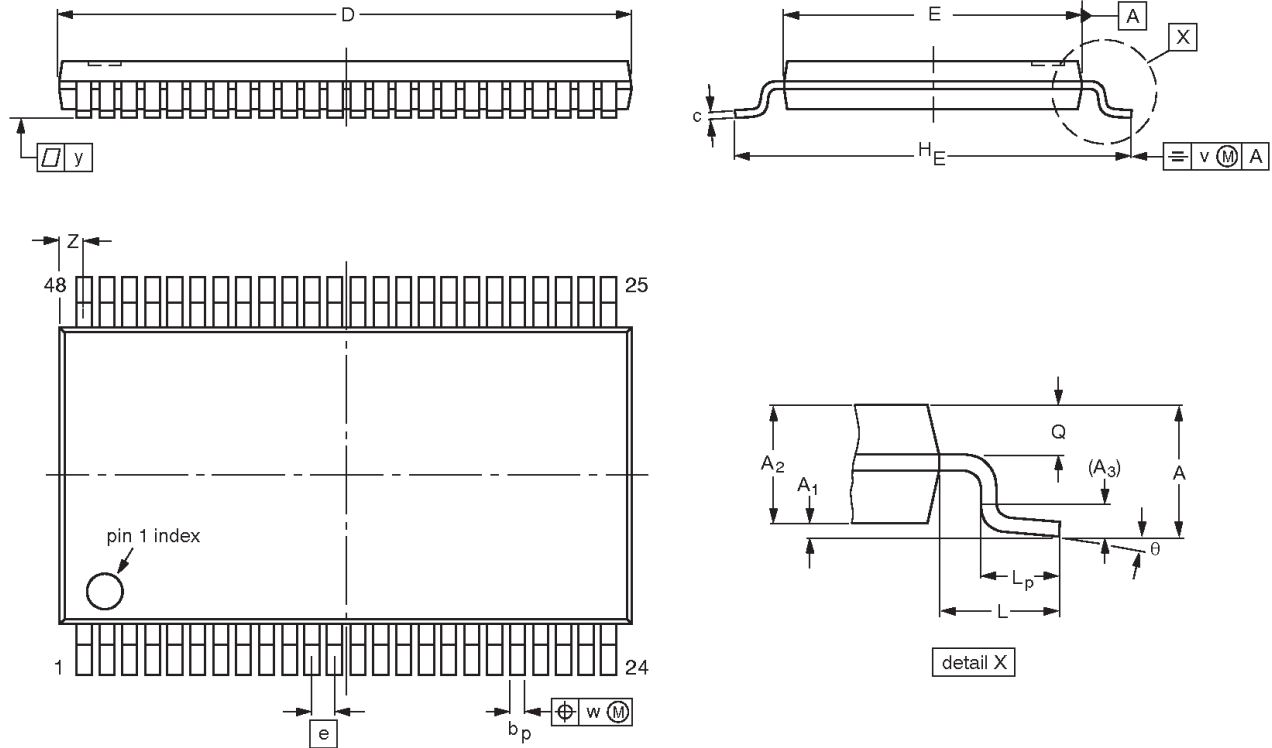


# 16-bit transparent latch (3-State)

## 74ABT16373B

**TSSOP48:** plastic thin shrink small outline package; 48 leads; body width 6.1 mm

**SOT362-1**



**DIMENSIONS (mm are the original dimensions).**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				-99-12-27 03-02-19

## 16-bit transparent latch (3-State)

74ABT16373B

**REVISION HISTORY**

Rev	Date	Description
_3	20040227	<b>Product data (9397 750 12821); 853-1751 ECN 01-A15429 of 27 January 2004.</b> <b>Replaces data sheet 74ABT_H16373B_2 of 1998 Feb 27 (9397 750 03491).</b> Modifications: <ul style="list-style-type: none"><li>• Delete all references to 74ABTH16373B (product discontinued).</li></ul>
_2	19980227	<b>Product specification (9397 750 03491); ECN 853-1751 19027 of 27 February 1998.</b> <b>Supersedes data of 1995 Aug 03.</b>
_1	19950803	

## 16-bit transparent latch (3-State)

74ABT16373B

## Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2] [3]</sup>	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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