

TOSHIBA Field Effect Transistor Silicon P Channel MOS Type

SSM3J05FU

Power Management Switch

High Speed Switching Applications

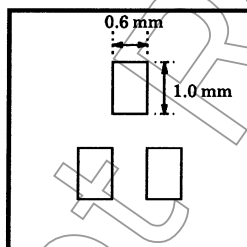
- Small package
- Low on resistance: $R_{on} = 3.3 \Omega$ (max) (@ $V_{GS} = -4$ V)
: $R_{on} = 4.0 \Omega$ (max) (@ $V_{GS} = -2.5$ V)
- Low gate threshold voltage

Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

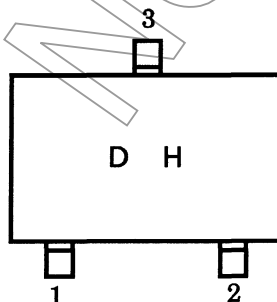
Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DS}	-20	V
Gate-source voltage		V_{GSS}	± 12	V
Drain current	DC	I_D	-200	mA
	Pulse	I_{DP}	-400	
Drain power dissipation ($T_a = 25^\circ\text{C}$)		P_D (Note 1)	150	mW
Channel temperature		T_{ch}	150	$^\circ\text{C}$
Storage temperature range		T_{stg}	-55~150	$^\circ\text{C}$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

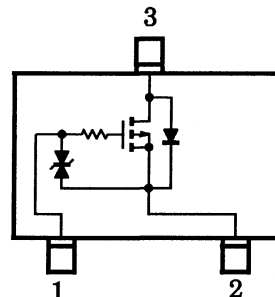
Note 1: Mounted on FR4 board.
(25.4 mm \times 25.4 mm \times 1.6 t, Cu pad: 0.6 mm² \times 3)



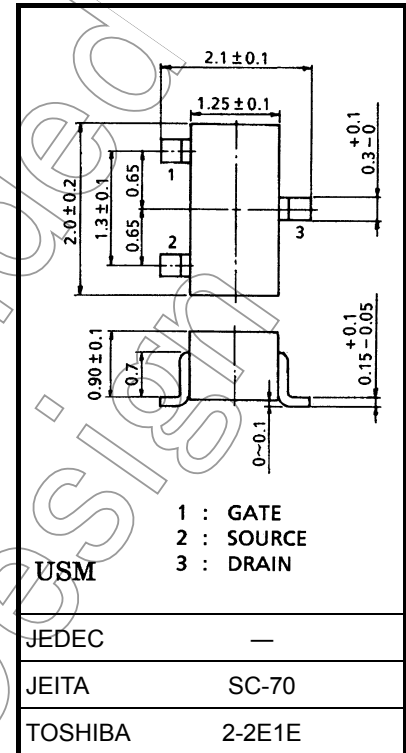
Marking



Equivalent Circuit



Unit: mm



Weight: 0.006 g (typ.)

Handling Precaution

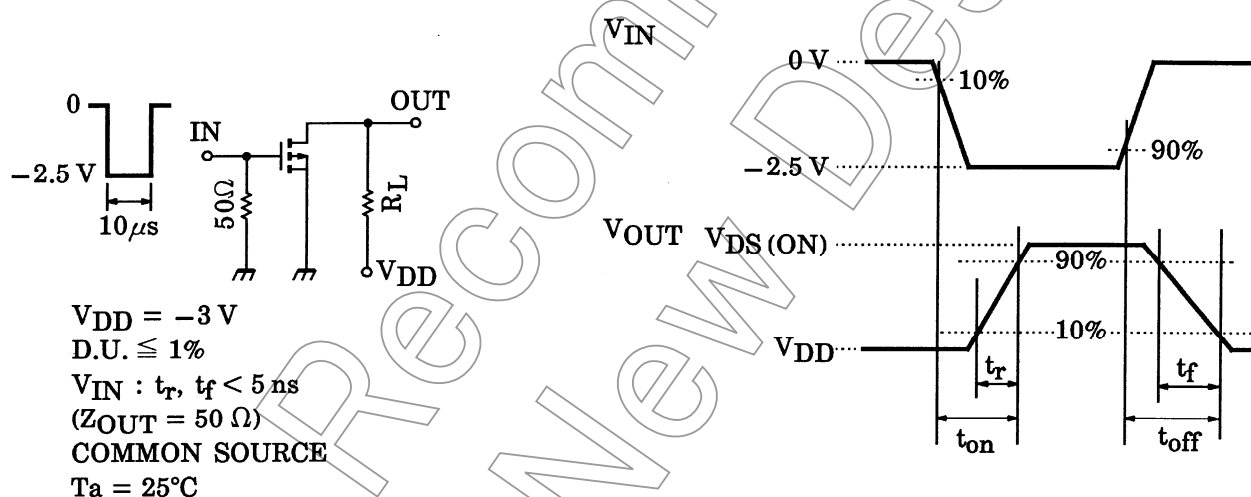
When handling individual devices (which are not yet mounting on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

Electrical Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	I_{GSS}	$V_{GS} = \pm 12\text{ V}, V_{DS} = 0$	—	—	± 1	μA
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = -1\text{ mA}, V_{GS} = 0$	-20	—	—	V
Drain cut-off current	I_{DSS}	$V_{DS} = -20\text{ V}, V_{GS} = 0$	—	—	-1	μA
Gate threshold voltage	V_{th}	$V_{DS} = -3\text{ V}, I_D = -0.1\text{ mA}$	-0.6	—	-1.1	V
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = -3\text{ V}, I_D = -50\text{ mA}$ (Note 2)	100	—	—	mS
Drain-source ON resistance	$R_{DS(ON)}$	$I_D = -100\text{ mA}, V_{GS} = -4\text{ V}$ (Note 2)	—	2.1	3.3	Ω
		$I_D = -50\text{ mA}, V_{GS} = -2.5\text{ V}$ (Note 2)	—	3.2	4.0	
Input capacitance	C_{iss}	$V_{DS} = -3\text{ V}, V_{GS} = 0, f = 1\text{ MHz}$	—	27	—	pF
Reverse transfer capacitance	C_{rss}	$V_{DS} = -3\text{ V}, V_{GS} = 0, f = 1\text{ MHz}$	—	7	—	pF
Output capacitance	C_{oss}	$V_{DS} = -3\text{ V}, V_{GS} = 0, f = 1\text{ MHz}$	—	21	—	pF
Switching time	Turn-on time	$V_{DD} = -3\text{ V}, I_D = -50\text{ mA}, V_{GS} = 0 \sim -2.5\text{ V}$	—	70	—	ns
	Turn-off time		—	70	—	

Note 2: Pulse test

Switching Time Test Circuit

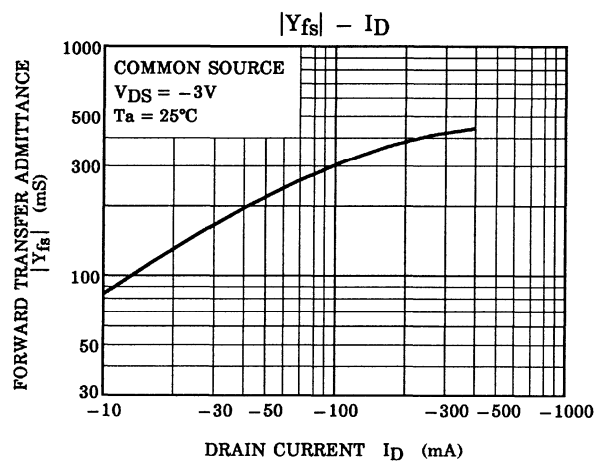
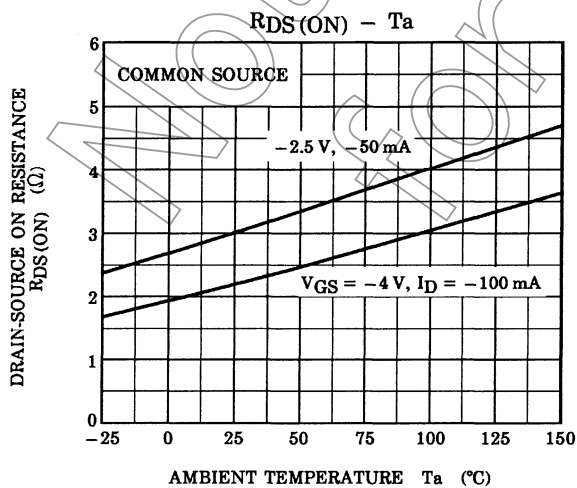
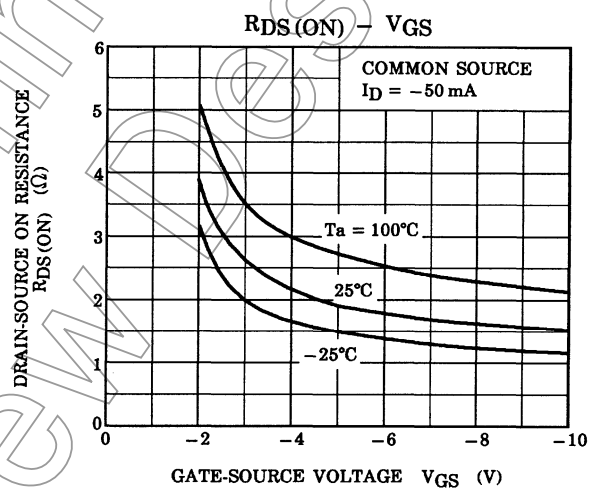
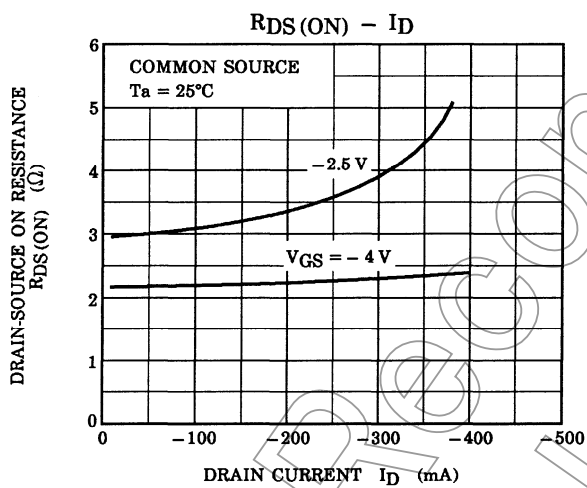
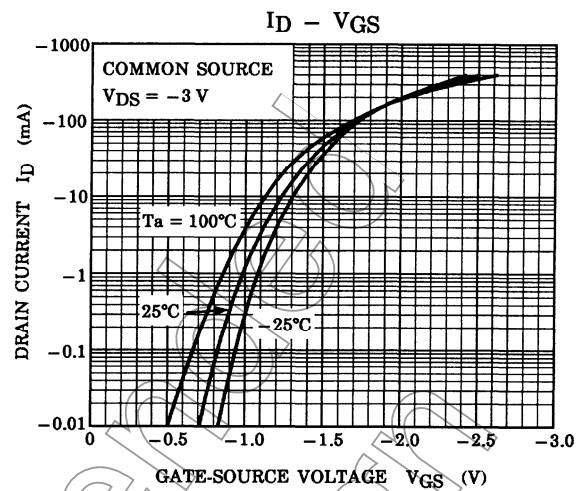
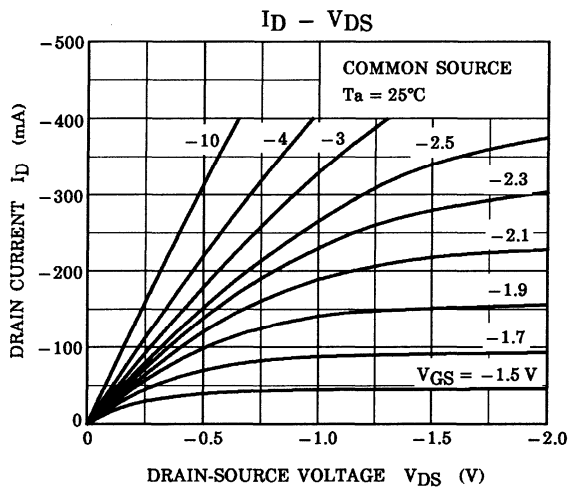


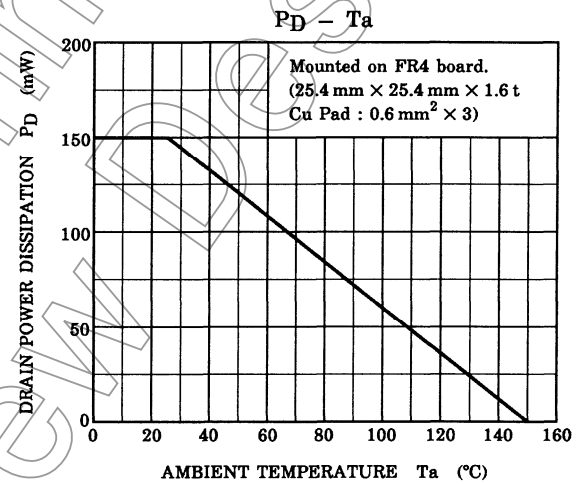
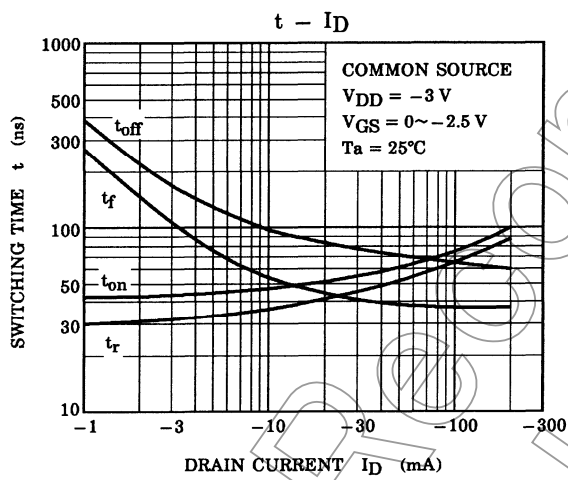
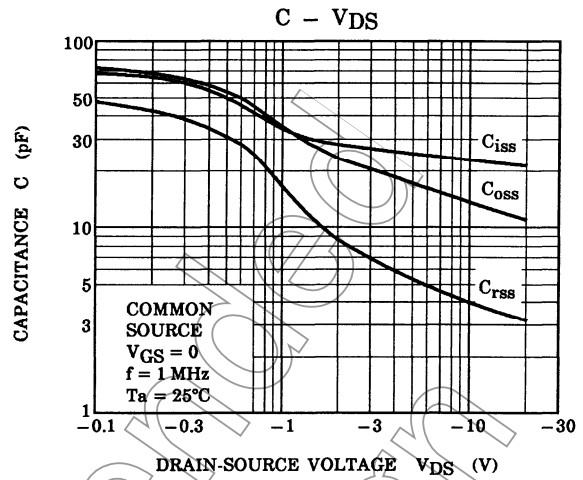
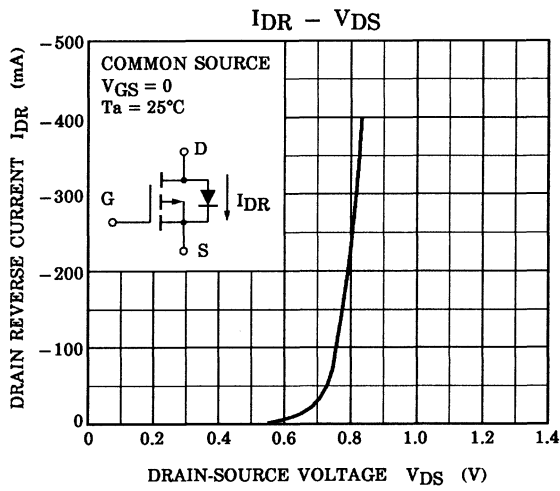
Precaution

V_{th} can be expressed as voltage between gate and source when low operating current value is $I_D = -100\ \mu\text{A}$ for this product. For normal switching operation, $V_{GS(ON)}$ requires higher voltage than V_{th} and $V_{GS(off)}$ requires lower voltage than V_{th} .

(Relationship can be established as follows: $V_{GS(off)} < V_{th} < V_{GS(ON)}$)

Please take this into consideration for using the device.





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