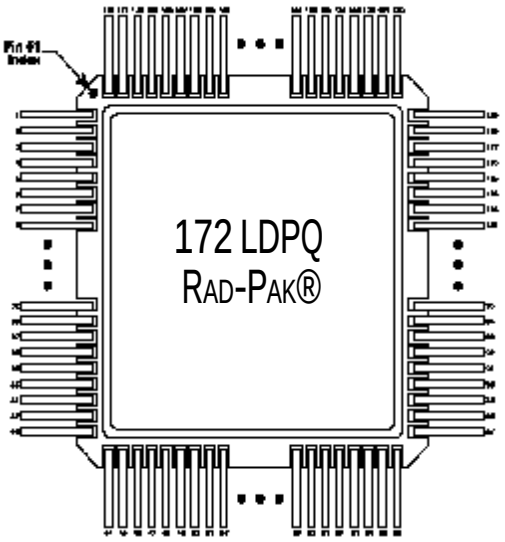
PRELIMINARY

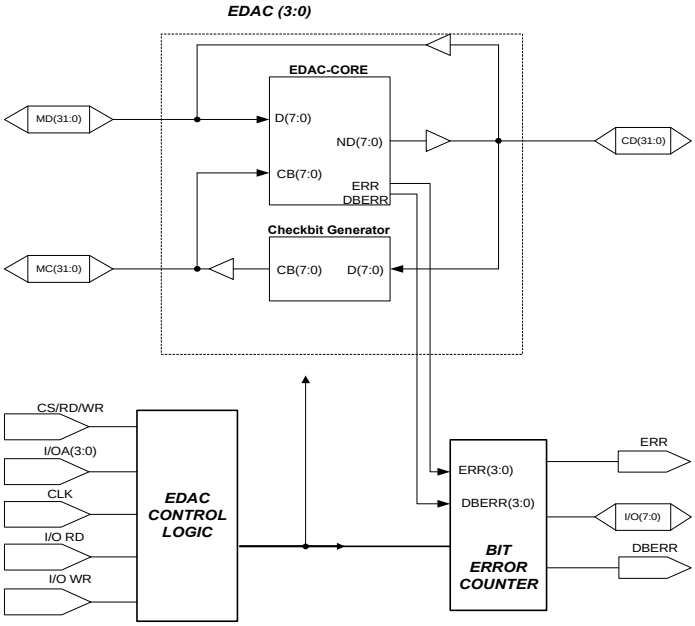
SPACE ELECTRONICS INC.
SPACE PRODUCTS

8/16/32 BIT SRAM EDAC

49S32DRP



FUNCTIONAL BLOCK DIAGRAM



FEATURES:

- Operates as 8, 16, or 32 bit EDAC
- No single event latchup > 100 MeV/mg/cm^2
- Single event upset ≥ IE -10 upsets/day
- Total dose hardness100 krad (Si) typical
- Package:
  - 172 pin RAD-PAK® quad flat pack
  - Weight: 20 grams
- Cascadable to 64 bit EDAC
- Flow-thru architecture
- Super-high speed
- Single and double bit error detection
- Single bit error counter
- Single bit auto-correct
- Double bit error counter
- No Read-Modify-Write required for partial word writes
- Absolute minimum gate usage

DESCRIPTION:

Space Electronics' 49S32DRP high speed CMOS SRAM EDAC (Error Dectection and Correction) features a minimum 100 kilorad (Si) total dose tolerance. The 49S32DRP does not require Read-Modify-Write to memory for partial word writes, thus can be used as an 8, 16, or 32 bit EDAC. These partial-word writes may be done in single bus cycle without performance penalties. The 49S32DRP incorporates four separate byte-wide EDAC modules in parallel. Each module is broken down into two main blocks -- the check bit generator (CBG) and the read/correct data (CORR). The unique flow-thru architecture achieves 25ns from data in (MD) to corrected data out (CD). Two readable error counters allow single-bit error (ERR) and double-bit error (DBERR) tracking. Error signals can be internally masked via two mask bits. Capable of surviving space environments, the SRAM EDAC is ideal for satellite, spacecraft, and space probe missions. The RAD-PAK® technology incorporates radiation shielding in the microcircuit package. It eliminates box shielding while providing lifetime in orbit. The SRAM EDAC is available with packaging and screening up to Class S.

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TABLE 1. 49S32DRP PIN DESCRIPTION

NAME	SYMBOL	I/O	FUNCTION
Memory Data Bus	MD0-7, MD8-15, MD16-23, MD24-31	I/O	These I/O pines accept 8, or 16, or 32 bit data word from main memory for error detection and/or correction.
Memory CheckBit Bus	MC0-7, MC8-15, MC16-23, MC24-31	I/O	The memory checkbits of 8, or 16, or 32 bits pins accept checkbits from the checkbit memory for error detection and/or correction. They also output corrected checkbits to checkbit memory when the 49S32DRP is used in bi-directional configuation.
CPU Data Bus	CD0-7, CD8-15, CD16-23, CD24-31	I/O	Data from MD0-31 appears at these pins corrected when in memory read mode. Partial-writes are done without read-modify-writes.
Memory Read Bus	MEM_RD0-3	I	Allows read select for four SRAM modules when performing data writes to memory.
Memory Write Bus	MEM_WR0-3	I	Allows write select for four SRAM modules when performing data writes to memory.
I/O Read	IO_RD	I	Selects the internal I/O registers for read.
I/O Write	IO_WR	I	Selects the internal I/O registers for write.
SRAM Chip Select Bus	SRAM_CS0-3	I	Selects memory modules 0 to 3 for read or write modules.
Clock A	CLKIN_A	I	System clock for 49S32DRP.
Clock B	CLKIN_B	I	Internal error counter clock.
Reset	RESET	I	Global reset. Clears 49S32DRP EDAC cores to all zeros.
I/O Address Bus	IO_A0-2	I	Internal I/O register address bus.
Error Counter Bus	IO_OUT0-7	I/O	Internal I/O register data bus.
Double Bit Error	DBERR	O	Indicates a double bit error has occurred.

TABLE 2. 49S32DRP ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	SYMBOL	MIN	MAX	UNITS
DC Voltage Supply	V_{CC}	-0.5	+7.0	V
Input Voltage	V_I	-0.5	V_{CC} + 0.5	V
Output Voltage	V_O	-0.5	V_{CC} + 0.5	V
I/O Source/Sink Current [2]	I_{IO}	-20	+20	mA
Storage Temperature	T_{STG}	-65	+150	°C

1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operationg Condition.
2. Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than V_{CC} + 0.5 or less than GND -0.5V, the internal protection diode will be forward-biased and can draw excessive current.

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TABLE 3. 49S32DRP RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	MAX	UNITS
Temperature Range [1]	-55	+125	°C
Power Supply Tolerance	-10	+10	$\%V_{CC}$

1. Case temperature (T_C) is used.

TABLE 4. 49S32DRP DC ELECTRICAL SPECIFICATIONS

SYMBOL	TEST CONDITIONS	GROUP A SUBGROUPS	LIMIT		UNITS
			MIN	MAX	
V_{OH}[1]	I_{OH} = -4 mA	1,2,3	3.7	--	V
V_{OL}[1]	I_{OL} - 4 mA	1,2,3	--	+0.4	V
V_{IH}		1,2,3	2.2	V_{CC} + 3	V
V_{IL}		1,2,3	-0.3	+0.8	V
Input Transition Ti me t_R, t_F[2]		--	--	+500	ns
C_{IO}, I/O Capacitance[2]		4	--	+20	pF
I_{IH}, I_{IL}	V_{IN} = V_{CC} or GND, V_{CC} = 5.5V	1,2,3	-10	+10	µA
I_{OZL}, I_{OZH}	V_{OUT} = V_{CC} or GND, V_{CC} = 5.5V	1,2,3	-10	+10	µA
I_{CC} Standby[3]		1,2,3	--	25	mA
I_{CC} Active[3,4]		1,2,3	--	325 typ	mA

1. Only one output tested at a time. V_{CC} = min.
2. Not tested, for information only.
3. All outputs unloaded. All inputs = V_{CC} or GND.
4. At 50 MHz.

TABLE 5. 49S32DRP AC ELECTRICAL CHARACTERISTICS

PROPICATION DELAY FROM INPUT	TO OUTPUT [1]			UNIT
	CD DATA OUT	ERR SINGLE BIT ERROR	DBERR SINGLE BIT ERROR	
MD Data In	25 max	25 max	25 max	nS

1. Dependent upon ASIC and/or FPGA type.

TABLE 6. 49S32DRP PIN ASSIGNMENT

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	NC	2	MD0	3	MD1

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TABLE 6. 49S32DRP PIN ASSIGNMENT

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
4	MD2	5	MD3	6	MD4
7	GND	8	MD5	9	MD6
10	MD7	11	MEM_RD0	12	V_{CC}
13	MEM_RD1	14	MD8	15	MD9
16	MD10	17	GND	18	MD11
19	MD12	20	MD13	21	MD14
22	GND	23	V_{CC}	24	V_{CC}
25	MD15	26	MEM_RD2	27	V_{CC}
28	MEM_RD3	29	MD16	30	MD17
31	MD18	32	GND	33	MD19
34	MD20	35	MD21	36	MD22
37	GND	38	MD23	39	MD24
40	MD25	41	MD26	42	MD27
43	MD28	44	MD29	45	MD30
46	MD31	47	MEM_WR0	48	MEM_WR1
49	MEM_WR2	50	V_{CC}	51	MEM_WR3
52	MC0	53	MC1	54	MC2
55	GND	56	MC3	57	MC4
58	MC5	59	MC6	60	MC7
61	MC8	62	MC9	63	MC10
64	MC11	65	GND	66	V_{CC}
67	ERR	68	MC12	69	MC13
70	MC14	71	MC15	72	MC16
73	MC17	74	MC18	75	GND
76	MC19	77	MC20	78	MC21
79	IO_RD	80	V_{CC}	81	IO_WR
82	MC22	83	MC23	84	MC24
85	MC25	86	MC26	87	MC27
88	MC28	89	MC29	90	MC30
91	MC31	92	IO_OUT_D0	93	IO_OUT_D1
94	IO_OUT_D2	95	IO_OUT_D3	96	IO_OUT_D4
97	IO_OUT_D5	98	GND	99	IO_OUT_D6
100	IO_OUT_D7	101	IO_A0	102	IO_A1
103	GND	104	IO_A2	105	CS_IO
106	GND	107	V_{CC}	108	GND
109	V_{CC}	110	V_{CC}	111	DBERR
112	RESET	113	V_{CC}	114	NC

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TABLE 6. 49S32DRP PIN ASSIGNMENT

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
115	CD0	116	CD1	117	CD2
118	GND	119	CD3	120	CD4
121	CD5	122	CD6	123	GND
124	CD7	125	CD8	126	CD9
127	CD10	128	CD11	129	CD12
130	CD13	131	(SDI)*	132	CD14
133	CD15	134	SRAM_CS0	135	SRAM_CS1
136	V_{CC}	137	SRAM_CS2	138	SRAM_CS3
139	CD16	140	CD17	141	GND
142	CD18	143	CD19	144	CD20
145	CD21	146	CD22	147	CD23
148	CD24	149	READY	150	CLKIN
151	V_{CC}	152	GND	153	CD25
154	SPARE4	155	CD26	156	CD27
157	CD28	158	CD29	159	CD30
160	CD31	161	GND	162	NC
163	NC	164	NC	165	NC
166	V_{CC}	167	NC	168	NC
169	NC	170	NC	171	NC
172	NC				

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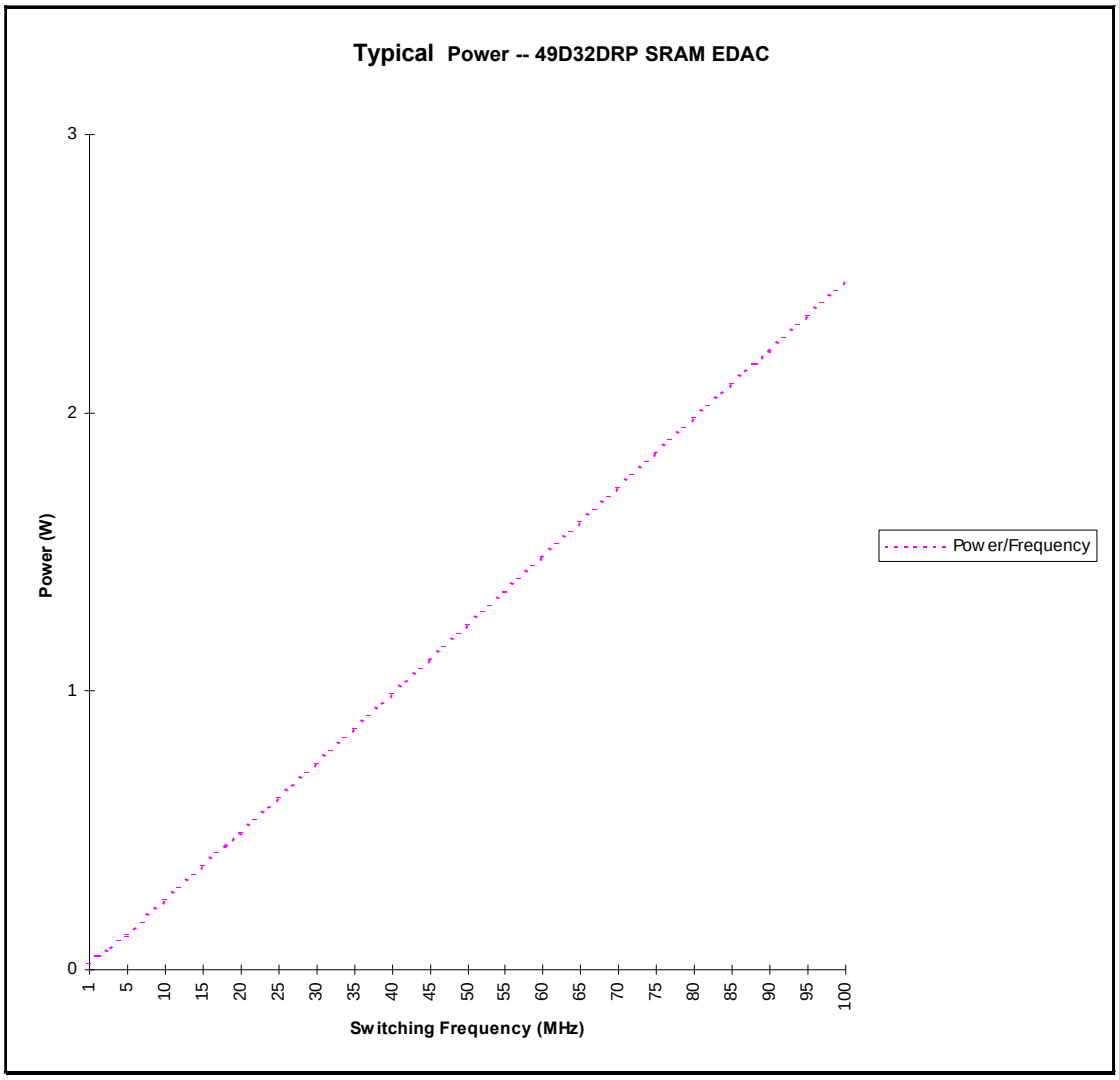

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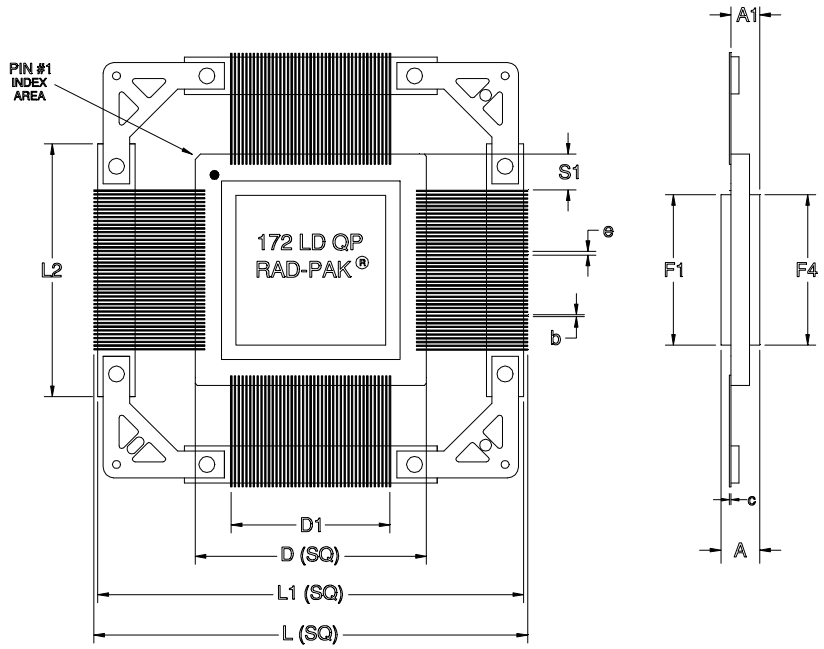

172 PIN RAD-PAK® QUAD FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.116	0.133	0.146
b	0.007	0.008	0.013
c	0.004	0.006	0.009
D	1.138	1.150	1.162
D1		1.050 BSC	
e		0.025 BSC	
S1	0.013	0.046	--
F1	0.890	0.895	0.900
F4	0.881	0.890	0.899
L	2.500	2.520	2.540
L1	2.485	2.500	2.505
L2	1.690	1.700	1.710
A1	0.079	0.091	0.103
N		172	

Q172-01
Note: All dimensions in inches

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