

4-Bit Decade Counter, 4-Bit Binary Counter

The LS/ALS90 and LS/ALS93 are 4-bit ripple type Decade and Binary Counters, respectively. Each device consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and a divide-by-five (LS/ALS90), or divide-by-eight (LS/ALS93) section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous Master Reset ($\overline{MR}_1$, $\overline{MR}_2$) is provided on all counters which overrides and clears all the flip-flops. A gated AND asynchronous Master Set ($\overline{MS}_1$, $\overline{MS}_2$) is provided on the LS/ALS 90 which overrides the clocks and the MR inputs and sets the outputs to count nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes.

LS/ALS90

A. BCD Decade Counter — The $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count and a BCD count sequence is produced.

B. Symmetrical Bi-quinary Divide-By-Ten Counter — The Q_3 output must be externally connected to the $\overline{CP}_0$ input. The input count is then applied to the $\overline{CP}_1$ input and a divide-by-ten square wave is obtained at output Q_0 .

C. Divide-By-Two and Divide-By-Five Counter — No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function ($\overline{CP}_0$ as the input and Q_0 as the output). The $\overline{CP}_1$ input is used to obtain binary divide-by-five operation at the Q_3 output.

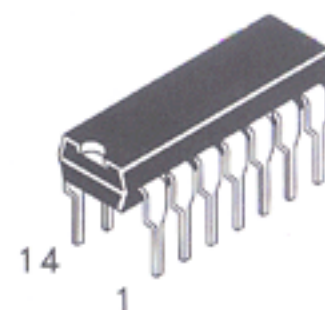
LS/ALS93

A. 4-Bit Ripple Counter — The output Q_0 must be externally connected to input $\overline{CP}_1$. The input count pulses are applied to input $\overline{CP}_0$. Simultaneous divisions of 2, 4, 8 and 16 are performed at the Q_0 , Q_1 , Q_2 , and Q_3 outputs as shown in the truth table.

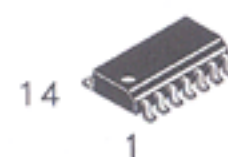
B. 3-Bit Ripple Counter — The input count pulses are applied to input $\overline{CP}_1$. Simultaneous frequency divisions of 2, 4 and 8 are available at the Q_1 , Q_2 , and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

- AVG's LS operates over extended V_{CC} from 4.5 to 5.5 V
- AVG's LS and ALS both have guaranteed DC and AC specification over full temperature and V_{CC} range
- Switching specifications for ALS at 50 pF
- AVG's ALS has the lowest speed power product (4pJ per gate typical) of all logic series

DV74LS90, DV74ALS90, DV74LS93, DV74ALS93

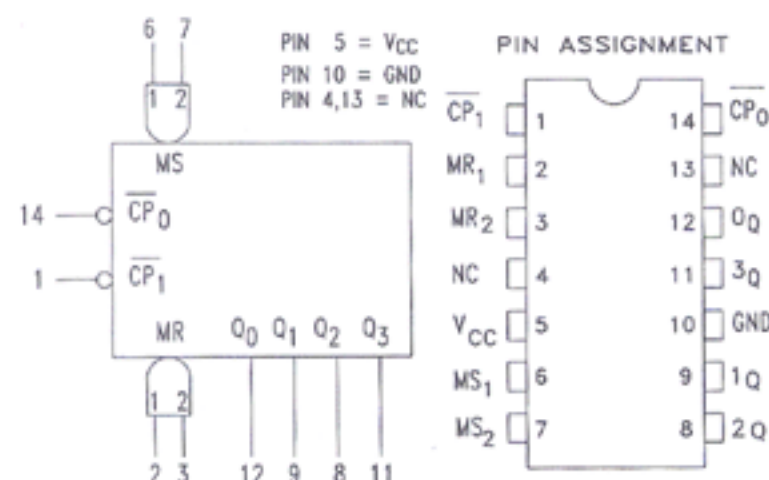


N Suffix
Plastic DIP
AVG-001 Case

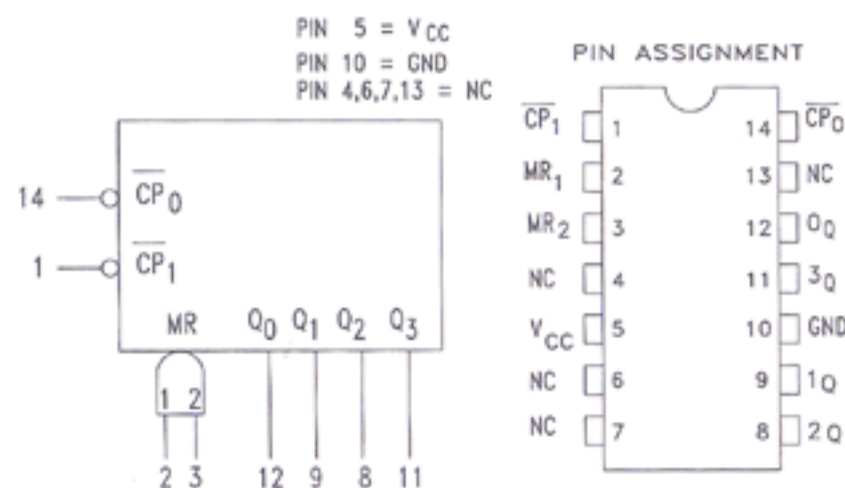


D Suffix
Plastic SOP
AVG-002 Case

LS90 and ALS90



LS93 and ALS93



ABSOLUTE MAXIMUM RATINGS

Maximum ratings are those values beyond which damage to the device may occur.

Symbol	Parameter	LS90, LS93	ALS90, ALS93	Unit
V _{CC}	Supply Voltage	7.0	7.0	V
V _{IN}	Input Voltage	7.0	7.0	V
T _{STG}	Storage Temperature Range	–65 to +150	–65 to +150	°C

GUARANTEED OPERATING CONDITIONS

Symbol	Parameter	LS90, LS93		ALS90, ALS93		Unit
		Min	Max	Min	Max	
V _{CC}	Supply Voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High Level Input Voltage	2.0		2.0		V
V _{IL}	Low Level Input Voltage		0.8		0.8	V
I _{OH}	High Level Output Current		–0.4		–0.4	mA
I _{OL}	Low Level Output Current		8.0		8.0	mA
T _A	Ambient Temperature Range	–10 to +70		–10 to +70		°C

DC ELECTRICAL CHARACTERISTICS over full operating conditions

Symbol	Parameter	Conditions	LS90, LS93			ALS90, ALS93			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{IK}	Input Clamp Voltage	V _{CC} = min, I _{IN} = –18 mA			–1.5			–1.5	V
V _{OH}	High Level Output Voltage	V _{CC} =min, I _{OH} =max	V _{CC} –2	3.5		V _{CC} –2			V
V _{OL}	Low Level Output Voltage	V _{CC} =min; I _{OL} =4.0mA		0.25	0.4		0.25	0.4	V
		V _{CC} =min; I _{OL} =8.0 mA		0.35	0.5		0.35	0.5	V
I _{IH}	High Level Input Current	V _{CC} =max, V _{IH} =2.7V			20			20	μA
		V _{CC} =max, V _{IH} = 7.0V			0.1			0.1	mA
I _{IL}	Low Level Input Current MS, MR CP ₀ CP ₁ (LS90) CP ₁ (LS93)	V _{CC} =max, V _{IN} =0.4V							mA
					–0.4			–0.1	
					–2.4			–0.6	
					–3.2			–0.8	
					–1.6			–0.4	
I _O	Short Circuit Current	V _{CC} =max, V _O =2.25V	–20		–110	–30		–112	mA
I _{CC}	Supply Current	V _{CC} =max			15			11	mA

SWITCHING CHARACTERISTICS over full operating conditions

Symbol	Parameter	LS90				ALS93				Unit
		LS90 C _L =15pF		LS93 C _L =15pF		ALS90 C _L =50pF R _L =500Ω		ALS93 C _L =50pF R _L =500Ω		
		Min	Max	Min	Max	Min	Max	Min	Max	
f _{max}	CP ₀ Input Clock Frequency	32		32		40		40		MHz
f _{max}	CP ₁ Input Clock Frequency	16		16		20		20		MHz
t _{PLH}	Propagation Delay, CP ₀ Input to Q0 Output		16		16		10		10	ns
t _{PHL}			18		18		12		12	
t _{PLH}	Propagation Delay, CP ₀ Input to Q3 Output		48		70		30		40	ns
t _{PHL}			50		70		32		40	

SWITCHING CHARACTERISTICS (Continued)

Symbol	Parameter	LS				ALS				Unit
		LS90 C _L =15pF		LS93 C _L =15pF		ALS90 C _L =50pF R _L =500Ω		ALS93 C _L =50pF R _L =500Ω		
		Min	Max	Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay, CP ₁ Input to Q1 Output		16		16		12		12	ns
t _{PHL}			21		21		15		15	
t _{PLH}	Propagation Delay, CP ₁ Input to Q2 Output		32		32		20		20	ns
t _{PHL}			35		35		22		22	
t _{PLH}	Propagation Delay, CP ₁ Input to Q3 Output		32		51		20		30	ns
t _{PHL}			35		51		22		30	
t _{PLH}	MS Input to Q0 and Q3 Outputs		30				20			ns
t _{PHL}	MS Input to Q1 and Q2 Outputs		40				25			ns
t _{PHL}	MR Input to Any Output		40		40		25		25	ns

AC SETUP REQUIREMENTS over full operating conditions

Symbol	Parameter	LS90	LS93	ALS90	ALS93	Unit
		Min	Min	Min	Min	
t_w	CP ₀ Pulse Width	15	15	10	10	ns
t_w	CP ₁ Pulse Width	30	30	18	18	ns
t_w	MS Pulse Width	15		10		ns
t_w	MR Pulse Width	15	15	10	10	ns
t_{rec}	Recovery Time MR to CP	25	25	15	15	ns

LS90, ALS90
MODE SELECTION

RESET/SET INPUTS				OUTPUTS			
MR1	MR2	MS1	MS2	Q0	Q1	Q2	Q3
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X	Count			
X	L	X	L	Count			
L	X	X	L	Count			
X	L	L	X	Count			

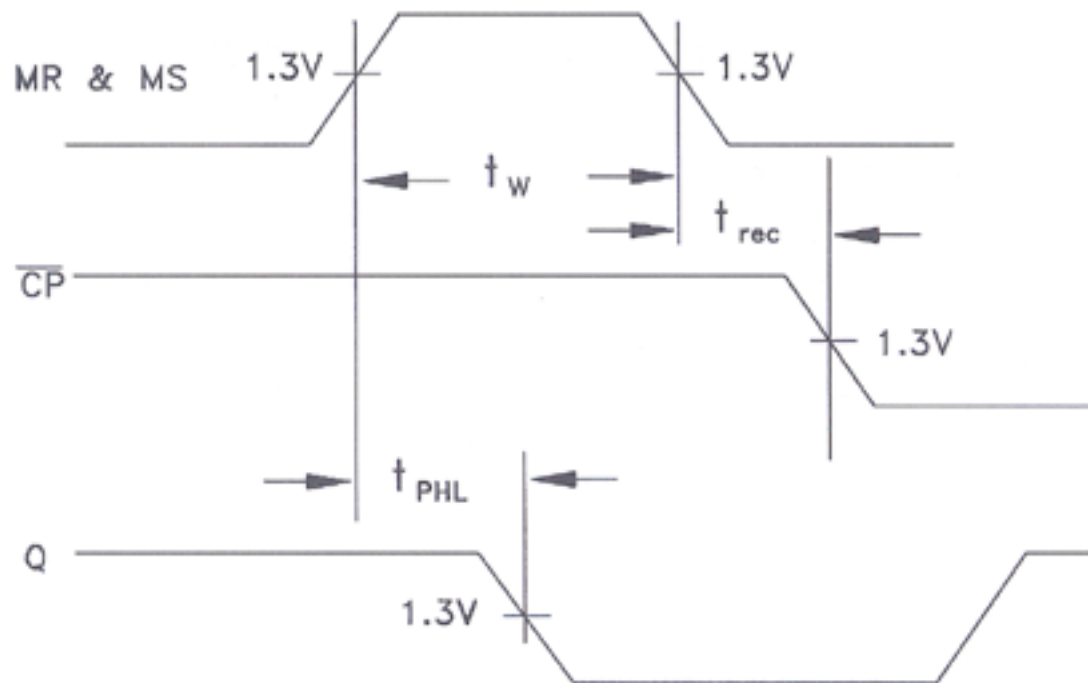
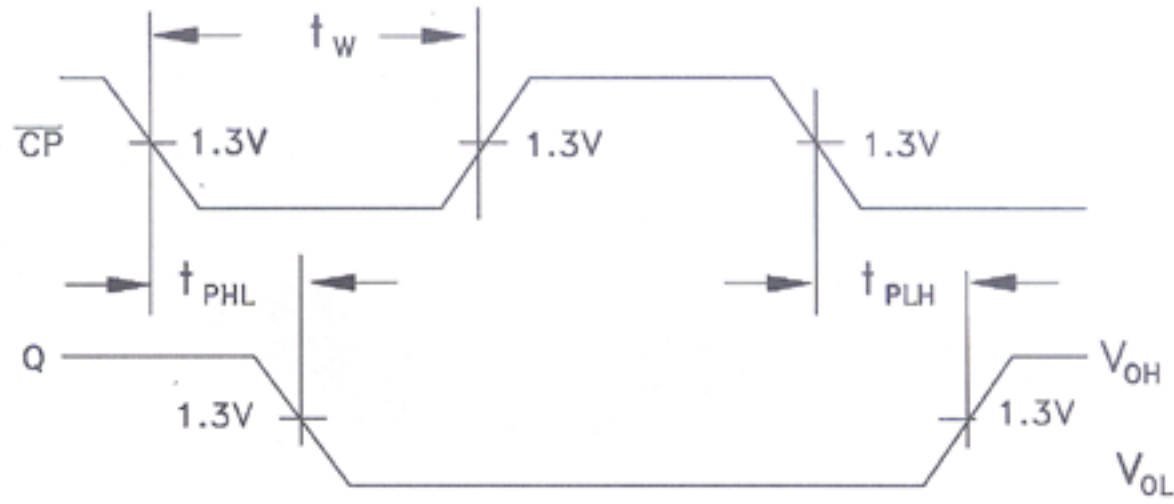
H = High Logic Level
L = Low Logic Level
X = Don't Care

LS90, ALS90
BCD COUNT SEQUENCE

COUNT	OUTPUT			
	Q0	Q1	Q2	Q3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

H = High Logic Level
L = Low Logic Level

SWITCHING WAVEFORMS



LS93, ALS93
BINARY COUNT SEQUENCE

LS93, ALS93
MODE SELECTION

RESET INPUTS		OUTPUTS			
MR1	MR2	Q0	Q1	Q2	Q3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

H = High Logic Level
L = Low Logic Level

COUNT	OUTPUT			
	Q0	Q1	Q2	Q3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

H = High Logic Level
L = Low Logic Level
X = Don't Care