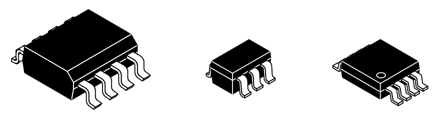


SLOS378B − SEPTEMBER 2001 − REVISED MARCH 2012

FAMILY OF MICROPOWER RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

FEATURES

- **BiMOS Rail-to-Rail Output**
- **Input Bias Current . . . 1 pA**
- **High Wide Bandwidth . . . 160 kHz**
- **High Slew Rate . . . 0.1 V/µs**
- **Supply Current . . . 7 µA (per channel)**
- **Input Noise Voltage . . . 89 nV/√Hz**
- **Supply Voltage Range . . . 2.7 V to 16 V**
- **Specified Temperature Range**
  - **−40°C to 125°C . . . Industrial Grade**
  - **0°C to 70°C . . . Commercial Grade**
- **Ultra-Small Packaging**
  - **5 Pin SOT-23 (TLV27L1)**

APPLICATIONS

- **Portable Medical**
- **Power Monitoring**
- **Low Power Security Detection Systems**
- **Smoke Detectors**

DESCRIPTION

The TLV27Lx single supply operational amplifiers provide rail-to-rail output capability. The TLV27Lx takes the minimum operating supply voltage down to 2.7 V over the extended industrial temperature range, while adding the rail-to-rail output swing feature. The TLV27Lx also provides 160-kHz bandwidth from only 7 µA. The maximum recommended supply voltage is 16 V, which allows the devices to be operated from (±8-V supplies down to ±1.35 V) two rechargeable cells.

The rail-to-rail outputs make the TLV27Lx good upgrades for the TLC27Lx family—offering more bandwidth at a lower quiescent current. The TLV27Lx offset voltage is equal to that of the TLC27LxA variant. Their cost effectiveness makes them a good alternative to the TLC/V225x, where offset and noise are not of premium importance.

The TLV27L1/2 are available in the commercial temperature range to enable easy migration from the equivalent TLC27Lx. The TLV27L1 is not available with the power saving/performance boosting programmable pin 8.

The TLV27L1 is available in the small SOT-23 package —something the TLC27(L)1 was not—enabling performance boosting in a smaller package. The TLV27L2 is available in the 3mm x 5mm MSOP, providing PCB area savings over the 8-pin SOIC and 8-pin TSSOP.

SELECTION GUIDE

DEVICE	V_S [V]	I_Q/ch [µA]	V_{ICR} [V]	V_{IO} [mV]	I_{IB} [pA]	GBW [MHz]	SLEW RATE [V/µs]	V_n, 1 kHz [nV/√Hz]
TLV27Lx	2.7 to 16	11	−0.2 to V_S+1.2	5	60	0.18	0.06	89
TLV238x	2.7 to 16	10	−0.2 to V_S−0.2	4.5	60	0.18	0.06	90
TLC27Lx	4 to 16	17	−0.2 to V_S−1.5	10/5/2	60	0.085	0.03	68
OPAx349	1.8 to 5.5	2	−0.2 to V_S+0.2	10	10	0.070	0.02	300
OPAx347	2.3 to 5.5	34	−0.2 to V_S+0.2	6	10	0.35	0.01	60
TLC225x	2.7 to 16	62.5	0 to V_S−1.5	1.5/0.85	60	0.200	0.02	19

NOTE: All dc specs are maximums while ac specs are typicals.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE CODE	SYMBOL	SPECIFIED TEMPERATURE RANGE	ORDER NUMBER	TRANSPORT MEDIA
TLV27L1CD	SOIC-8	D	27V1C	0°C to 70°C	TLV27L1CD	Tube
					TLV27L1CDR	Tape and Reel
TLV27L1CDBV	SOT-23	DBV	VBIC		TLV27L1CDBVR	Tape and Reel
					TLV27L1CDBVT	
TLV27L1ID	SOIC-8	D	27V1I	−40°C to 125°C	TLV27L1ID	Tube
					TLV27L1IDR	Tape and Reel
TLV27L1IDBV	SOT-23	DBV	VBII		TLV27L1IDBVR	Tape and Reel
					TLV27L1IDBVT	
TLV27L2CD	SOIC-8	D	27V2C	0°C to 70°C	TLV27L2CD	Tube
					TLV27L2CDR	Tape and Reel
TLV27L2ID	SOIC-8	D	27V2I	−40°C to 125°C	TLV27L2ID	Tube
					TLV27L2IDR	Tape and Reel

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_S . . . . 16.5 V
Input voltage, V_I (see Note 1) . . . . V_S
Output current, I_O . . . . 100 mA
Differential input voltage, V_{ID} . . . . V_S
Continuous total power dissipation . . . . See Dissipation Rating Table
Maximum junction temperature, T_J . . . . 150°C
Operating free-air temperature range, T_A: C suffix . . . . 0°C to 70°C
I suffix . . . . –40°C to 125°C
Storage temperature range, T_{stg} . . . . –65°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Relative to GND pin.

DISSIPATION RATING TABLE

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	$T_A \leq 25°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D (8)	38.3	176	710 mW	370 mW
DBV (5)	55	324.1	385 mW	201 mW
DBV (6)	55	294.3	425 mW	221 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, (V_S)	Dual supply	±1.35	±8	V
	Single supply	2.7	16	
Input common-mode voltage range		−0.2	V_S−1.2	V
Operating free-air temperature, T_A	C-suffix	0	70	°C
	I-suffix	−40	125	

electrical characteristics at recommended operating conditions, V_S = 2.7 V, 5 V, and 10 V (unless otherwise noted)

dc performance

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_S/2$, $V_O = V_S/2$, R_L = 100 kΩ, R_S = 50 Ω		25°C		0.5	5	mV
				Full range			7	
α_{VIO}	Offset voltage drift			25°C		1.1		µV/°C
CMRR	Common-mode rejection ratio	V_{IC} = 0 V to V_S−1.2 V, R_S = 50 Ω		25°C	71	86		dB
				Full range	70			
A_{VD}	Large-signal differential voltage amplification	$V_{O(PP)} = V_S/2$, R_L = 100 kΩ	V_S = 2.7 V, 5 V	25°C	80	100		dB
				Full range	77			
			V_S = ±5 V	25°C	77	82		
				Full range	74			

† Full range is −40°C to 125°C for I suffix.

input characteristics

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
I_{IO}	Input offset current	$V_{IC} = V_S/2$, $V_O = V_S/2$, R_L = 100 kΩ, R_S = 50 Ω	≤25°C		1	60	pA
			≤70°C			100	
			≤125°C			1000	
I_{IB}	Input bias current		≤25°C		1	60	pA
			≤70°C			200	
			≤125°C			1000	
$r_{i(d)}$	Differential input resistance		25°C		1000		GΩ
C_{IC}	Common-mode input capacitance	f = 1 kHz	25°C		8		pF

power supply

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
I_Q	Quiescent current (per channel)	$V_O = V_S/2$	25°C		7	11	µA
			Full range			16	
PSRR	Power supply rejection ratio ($\Delta V_S/\Delta V_{IO}$)	V_S = 2.7 V to 16 V, No load, $V_{IC} = V_S/2$ V	25°C	74	82		dB
			Full range	70			

† Full range is −40°C to 125°C for I suffix.

electrical characteristics at recommended operating conditions, V_S = 2.7 V, 5 V, and ±5 V (unless otherwise noted) (continued)

output characteristics

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_O	Output voltage swing from rail	$V_{IC} = V_S/2$, I_{OL} = 100 µA	V_S = 2.7 V	25°C		160	200	mV
				Full range			220	
			V_S = 5 V	25°C		85	120	
				Full range			200	
			V_S = ±5 V	25°C		50	120	
				Full range			150	
		$V_{IC} = V_S/2$, I_{OL} = 500 µA	V_S = 5 V	25°C		420	800	
				Full range			900	
			V_S = ±5 V	25°C		200	400	
				Full range			500	
I_O	Output current	V_O = 0.5 V from rail	V_S = 2.7 V	25°C		400		µA

† Full range is −40°C to 125°C for I suffix.

dynamic performance

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
GBP	Gain bandwidth product	R_L = 100 kΩ, C_L = 10 pF, f = 1 kHz		25°C		160		kHz
SR	Slew rate at unity gain	$V_{O(pp)}$ = 1 V, R_L = 100 kΩ, C_L = 50 pF		25°C		0.06		V/µs
				−40°C		0.05		
				125°C		0.8		
ϕ_M	Phase margin	R_L = 100 kΩ, C_L = 50 pF		25°C		62		°
t_s	Settling time (0.1%)	$V_{(STEP)pp}$ = 1 V, A_V = −1, C_L = 50 pF, R_L = 100 kΩ	Rise	25°C		62		µs
			Fall			44		

noise/distortion performance

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_n	Equivalent input noise voltage	f = 1 kHz	25°C		89		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.6		fA/√Hz

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	vs Common-mode input voltage	1, 2, 3
I_{IB}/I_{IO}	Input bias and offset current	vs Free-air temperature	4
V_{OH}	High-level output voltage	vs High-level output current	5, 7, 9
V_{OL}	Low-level output voltage	vs Low-level output current	6, 8, 10
I_Q	Quiescent current	vs Supply voltage	11
		vs Free-air temperature	12
	Supply voltage and supply current ramp up		13
A_{VD}	Differential voltage gain and phase shift	vs Frequency	14
GBP	Gain-bandwidth product	vs Free-air temperature	15
ϕ_m	Phase margin	vs Load capacitance	16
CMRR	Common-mode rejection ratio	vs Frequency	17
PSRR	Power supply rejection ratio	vs Frequency	18
	Input referred noise voltage	vs Frequency	19
SR	Slew rate	vs Free-air temperature	20
$V_{O(PP)}$	Peak-to-peak output voltage	vs Frequency	21
	Inverting small-signal response		22
	Inverting large-signal response		23
	Crosstalk	vs Frequency	24

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

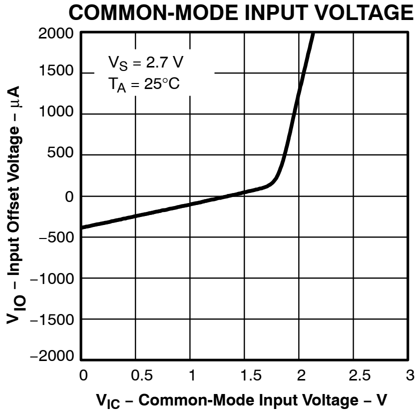


Figure 1

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

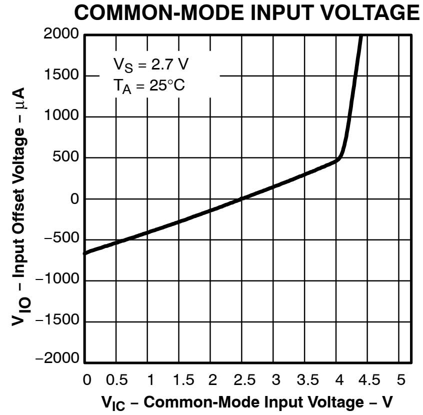


Figure 2

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

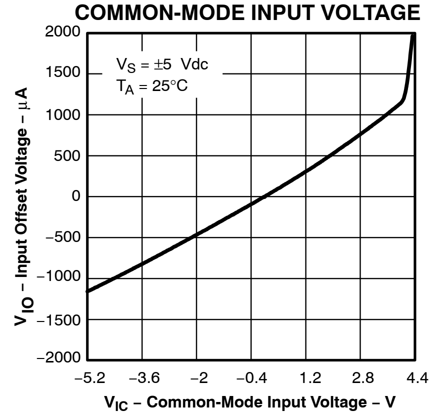


Figure 3

TYPICAL CHARACTERISTICS

INPUT BIAS AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

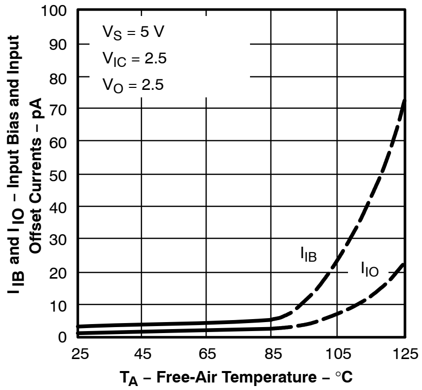


Figure 4

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

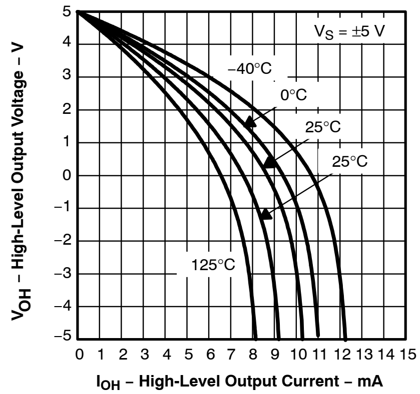


Figure 5

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

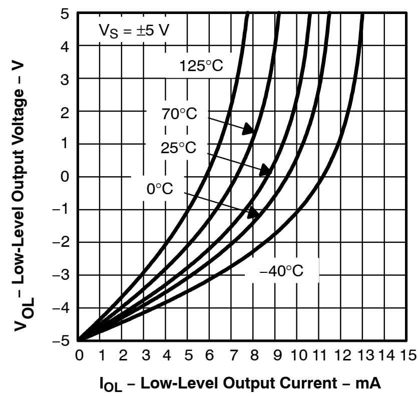


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

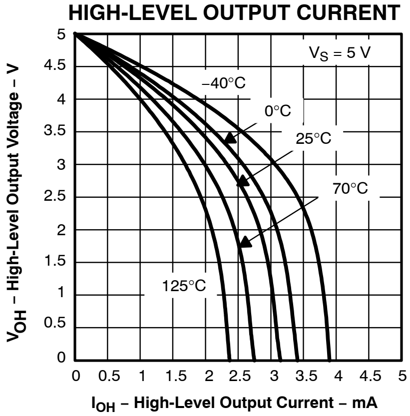


Figure 7

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

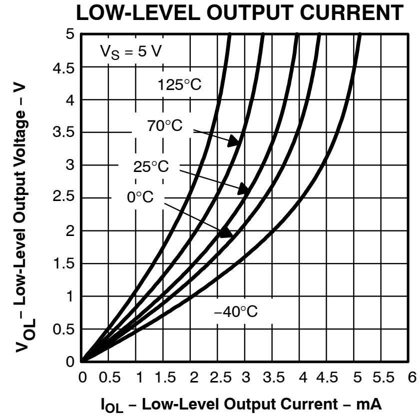


Figure 8

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

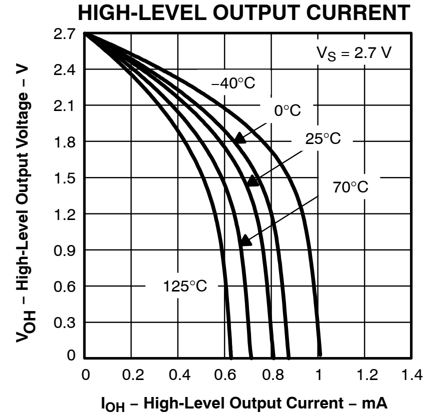


Figure 9

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

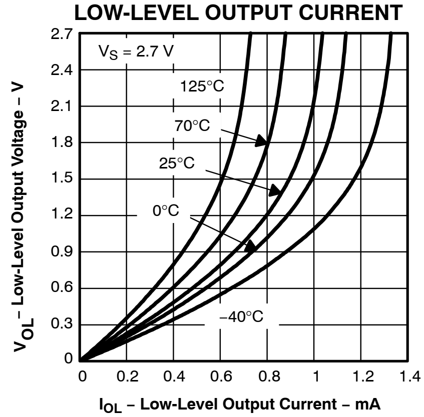


Figure 10

QUIESCENT CURRENT vs SUPPLY VOLTAGE

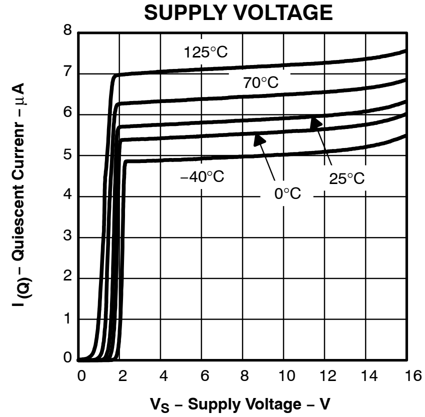


Figure 11

QUIESCENT CURRENT vs FREE-AIR TEMPERATURE

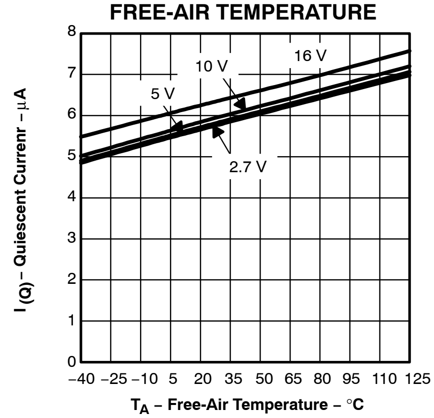


Figure 12

TYPICAL CHARACTERISTICS

SUPPLY VOLTAGE AND SUPPLY CURRENT RAMP UP

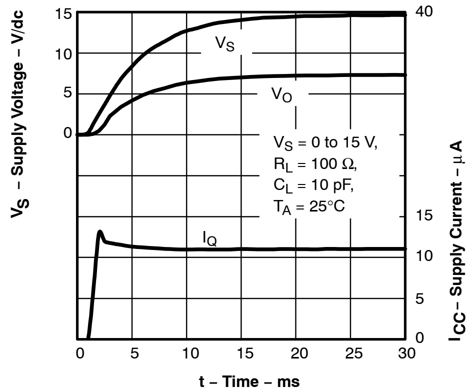


Figure 13

DIFFERENTIAL VOLTAGE GAIN AND PHASE SHIFT vs FREQUENCY

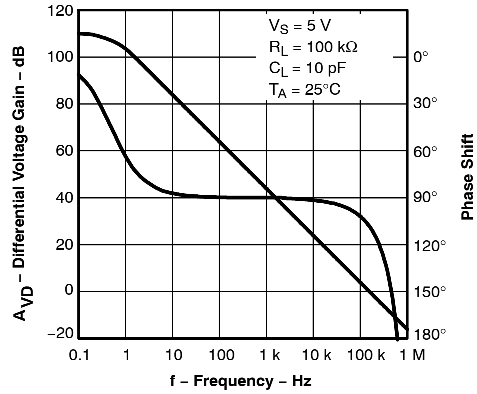


Figure 14

GAIN-BANDWIDTH PRODUCT vs FREE-AIR TEMPERATURE

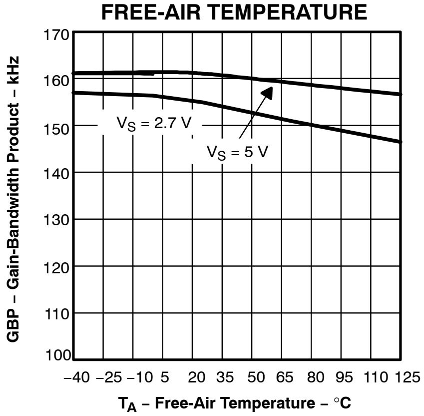


Figure 15

PHASE MARGIN vs LOAD CAPACITANCE

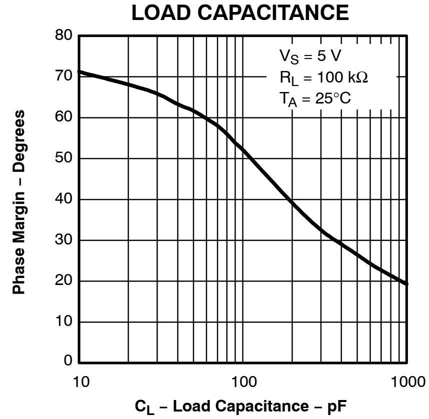


Figure 16

COMMON-MODE REJECTION RATIO vs FREQUENCY

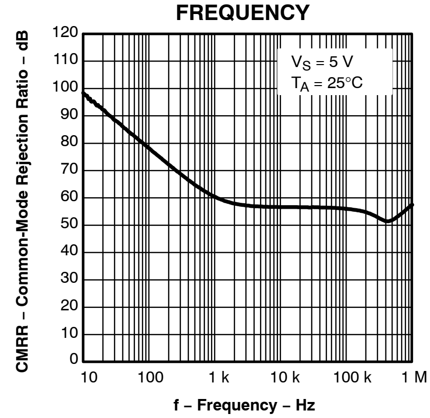


Figure 17

POWER SUPPLY REJECTION RATIO vs FREQUENCY

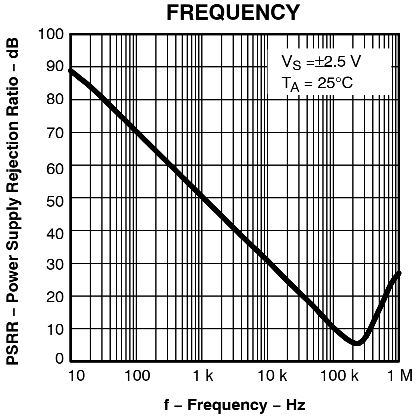


Figure 18

INPUT REFERRED NOISE VOLTAGE vs FREQUENCY

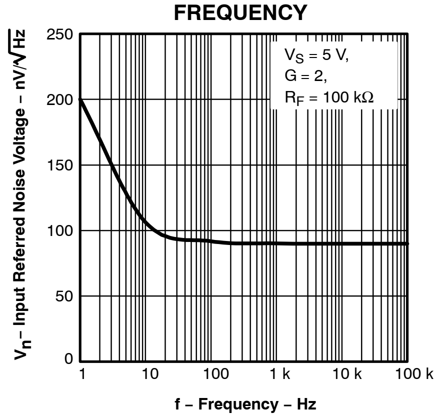


Figure 19

SLEW RATE vs FREE-AIR TEMPERATURE

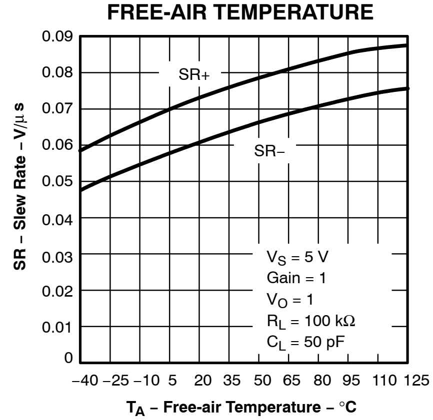


Figure 20

TYPICAL CHARACTERISTICS

PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

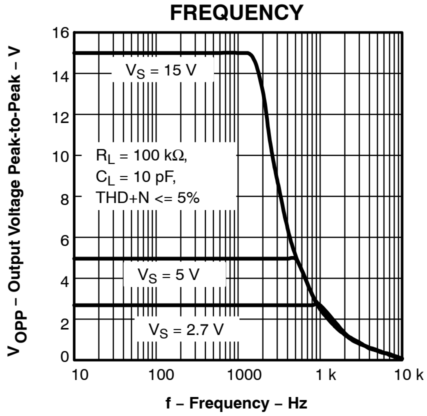


Figure 21

INVERTING SMALL-SIGNAL RESPONSE

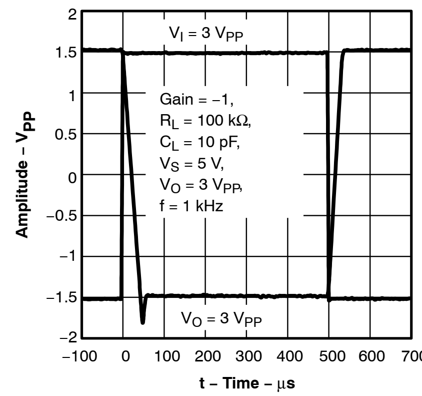


Figure 22

INVERTING LARGE-SIGNAL RESPONSE

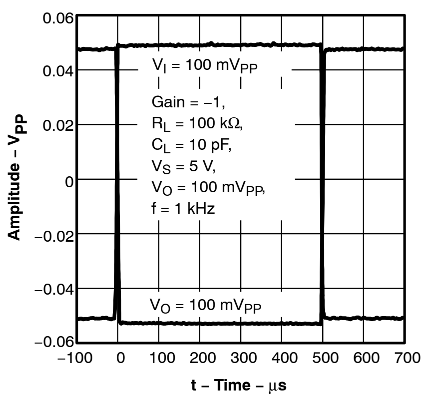


Figure 23

CROSSTALK vs FREQUENCY

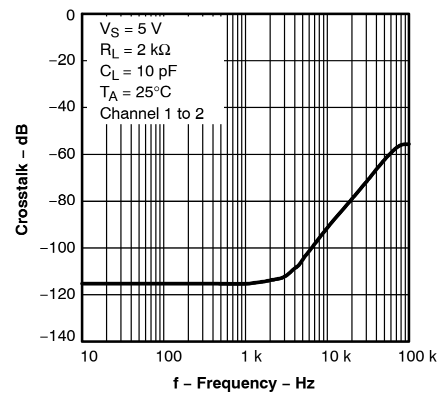
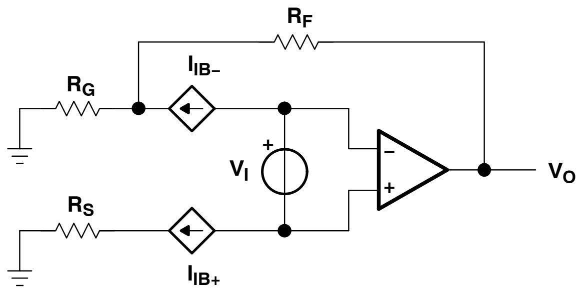


Figure 24

APPLICATION INFORMATION

offset voltage

The output offset voltage (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:

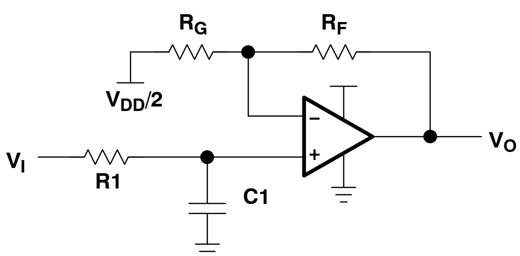


$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+}\, R_S \left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-}\, R_F$$

Figure 25. Output Offset Voltage Model

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 26).

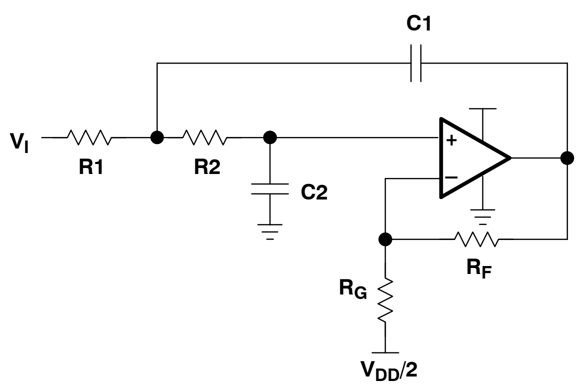


$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR1C1}\right)$$

$$f_{-3dB} = \frac{1}{2\pi R1C1}$$

Figure 26. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.



R1 = R2 = R
C1 = C2 = C
Q = Peaking Factor
(Butterworth Q = 0.707)

$$f_{-3dB} = \frac{1}{2\pi RC}$$

$$R_G = \frac{R_F}{\left(2 - \frac{1}{Q}\right)}$$

Figure 27. 2-Pole Low-Pass Sallen-Key Filter

APPLICATION INFORMATION

circuit layout considerations

To achieve the levels of high performance of the TLV27Lx, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- Ground planes—It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling—Use a 6.8-µF tantalum capacitor in parallel with a 0.1-µF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-µF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-µF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets—Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements—Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components—Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

APPLICATION INFORMATION

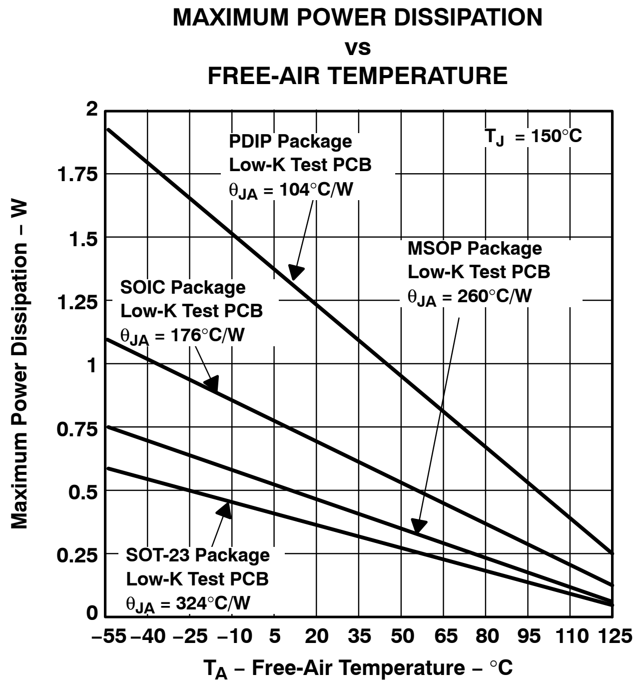
general power dissipation considerations

For a given θ_{JA}, the maximum power dissipation is shown in Figure 28 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}}\right)$$

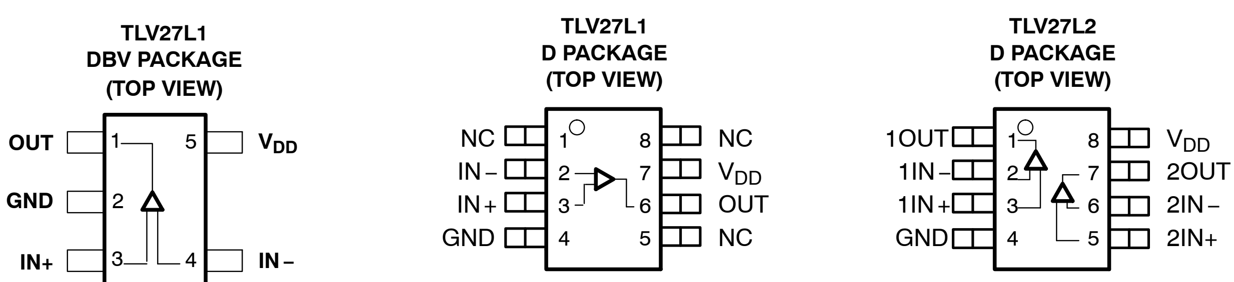
Where:

P_D = Maximum power dissipation of TLV27Lx IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
θ_{JA} = $\theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case
θ_{CA} = Thermal coefficient from case to ambient air (°C/W)



NOTE A: Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 28. Maximum Power Dissipation vs Free-Air Temperature



NC − No internal connection

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV27L1CD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	27V1C
TLV27L1CDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	VBIC
TLV27L1CDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	VBIC
TLV27L1CDBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	VBIC
TLV27L1CDBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	VBIC
TLV27L1ID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	27V1I
TLV27L1IDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	VBII
TLV27L1IDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	VBII
TLV27L1IDBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TLV27L1IDBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	VBII
TLV27L1IDBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	VBII
TLV27L1IDBVTG4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	-	Call TI	Call TI	-40 to 125	
TLV27L1IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27V1I
TLV27L1IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27V1I
TLV27L2CDGK	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-	BAC
TLV27L2CDGK.A	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BAC
TLV27L2CDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-	BAC
TLV27L2CDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BAC
TLV27L2CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	27V2C
TLV27L2CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	27V2C
TLV27L2ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27V2I
TLV27L2ID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27V2I
TLV27L2IDGK	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-	BAD
TLV27L2IDGK.A	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BAD
TLV27L2IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-	BAD
TLV27L2IDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BAD
TLV27L2IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27V2I
TLV27L2IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27V2I

[1] **Status:** For more details on status, see our product life cycle.

[2] **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

[3] **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV27L2 :

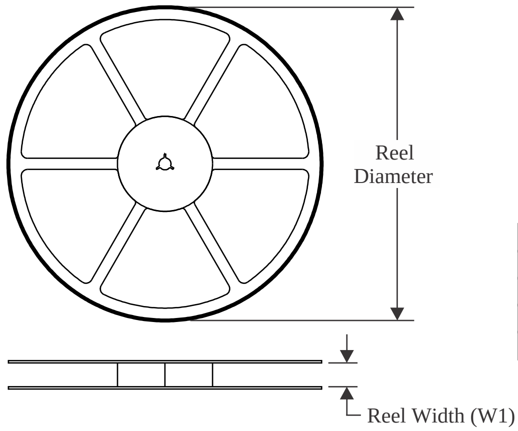
- Automotive : TLV27L2-Q1

NOTE: Qualified Version Definitions:

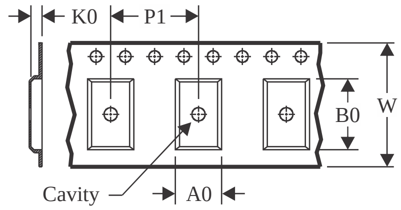
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

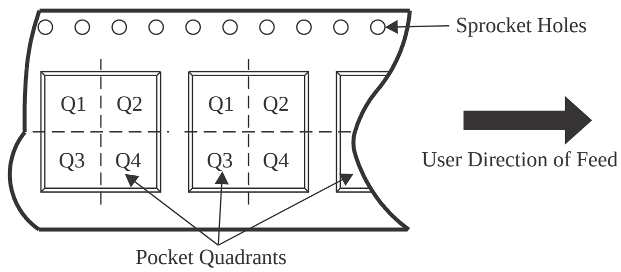


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

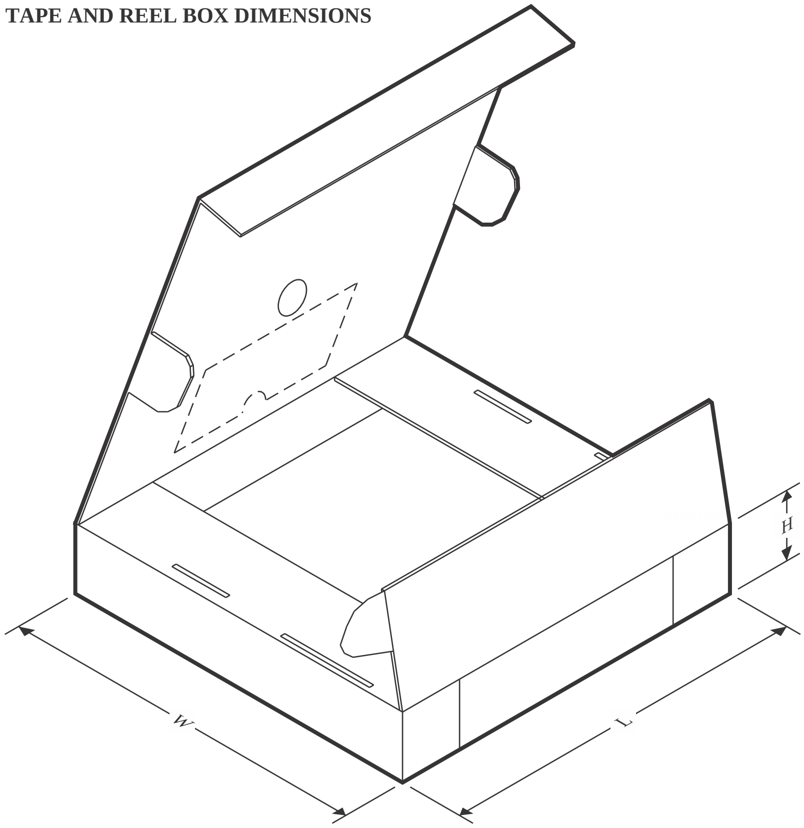
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV27L1CDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV27L1CDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV27L1IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV27L1IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV27L1IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV27L2CDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV27L2CDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV27L2CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV27L2IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV27L2IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV27L2IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

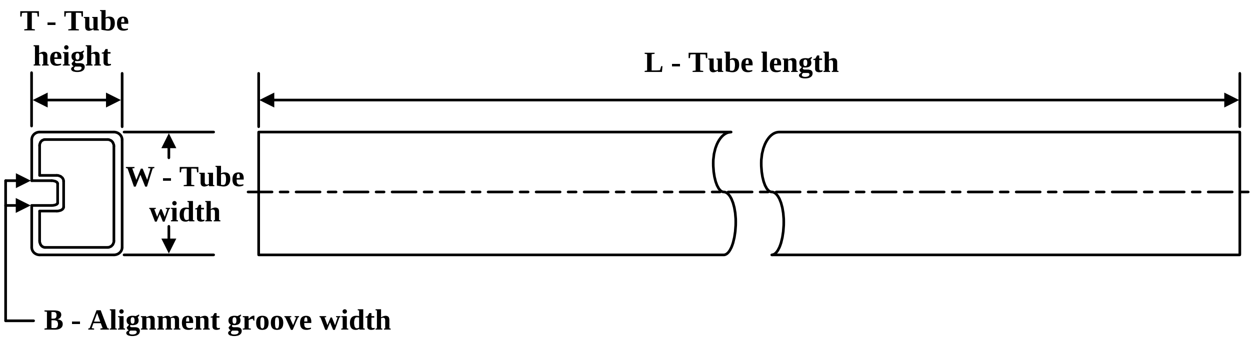
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

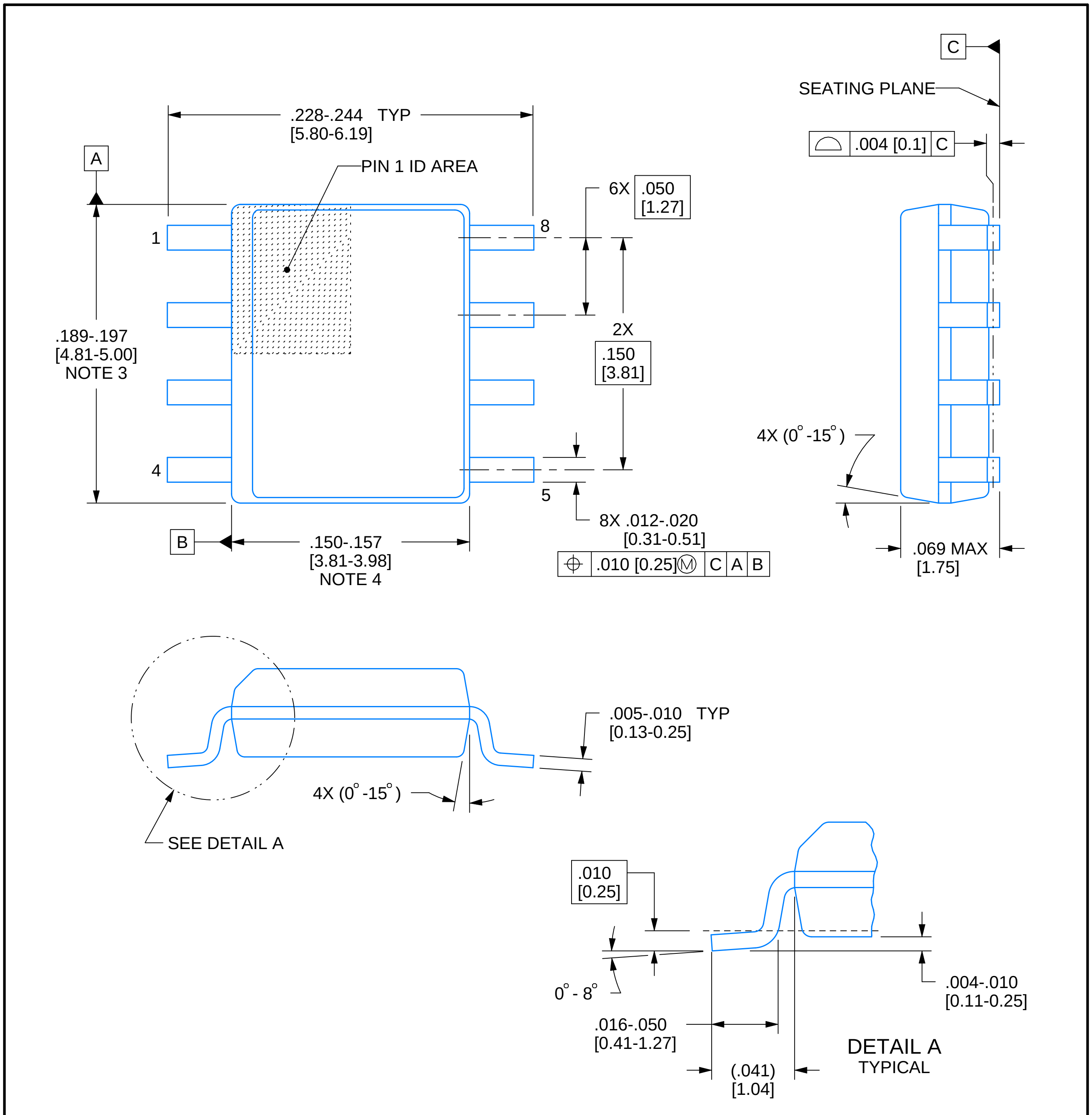
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV27L1CDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV27L1CDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV27L1IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV27L1IDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV27L1IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLV27L2CDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TLV27L2CDGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
TLV27L2CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV27L2IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TLV27L2IDGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
TLV27L2IDR	SOIC	D	8	2500	340.5	338.1	20.6

TUBE



*All dimensions are nominal

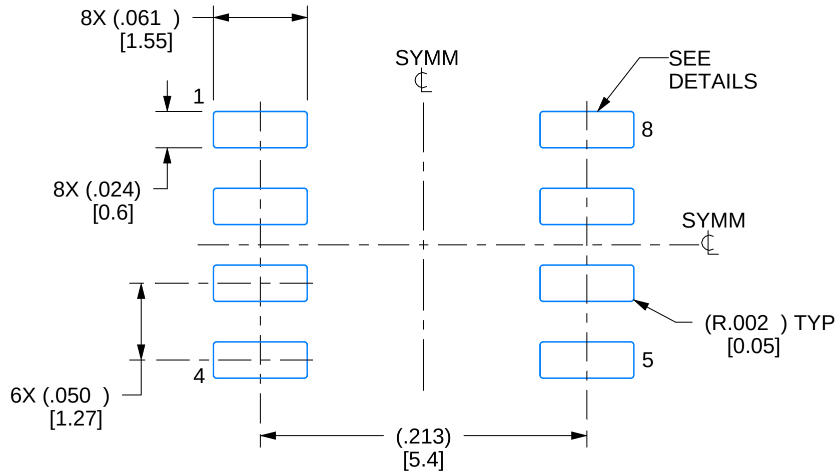
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV27L2CDGK	DGK	VSSOP	8	80	330	6.55	500	2.88
TLV27L2CDGK.A	DGK	VSSOP	8	80	330	6.55	500	2.88
TLV27L2ID	D	SOIC	8	75	507	8	3940	4.32
TLV27L2ID.A	D	SOIC	8	75	507	8	3940	4.32
TLV27L2IDGK	DGK	VSSOP	8	80	330	6.55	500	2.88
TLV27L2IDGK.A	DGK	VSSOP	8	80	330	6.55	500	2.88



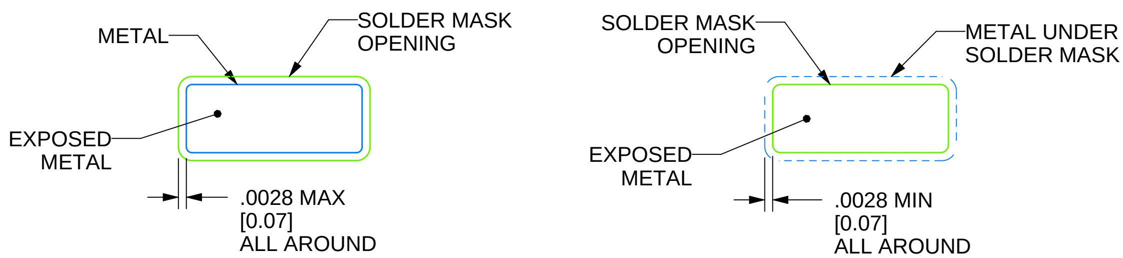
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

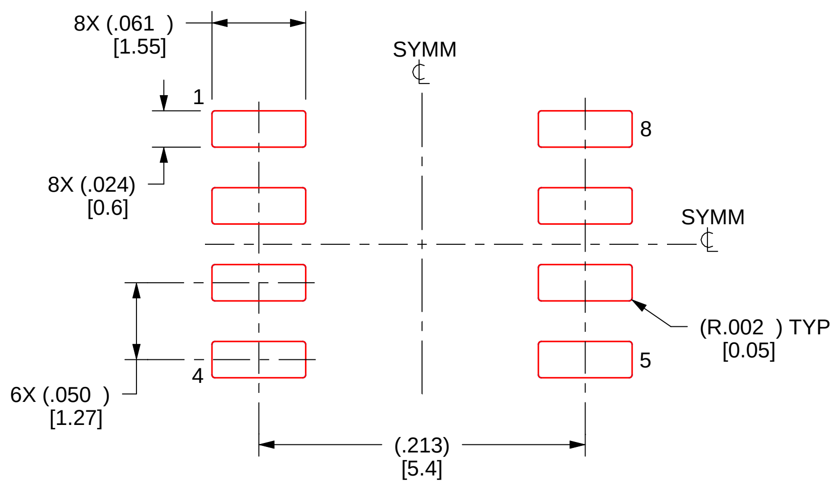
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

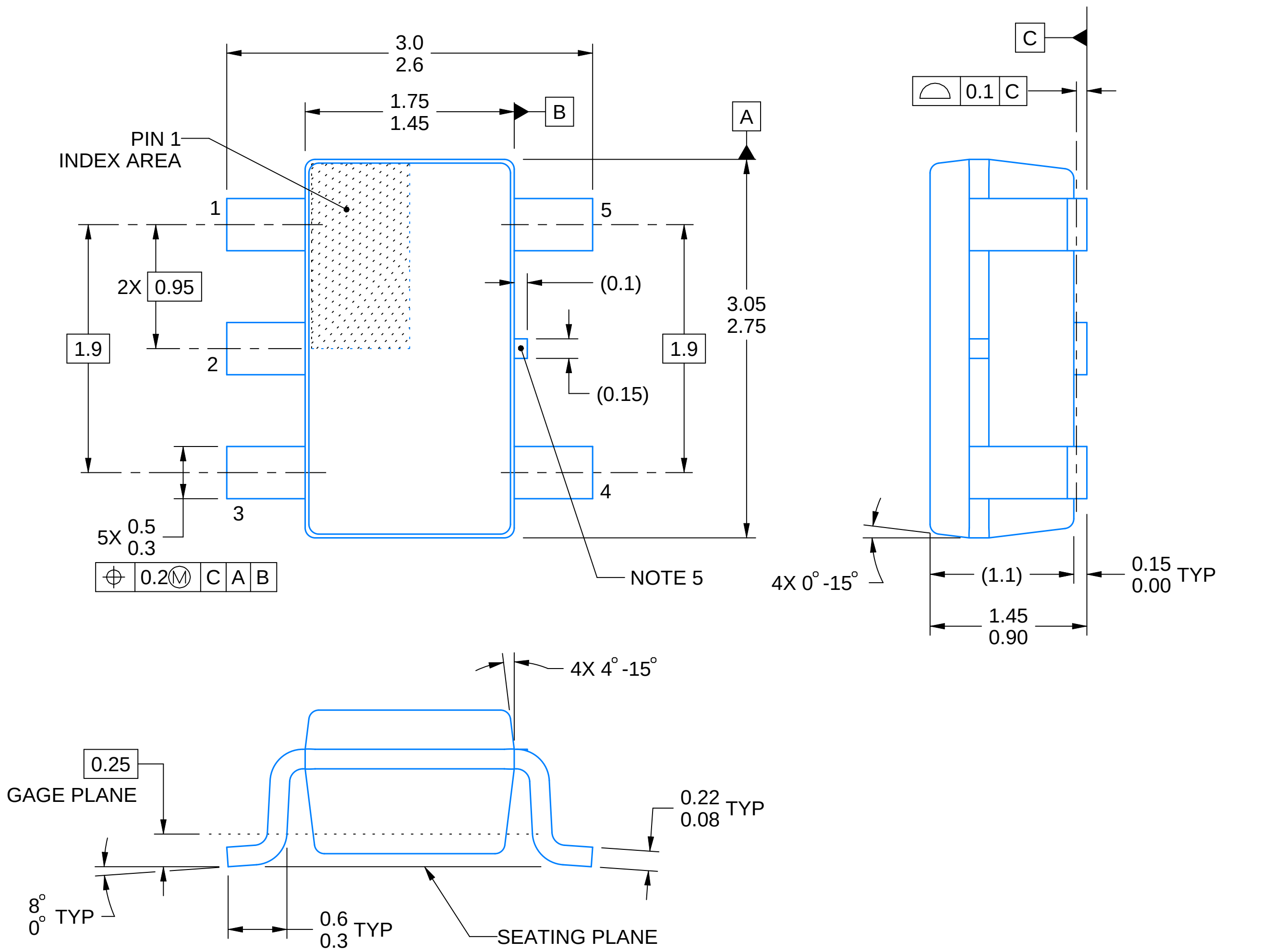


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

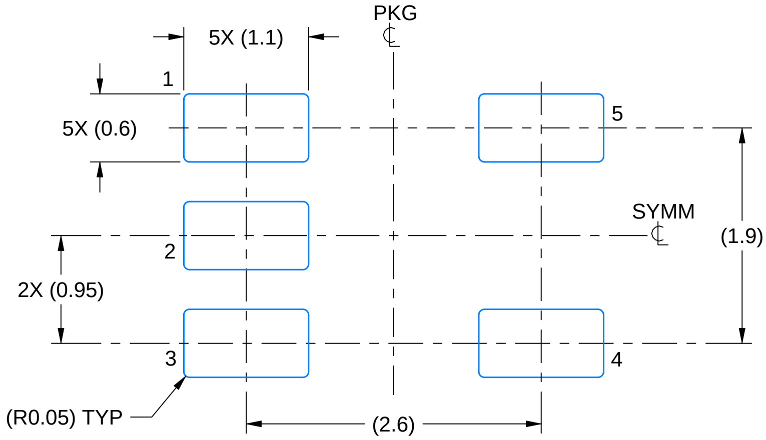
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



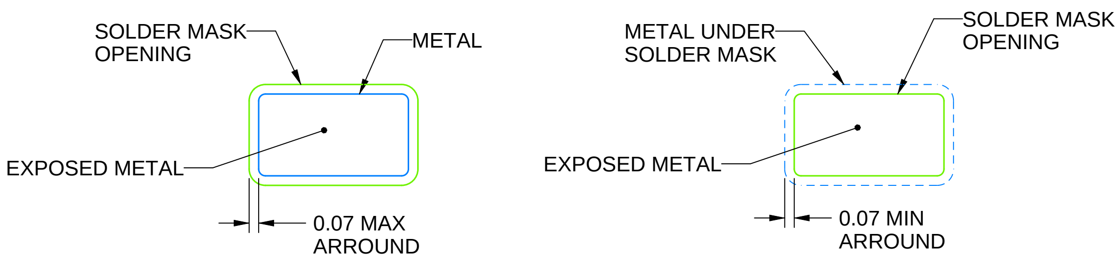
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK DEFINED (PREFERRED)

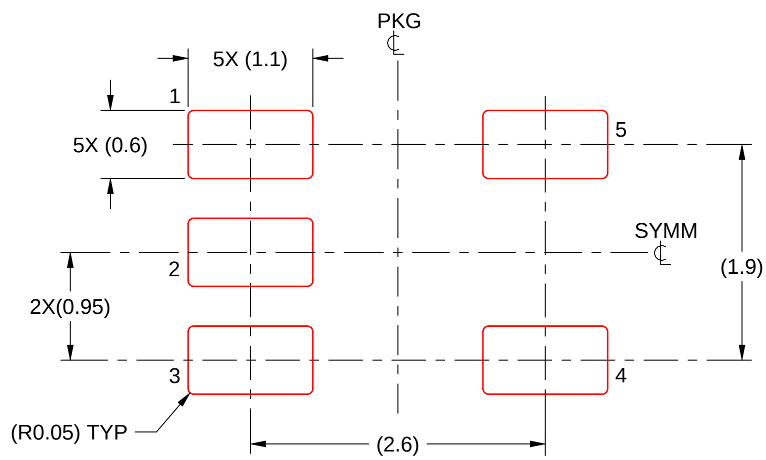
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

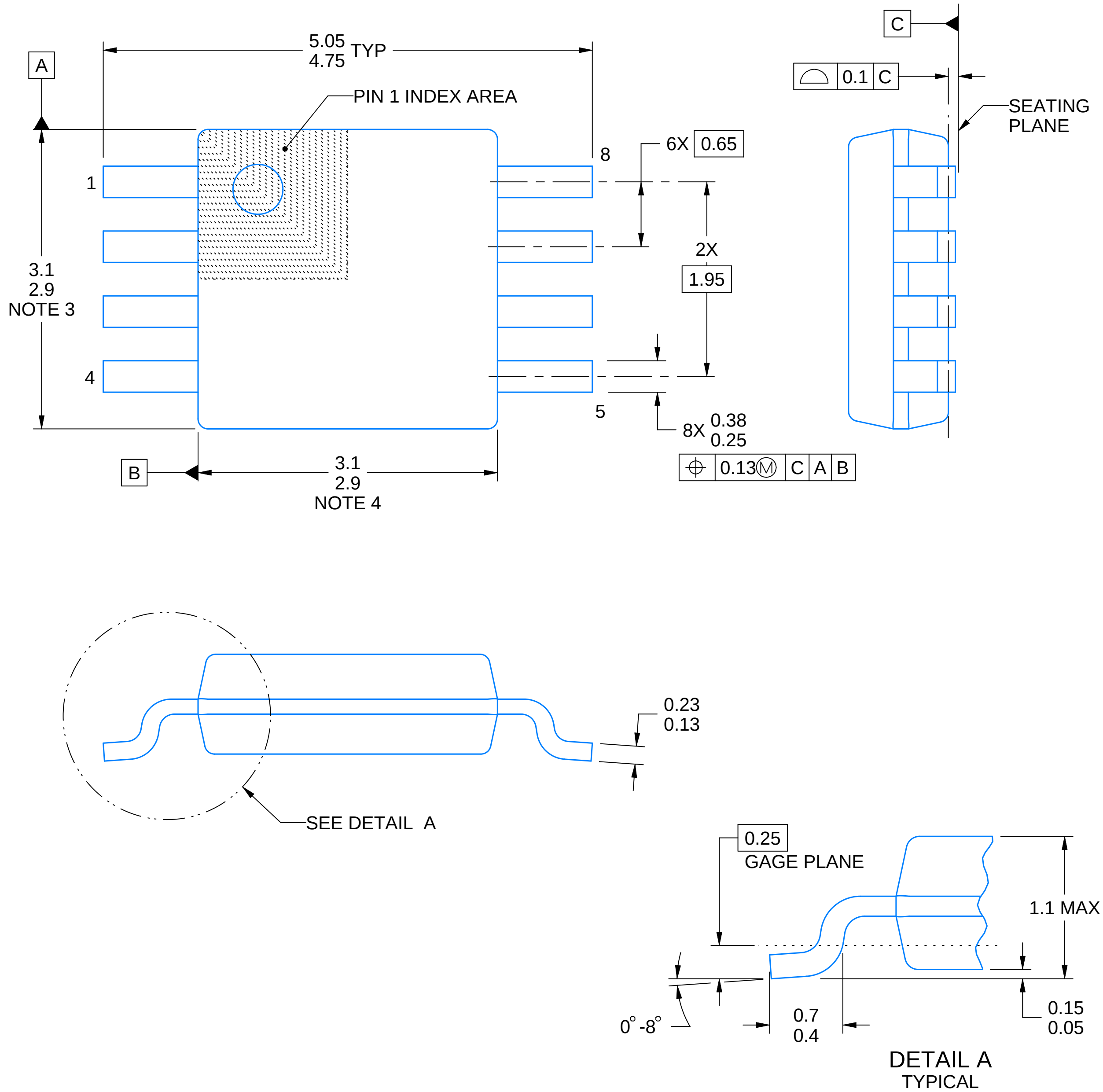


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4214862/A 04/2023

PowerPAD is a trademark of Texas Instruments.

NOTES:

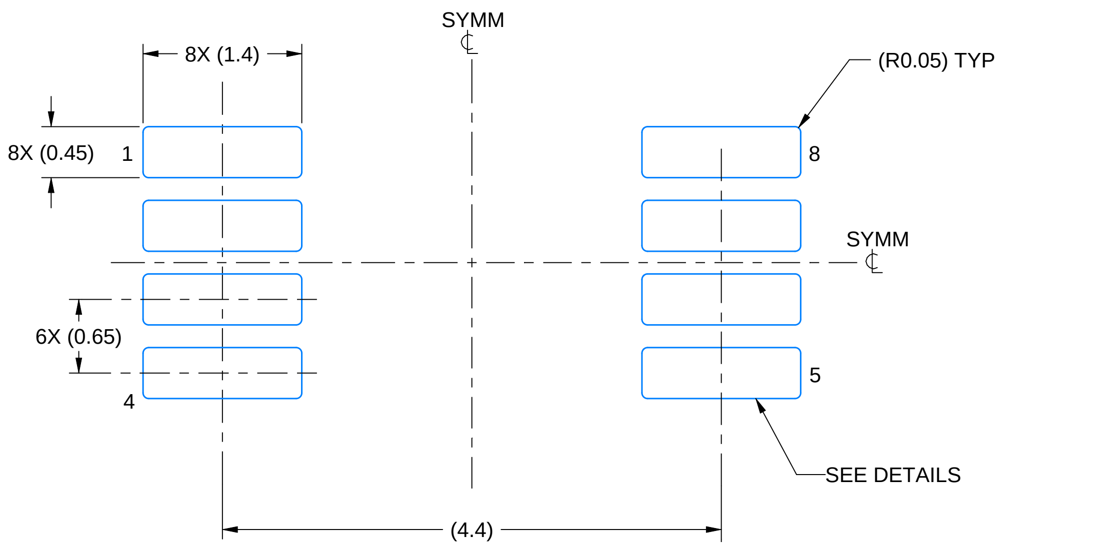
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

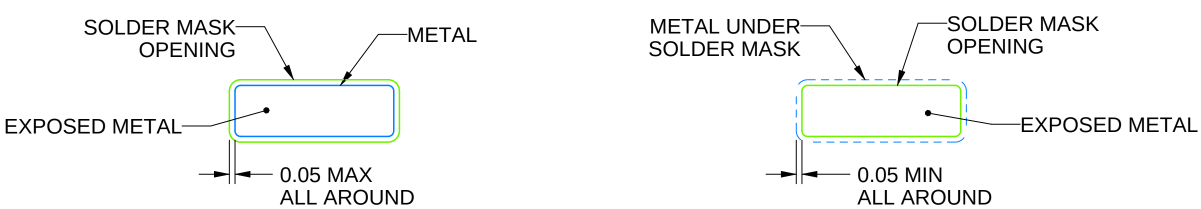
DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON-SOLDER MASK DEFINED (PREFERRED)

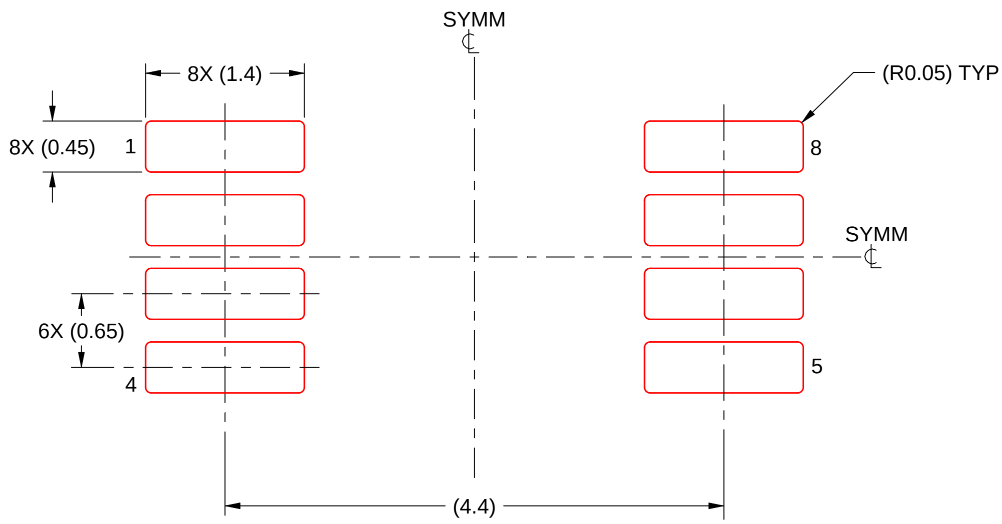
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265