

FQP6N80C/FQPF6N80C

800V N-Channel MOSFET

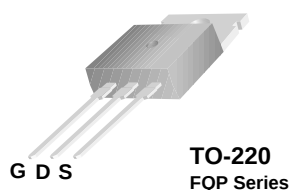
General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supplies.

Features

- 5.5A, 800V, $R_{DS(on)} = 2.5\Omega$ @ $V_{GS} = 10V$
- Low gate charge (typical 21 nC)
- Low C_{rss} (typical 8 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FQP6N80C	FQPF6N80C	Units
V_{DSS}	Drain-Source Voltage	800		V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	5.5	5.5 *	A
	- Continuous ($T_C = 100^\circ\text{C}$)	3.2	3.2 *	A
I_{DM}	Drain Current - Pulsed (Note 1)	22	22 *	A
V_{GSS}	Gate-Source Voltage	± 30		V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	680		mJ
I_{AR}	Avalanche Current (Note 1)	5.5		A
E_{AR}	Repetitive Avalanche Energy (Note 1)	15.8		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5		V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$)	158	51	W
	- Derate above 25°C	1.27	0.41	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150		$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		$^\circ\text{C}$

* Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	FQP6N80C	FQPF6N80C	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.79	2.45	$^\circ\text{C/W}$
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink Typ.	0.5	--	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	62.5	$^\circ\text{C/W}$

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	800	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C	--	0.97	--	V/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 800\text{ V}, V_{GS} = 0\text{ V}$	--	--	10	μA
		$V_{DS} = 640\text{ V}, T_C = 125^\circ\text{C}$	--	--	100	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 2.75\text{ A}$	--	2.1	2.5	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 50\text{ V}, I_D = 2.75\text{ A}$ (Note 4)	--	5.4	--	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	1010	1310	pF
C_{oss}	Output Capacitance		--	90	115	pF
C_{rss}	Reverse Transfer Capacitance		--	8	11	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 400\text{ V}, I_D = 5.5\text{ A},$ $R_G = 25\text{ }\Omega$ (Note 4, 5)	--	26	60	ns
t_r	Turn-On Rise Time		--	65	140	ns
$t_{d(off)}$	Turn-Off Delay Time		--	47	105	ns
t_f	Turn-Off Fall Time		--	44	90	ns
Q_g	Total Gate Charge	$V_{DS} = 640\text{ V}, I_D = 5.5\text{ A},$ $V_{GS} = 10\text{ V}$ (Note 4, 5)	--	21	30	nC
Q_{gs}	Gate-Source Charge		--	6	--	nC
Q_{gd}	Gate-Drain Charge		--	9	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I _S	Maximum Continuous Drain-Source Diode Forward Current		--	--	5.5	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	22	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 5.5 A	--	--	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 5.5 A, dI _F / dt = 100 A/μs (Note 4)	--	615	--	ns
Q _{rr}	Reverse Recovery Charge		--	5.4	--	μC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 42\text{ mH}$, $I_{AS} = 5.5\text{ A}$, $V_{DD} = 50\text{ V}$, $R_G = 25\text{ }\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 5.5\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature

Typical Characteristics

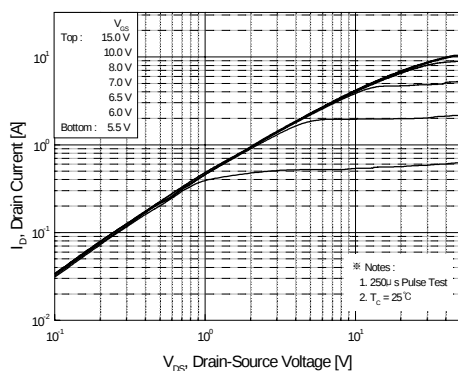


Figure 1. On-Region Characteristics

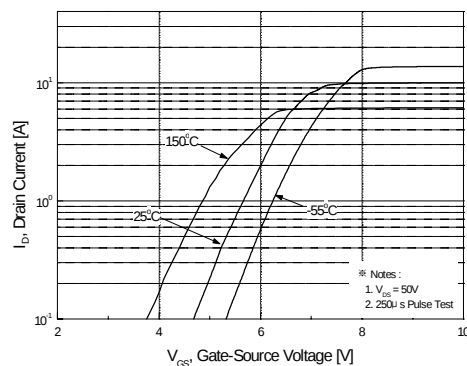


Figure 2. Transfer Characteristics

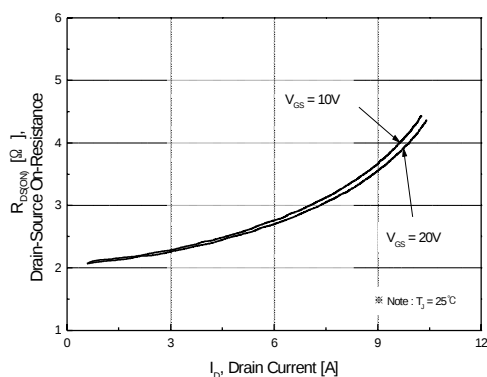


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

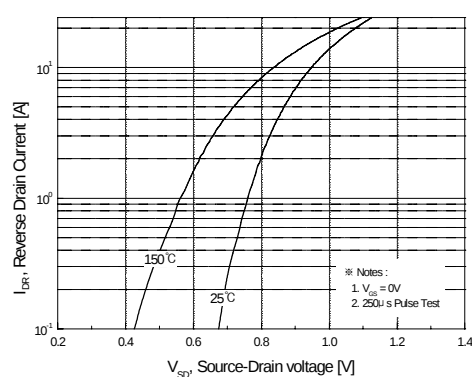


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

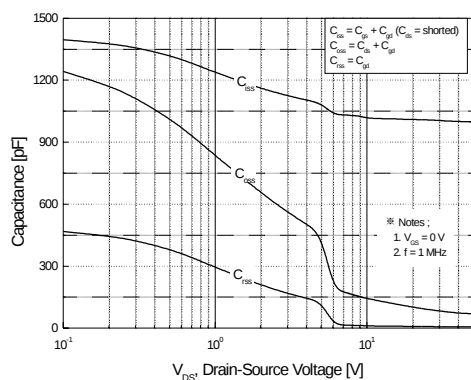


Figure 5. Capacitance Characteristics

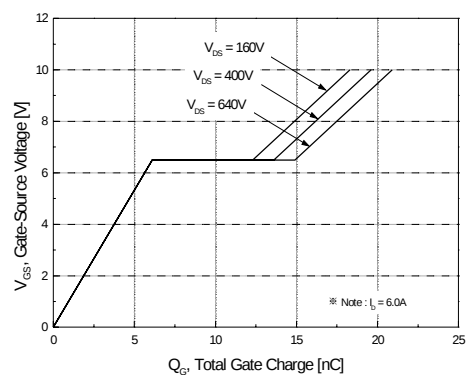


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

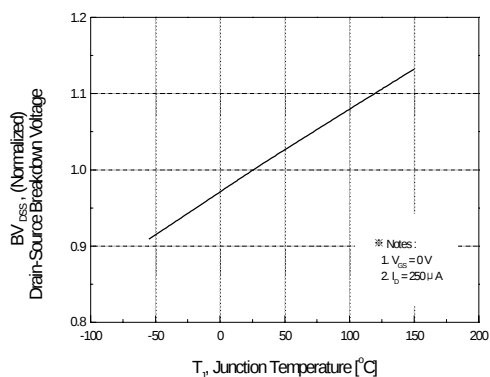


Figure 7. Breakdown Voltage Variation vs Temperature

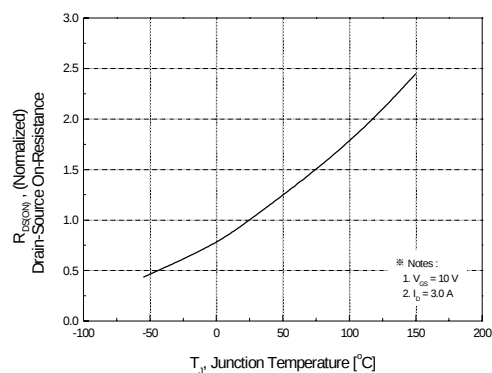


Figure 8. On-Resistance Variation vs Temperature

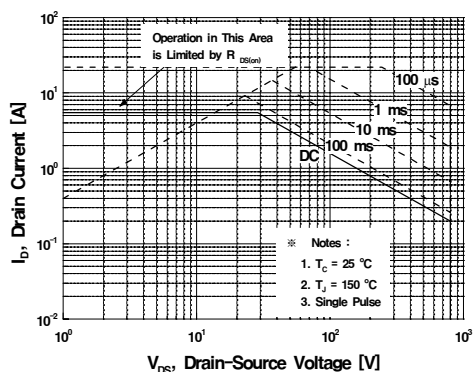


Figure 9-1. Maximum Safe Operating Area for FQP6N80C

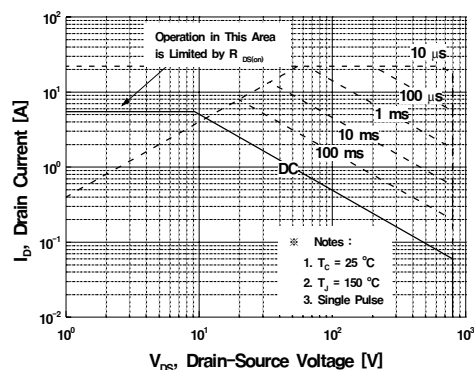


Figure 9-2. Maximum Safe Operating Area for FQPF6N80C

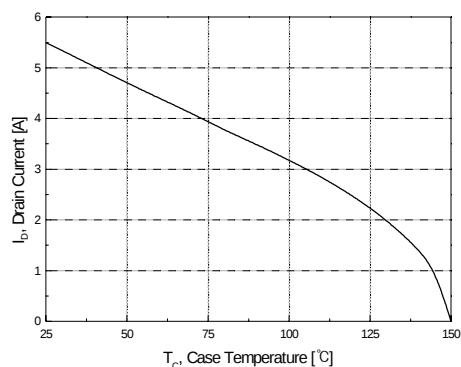


Figure 10. Maximum Drain Current vs Case Temperature

Typical Characteristics (Continued)

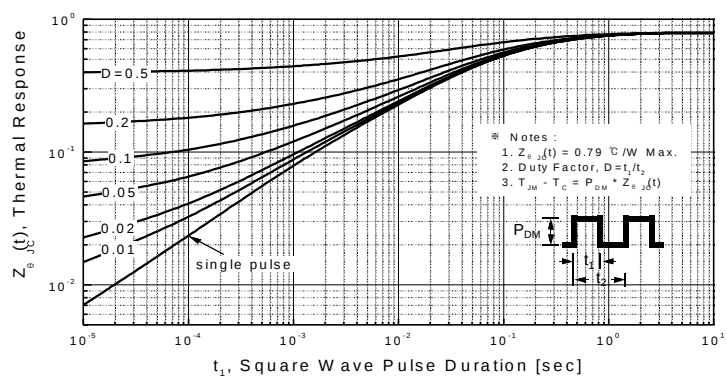


Figure 11-1. Transient Thermal Response Curve for FQP6N80C

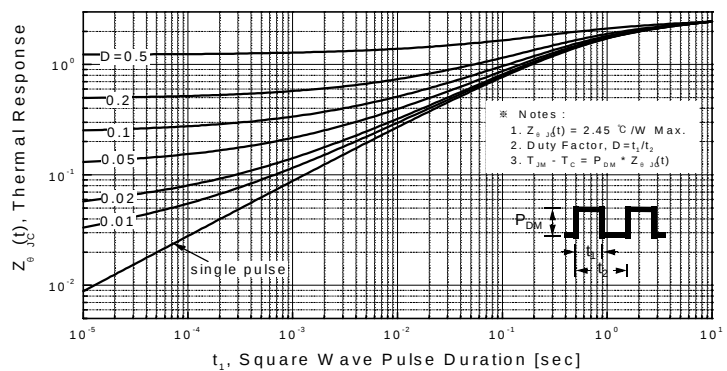


Figure 11-2. Transient Thermal Response Curve for FQPF6N80C

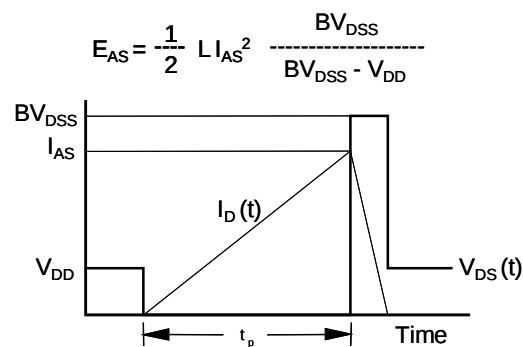
Gate Charge Test Circuit & Waveform



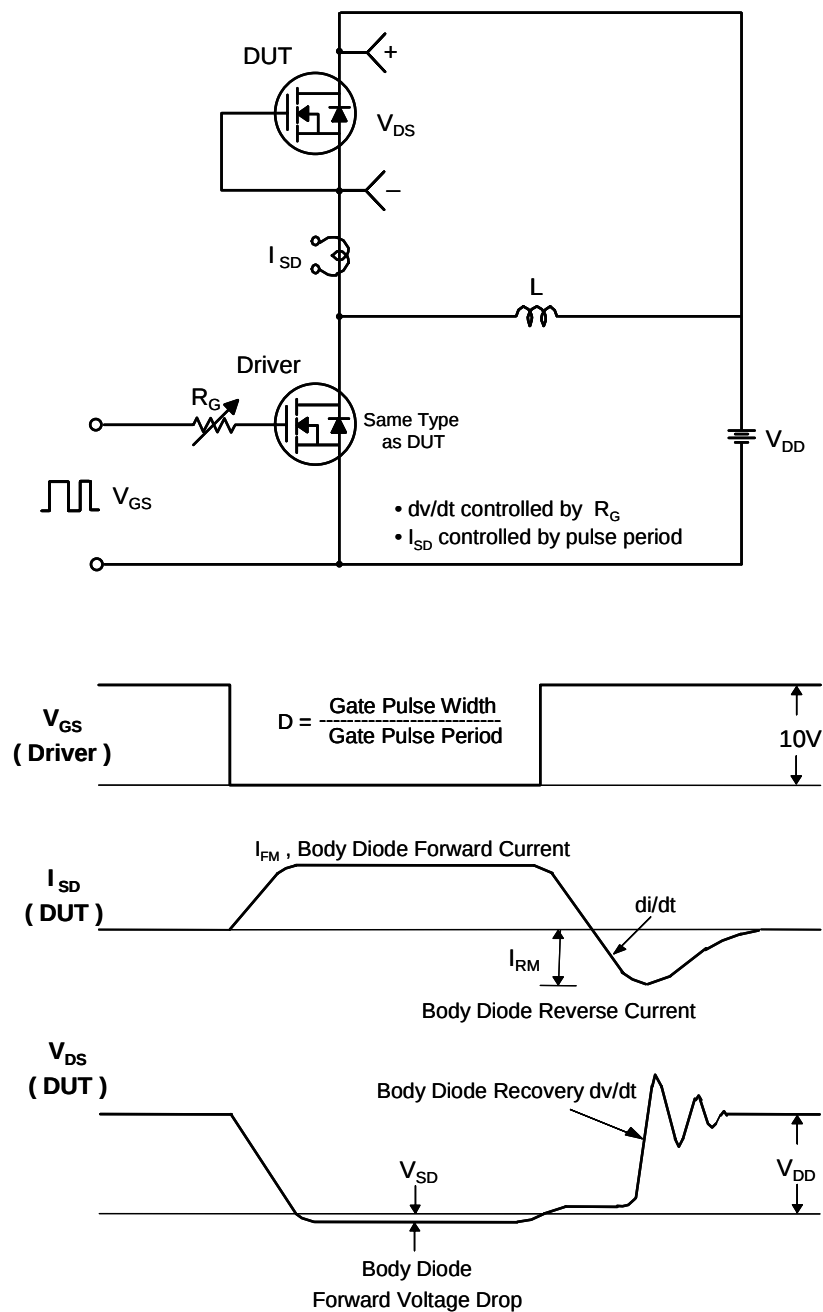
Resistive Switching Test Circuit & Waveforms



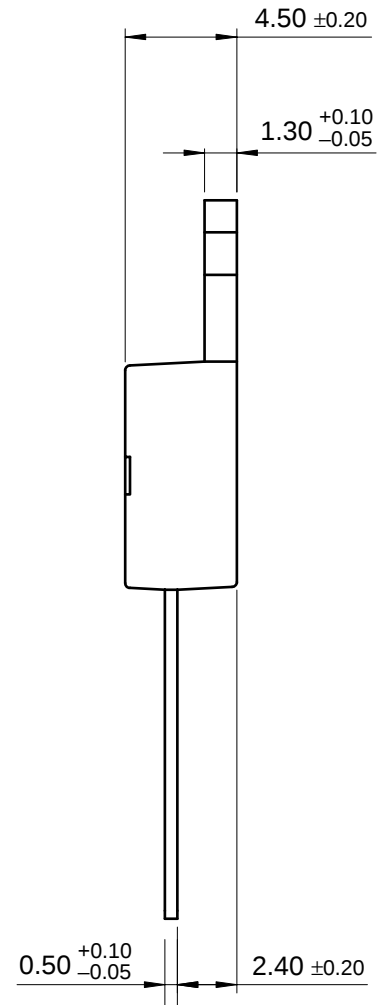
Unclamped Inductive Switching Test Circuit & Waveforms



Peak Diode Recovery dv/dt Test Circuit & Waveforms



TO-220



Rev. A, June 2003

Package Dimensions (Continued)

TO-220F



Dimensions in Millimeters

FQP6N80C/FQPF6N80C

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