

Features

- DC to 1500 MHz operation
- Fixed divide ratio of 4
- Low-power consumption: 8 mA typical @ 3V
- RF or LV Digital Interface
- Ultra-small package: 6-lead SC-70

Product Description

The PE3512 is a high-performance static UltraCMOS™ prescaler with a fixed divide ratio of 4. Its operating frequency range is DC to 1500 MHz. The PE3512 operates on a nominal 3 V supply and draws only 8 mA. The input and output interfaces support both AC-coupled, low-Z RF as well as direct connection to low voltage positive logic devices. It is packaged in a small 6-lead SC-70 and is ideal for frequency scaling solutions

The PE3512 is manufactured on Peregrine's UltraCMOS™ process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Schematic Diagram

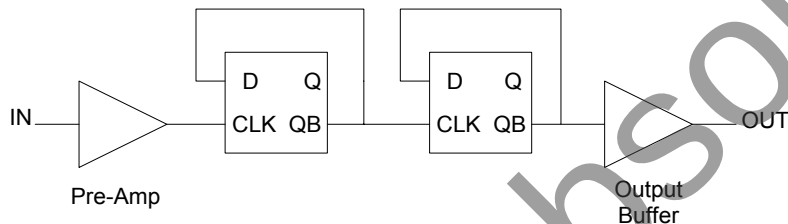


Figure 2. Package Type

6-lead SC70



Table 1. Electrical Specifications ($Z_S = Z_L = 50 \Omega$)

$V_{DD} = 3.0 \text{ V}$, $-40^\circ \text{ C} \leq T_A \leq 85^\circ \text{ C}$, unless otherwise specified

Parameter	Conditions	Minimum	Typical	Maximum	Units
Supply Voltage		2.85	3.0	3.15	V
Supply Current			8	12	mA
Input Frequency (F_{in})		DC		1500	MHz
Input Power (P_{in})	DC < $F_{in} \leq 1000 \text{ MHz}$ (Note 1)	-10		+10	dBm
	1000 MHz < $F_{in} \leq 1500$	-3			dBm
Output Power (P_{out})	DC < $F_{in} \leq 1500 \text{ MHz}$	2			dBm

Note 1: CMOS logic levels can be used to drive the reference input if DC coupled. Voltage input needs to be a minimum of 0.5 Vp-p. The input edge rate should be faster than 80mV/ns from DC - 10 MHz.

Table 2. DC Electrical Characteristics ($-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$)

Symbol	Parameter	Condition	Typical	Unit
V_{IH}	High Level Input Voltage	$2.7\text{ V} \leq V_{DD} \leq 3.3\text{ V}$	2.0	V
V_{IL}	Low Level Input Voltage	$2.7\text{ V} \leq V_{DD} \leq 3.3\text{ V}$	0.8	V
V_{OH}	High Level Output Voltage	$V_{DD} = 2.7\text{ V}; I_{OH} = 2.9\text{ mA}$	2.2	V
V_{OL}	Low Level Output Voltage	$V_{DD} = 2.7\text{ V}; I_{OL} = 2.6\text{ mA}$	0.4	V

Table 3. AC Characteristics ($-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$)

Symbol	Parameter	Condition*	Typical	Unit
t_{PHL}	Propagation Delay (High to Low)	50 MHz Pulse Train Input; $C_L = 10\text{ pF}, R_L = 500\ \Omega$	3.0	ns
t_{PLH}	Propagation Delay (Low to High)	50 MHz Pulse Train Input; $C_L = 10\text{ pF}, R_L = 500\ \Omega$	3.2	ns
t_r	Output Rise Time (10% to 90%)	50 MHz Pulse Train Input; $C_L = 10\text{ pF}, R_L = 500\ \Omega$	2.0	ns
t_f	Output Fall Time (90% to 10%)	50 MHz Pulse Train Input; $C_L = 10\text{ pF}, R_L = 500\ \Omega$	2.0	ns

* See figure 5 for AC test circuit

Table 4. Typical Output Swing ($V_{DD} = 2.7\text{ V}$)

Frequency	Condition	Typical	Unit
50 MHz	200 mVp-p Sinusoidal Input; $C_L = 10\text{ pF}, R_L = 500\ \Omega$	2.3	Vp-p
500 MHz	200 mVp-p Sinusoidal Input; $C_L = 10\text{ pF}, R_L = 500\ \Omega$	2.2	Vp-p
1500 MHz	200 mVp-p Sinusoidal Input; $C_L = 10\text{ pF}, R_L = 500\ \Omega$	1.7	Vp-p

Figure 3. Pin Configuration (Top View)

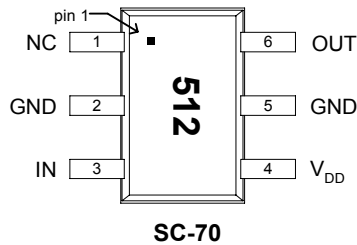


Table 5. Pin Descriptions

Pin No.	Pin Name	Description
1	N/C	No Connect. This pin should be left open.
2	GND	Ground pin. Ground pattern on the board should be as wide as possible to reduce ground impedance.
3	IN	Input signal pin. DC blocking capacitor required (100 pF typical).
4	V _{DD}	Power supply pin. Bypassing is required.
5	GND	Ground pin.
6	OUT	Divided frequency output pin. DC blocking capacitor required (100 pF typical).

Table 6. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V _{DD}	Supply voltage		4.0	V
P _{in}	Input Power		13	dBm
T _{ST}	Storage temperature range	-65	150	°C
T _{OP}	Operating temperature range	-40	85	°C
V _{ESD}	ESD voltage (Human Body Model)		2000	V

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in Table 6.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Device Functional Considerations

The PE3512 divides an input signal, up to a frequency of 1500 MHz, by a factor of four thereby producing an output frequency at one-fourth the input frequency. To work properly with low impedance, ground referenced interfaces, the input and output signals (pins 3 & 6) must be AC coupled via an external capacitor, as shown in the test circuit in Figure 4.

The ground pattern on the board should be made as wide as possible to minimize ground impedance. See Figure 9 for a layout example.

Figure 4. Test Circuit Block Diagram

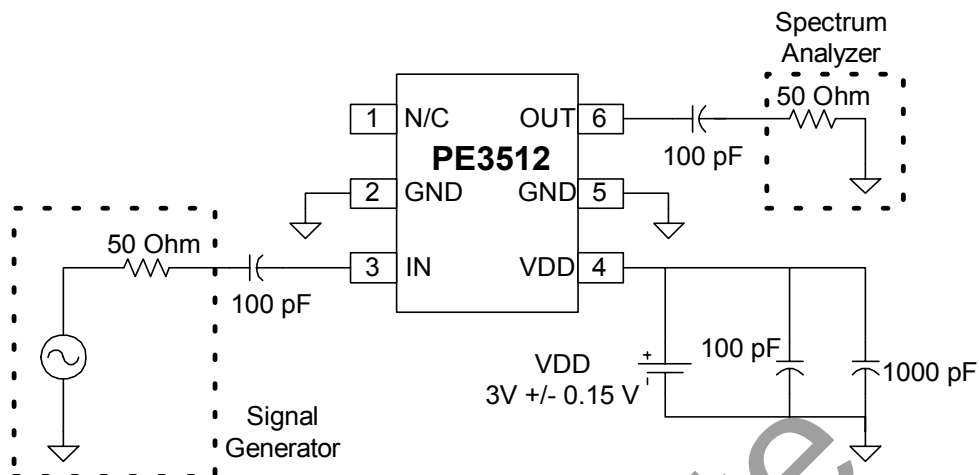
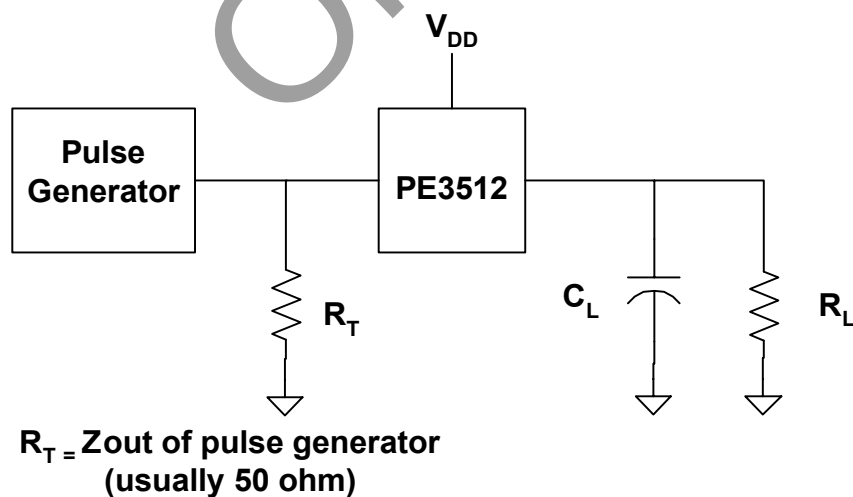


Figure 5. AC Test Circuit



Typical Performance Data: $V_{DD} = 3.0\text{ V}$

Figure 6. Input Sensitivity

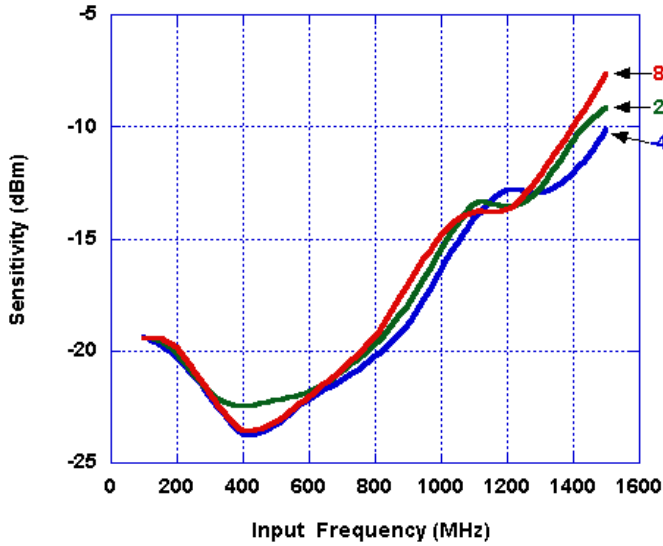


Figure 7. Device Current

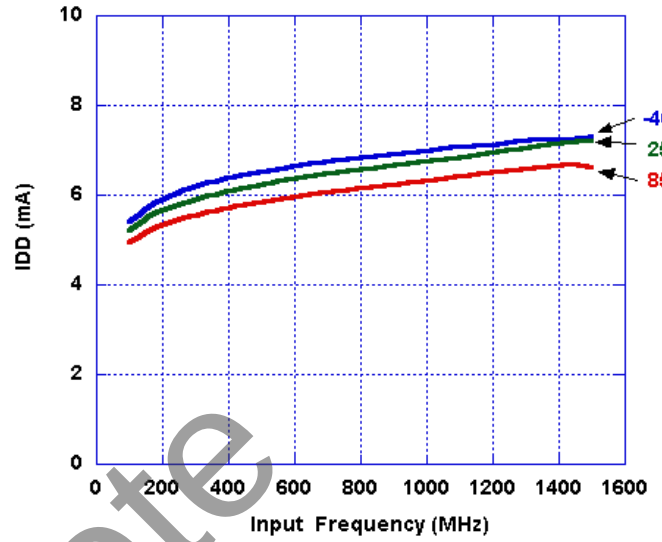
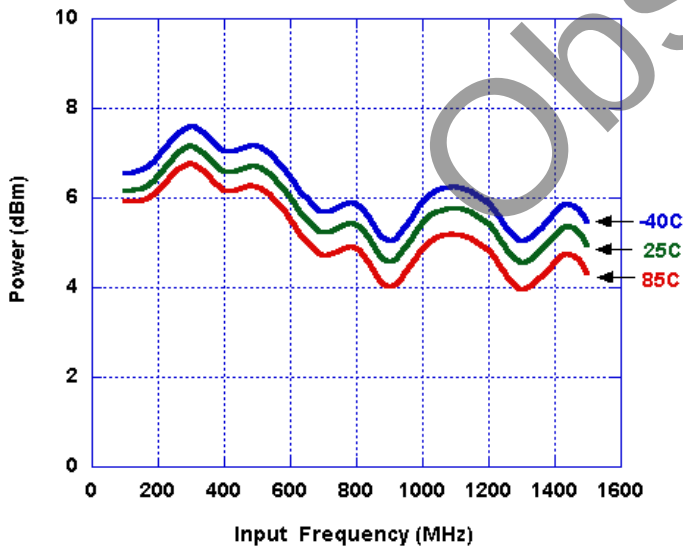


Figure 8. Output Power



Evaluation Kit

Evaluation Kit Operation

The SC-70 Prescaler Evaluation Board was designed to help customers evaluate the **PE3512** divide-by-4 prescaler. On this board, the device input (pin 3) is connected to connector J1 through a 50 Ω transmission line. A series capacitor (C1) provides the necessary DC block for the device input. A value of 100 pF was used for this board layout; other applications may require a different value.

The device output (pin 6) is connected to J3 through a 50 Ω transmission line. A series capacitor (C5) provides the necessary DC block for the device output. This capacitor value must be chosen to have a low impedance at the desired output frequency of the device. A value of 100 pF was chosen for the evaluation board. At both input and output, select a capacitor value that offers low series reactance while ensuring that any parasitic resonances are well above the operating bandwidth.

The board is constructed of a two-layer FR4 material with a total thickness of 0.031". The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide above ground plane model with trace width of 0.030", trace gaps of 0.007", dielectric thickness of 0.028", metal thickness of 0.0014", and ϵ_r of 4.4. Note that the predominate mode of these transmission lines is coplanar waveguide. Liberal numbers of plated through holes unite the top and

bottom ground areas for best performance.

J6 provides DC power to the device via pin 4. Two decoupling capacitors (100 pF, 1000 pF) are included on this trace. It is the customer's responsibility to determine proper supply decoupling for their design application.

Applications Support

If you have a problem with your evaluation kit or if you have applications questions call (858) 731-9400 and ask for applications support. You may also contact us by fax or e-mail:

Fax: (858) 731-9499

E-Mail: help@psemi.com

Figure 9. Evaluation Board Layouts

Peregrine Specification 101/0110

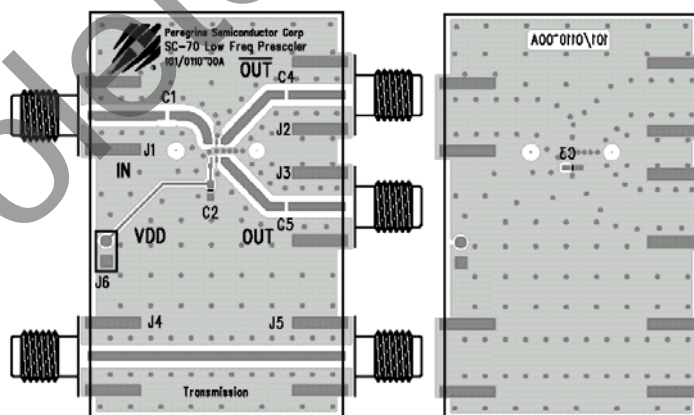


Figure 10. Evaluation Board Schematic

Peregrine Specification 102/0190

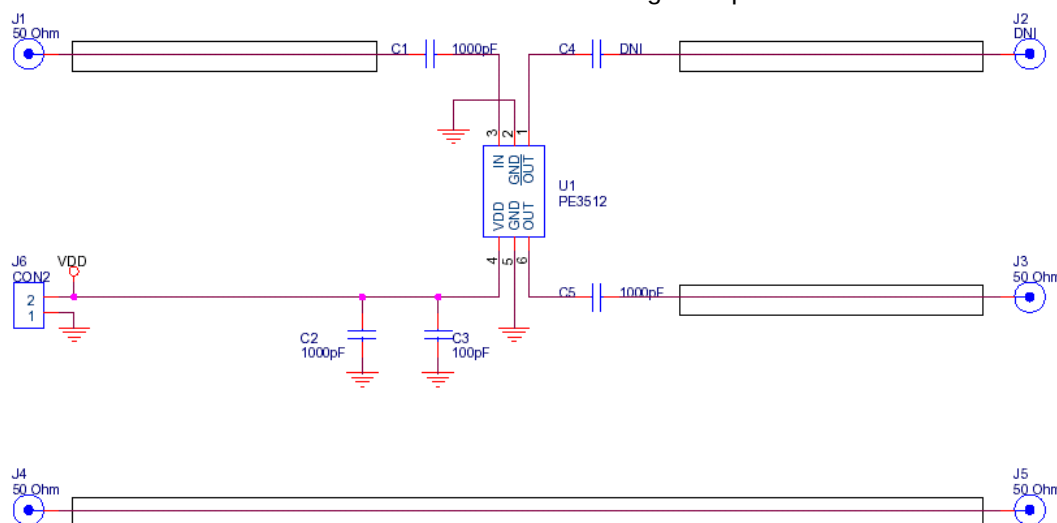
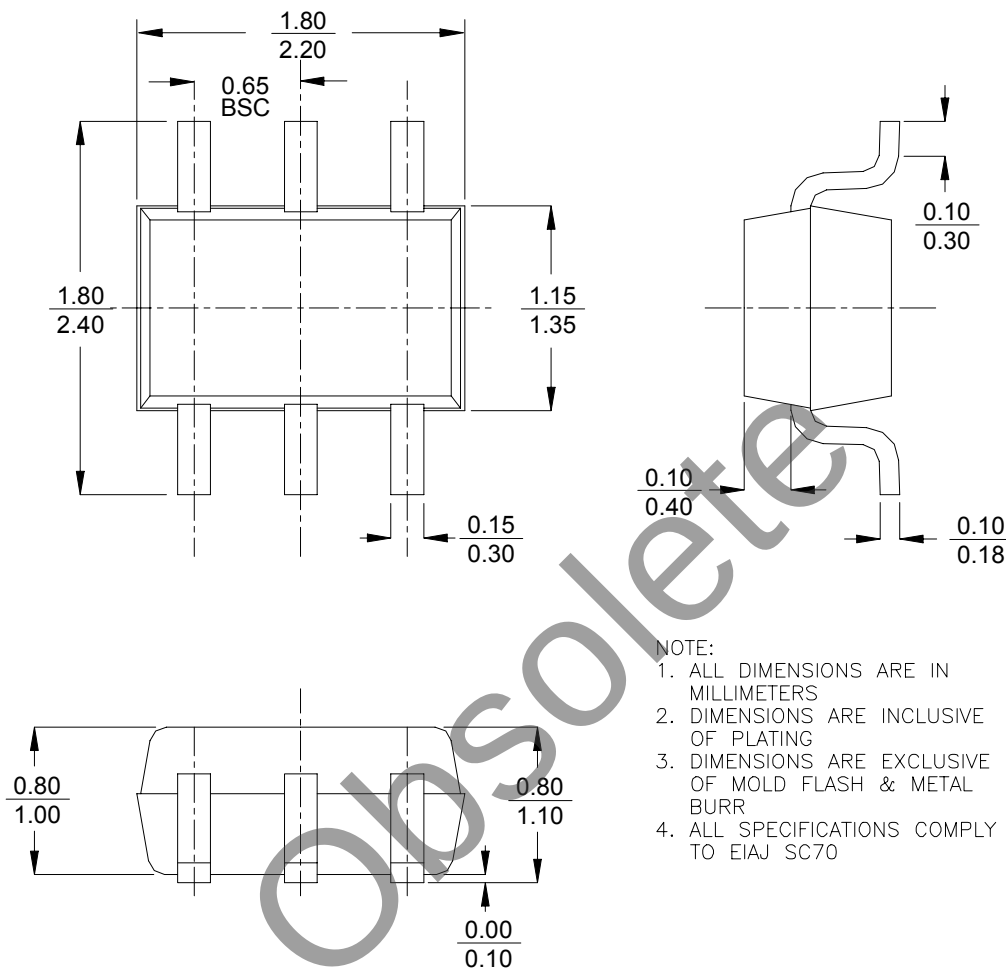


Figure 11. Package Drawing

6-lead SC-70



Technical drawing of a 6-pin connector. The drawing includes a side view and a cross-section view labeled "Section A-A".

Dimensions and Tolerances:

- Overall length: 4.0
- Pin pitch: 2.0 ± 0.05 (See Note 6)
- Pin diameter: $\phi 1.0$ MIN
- Pin spacing (center-to-center): 4.0
- Pin diameter: $\phi 1.5 \pm 0.1/-0.0$
- Pin diameter: 3.5 ± 0.05 (See Note 6)
- Pin diameter: 8.0 ± 0.3
- Pin diameter: 1.75
- Pin diameter: 0.30 ± 0.05
- Pin diameter: $R0.3$ MAX
- Pin diameter: $R0.5$ TYP

Notes:

- See Note 1
- See Note 6
- See Note 6

Section A-A:

Section A-A shows the internal structure of the connector, including the pins and the housing. The section is labeled "Section A-A" and "Pin 1".

Other Labels:

- Bo
- Pin 1
- Ao
- A
- A
- R0.5 TYP

Assembly Direction:

Assembly Direction is indicated by a dashed arrow pointing to the right, labeled "Tape Feed Direction".

1. 10 sprocket hole pitch cumulative tolerance ± 0.2
2. Camber not to exceed 1mm in 100mm.
3. Material: Black Conductive Advantek Polystyrene.
4. Ao and Bo measured on a plane 0.3mm above the bottom of the pocket
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

$A_o = 2.25 \text{ mm}$
 $B_o = 2.4 \text{ mm}$
 $K_o = 1.2 \text{ mm}$

Order Code	Part Marking	Description	Package	Shipping Method
3512-51	512	PE3512G-06SC70-7680A	Green 6-lead SC-70	Tape or loose
3512-52	512	PE3512G-06SC70-3000C	Green 6-lead SC-70	3000 units / T&R
3512-00	PE3512-EK	PE3512-06SC70-EK	Evaluation Kit	1 / Box

Sales Offices

The Americas

Peregrine Semiconductor Corporation

9380 Carroll Park Drive
San Diego, CA 92121
Tel: 858-731-9400
Fax: 858-731-9499

Europe

Peregrine Semiconductor Europe

Bâtiment Maine
13-15 rue des Quatre Vents
F-92380 Garches, France
Tel: +33-1-4741-9173
Fax : +33-1-4741-9173

Space and Defense Products

Americas:

Tel: 858-731-9453

Europe, Asia Pacific:

180 Rue Jean de Guirmand
13852 Aix-En-Provence Cedex 3, France
Tel: +33-4-4239-3361
Fax: +33-4-4239-7227

Peregrine Semiconductor, Asia Pacific (APAC)

Shanghai, 200040, P.R. China
Tel: +86-21-5836-8276
Fax: +86-21-5836-7652

Peregrine Semiconductor, Korea

#B-2607, Kolon Tripolis, #210
Geumgok-dong, Bundang-gu, Seongnam-si
Gyeonggi-do, 463-480 S. Korea
Tel: +82-31-728-4300
Fax: +82-31-728-4305

Peregrine Semiconductor K.K., Japan

Teikoku Hotel Tower 10B-6
1-1-1 Uchisaiwai-cho, Chiyoda-ku
Tokyo 100-0011 Japan
Tel: +81-3-3502-5211
Fax: +81-3-3502-5213

For a list of representatives in your area, please refer to our Web site at: www.psemi.com

Data Sheet Identification

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a DCN (Document Change Notice).

The information in this data sheet is believed to be reliable. However, Peregrine assumes no liability for the use of this information. Use shall be entirely at the user's own risk.

No patent rights or licenses to any circuits described in this data sheet are implied or granted to any third party.

Peregrine's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the Peregrine product could create a situation in which personal injury or death might occur. Peregrine assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

The Peregrine name, logo, and UTSi are registered trademarks and UltraCMOS and HaRP are trademarks of Peregrine Semiconductor Corp.