# CY62147EV18
# MoBL2™

# 4-Mbit (256K x 16) Static RAM

## Features

- **Very high speed: 45 ns**
- **Wide voltage range: 1.65V–2.25V**
- **Pin-compatible with CY62147DV18**
- **Ultra low standby power**
  - **Typical standby current: 1 μA**
  - **Maximum standby current: 7 μA**
- **Ultra-low active power**
  - **Typical active current: 2 mA @ f = 1 MHz**
- **Ultra low standby power**
- **Easy memory expansion with $\overline{CE}$, and $\overline{OE}$ features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Available in a 48-ball Pb-free VFBGA package**

## Functional Description[1]

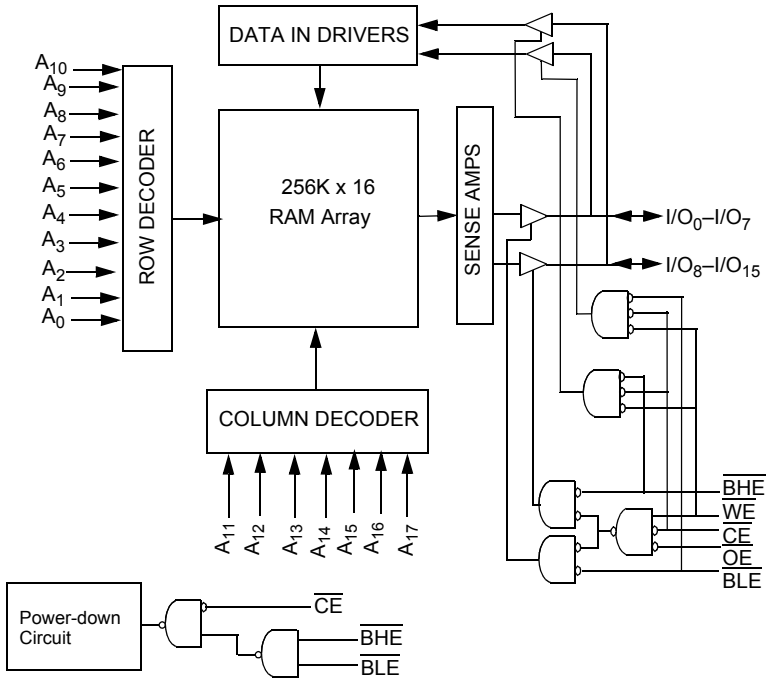
The CY62147EV18 is a high-performance CMOS static RAM organized as 256K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption when addresses are not toggling. The device can also be put into standby mode reducing power consumption by more than 99% when deselected ($\overline{CE}$ HIGH or both BLE and $\overline{BHE}$ are HIGH). The input/output pins ($I/O_0$ through $I/O_{15}$) are placed in a high-impedance state when: deselected ($\overline{CE}$ HIGH), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, BLE HIGH), or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins ($I/O_0$ through $I/O_7$), is written into the location specified on the address pins ($A_0$ through $A_{17}$). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins ($I/O_8$ through $I/O_{15}$) is written into the location specified on the address pins ($A_0$ through $A_{17}$).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on $I/O_0$ to $I/O_7$. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on $I/O_8$ to $I/O_{15}$. See the truth table at the back of this data sheet for a complete description of read and write modes.

The CY62147EV18 is available in a 48-ball VFBGA package.

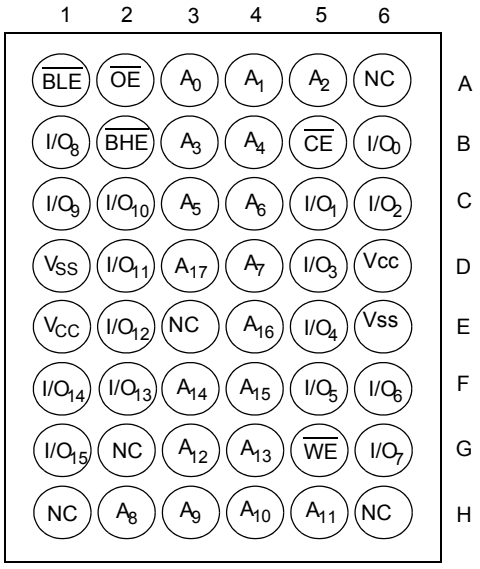
## Logic Block Diagram




**Note:**
1. For best practice recommendations, please refer to the Cypress application note “System Design Guidelines” on http://www.cypress.com.

## Pin Configuration[2, 3]

**48-ball VFBGA Pinout**
**Top View**




## Product Portfolio

| Product | $V_{CC}$ Range (V) | | | Speed (ns) | Power Dissipation | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Operating $I_{CC}$ (mA) | | | | Standby $I_{SB2}$ (µA) | |
| | | | | | f = 1MHz | | f = $f_{max}$ | | | |
| | Min. | Typ.[4] | Max. | | Typ.[4] | Max. | Typ.[4] | Max. | Typ.[4] | Max. |
| CY62147EV18-45LL | 1.65 | 1.8 | 2.25 | 45 | 2 | 2.5 | 15 | 20 | 1 | 7 |

**Notes:**
2. NC pins are not connected on the die.
3. Pins H1, G2, and H6 in the VFBGA package are address expansion pins for 8 Mb, 16 Mb and 32 Mb, respectively.
4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, $T_A = 25°C$.

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to + 150°C

Ambient Temperature with Power Applied .....–55°C to + 125°C

Supply Voltage to Ground Potential .....–0.2V to + 2.45V ($V_{CCMAX}$ + 0.2V)

DC Voltage Applied to Outputs in High-Z State[5,6].....–0.2V to 2.45V ($V_{CCMAX}$ + 0.2V)

DC Input Voltage[5,6]..... –0.2V to 2.45V ($V_{CCMAX}$ + 0.2V)

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current .....> 200 mA

## Operating Range

| Device | Range | Ambient Temperature | $V_{CC}$ [7] |
|---|---|---|---|
| CY62147EV18 | Industrial | –40°C to +85°C | 1.65V to 2.25V |

## Electrical Characteristics (Over the Operating Range)

| Parameter | Description | Test Conditions | | 45 ns | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ.[4] | Max. | |
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = –0.1 mA | $V_{CC}$ = 1.65V | 1.4 | | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 0.1 mA | $V_{CC}$ = 1.65V | | | 0.2 | V |
| $V_{IH}$ | Input HIGH Voltage | $V_{CC}$ =1.65V to 2.25V | | 1.4 | | $V_{CC}$+ 0.2V | V |
| $V_{IL}$ | Input LOW Voltage | $V_{CC}$ =1.65V to 2.25V | | –0.2 | | 0.4 | V |
| $I_{IX}$ | Input Leakage Current | GND ≤ $V_I$ ≤ $V_{CC}$ | | –1 | | +1 | µA |
| $I_{OZ}$ | Output Leakage Current | GND ≤ $V_O$ ≤ $V_{CC}$, Output Disabled | | –1 | | +1 | µA |
| $I_{CC}$ | $V_{CC}$ Operating Supply Current | f = $f_{MAX}$ = 1/$t_{RC}$ | $V_{CC(max)}$=2.25V $I_{OUT}$ = 0 mA CMOS levels | | 15 | 20 | mA |
| | | f = 1 MHz | $V_{CC(max)}$=2.25V | | 2 | 2.5 | mA |
| $I_{SB1}$ | Automatic CE Power-down Current — CMOS Inputs | $\overline{CE}$ ≥ $V_{CC}$–0.2V, $V_{IN}$≥$V_{CC}$ – 0.2V, $V_{IN}$ ≤ 0.2V) f = $f_{MAX}$ (Address and Data Only), f = 0 ($\overline{OE}$, $\overline{WE}$, $\overline{BHE}$ and $\overline{BLE}$) | $V_{CC(max)}$=2.25V | | 1 | 7 | µA |
| $I_{SB2}$ | Automatic CE Power-down Current — CMOS Inputs | $\overline{CE}$ ≥ $V_{CC}$ – 0.2V, $V_{IN}$ ≥ $V_{CC}$ – 0.2V or $V_{IN}$ ≤ 0.2V, f = 0 | $V_{CC(max)}$=2.25V | | 1 | 7 | µA |

## Capacitance (for all Packages) [8]

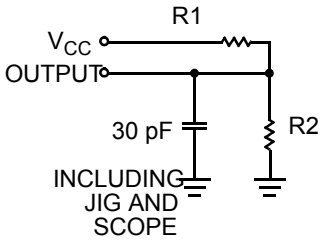
| Parameter | Description | Test Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $T_A$ = 25°C, f = 1 MHz, $V_{CC}$ = $V_{CC(typ)}$ | 10 | pF |
| $C_{OUT}$ | Output Capacitance | | 10 | pF |

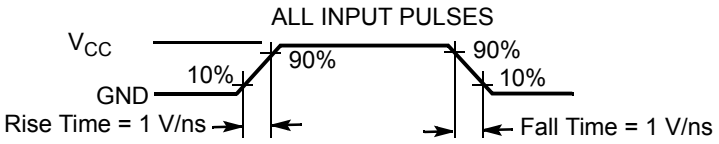
**Note:**
5. $V_{IL(min.)}$ = –2.0V for pulse durations less than 20 ns.
6. $V_{IH(max)}$=$V_{CC}$+0.5V for pulse durations less than 20 ns.
7. Full device AC operation assumes a minimum of 100 µs ramp time from 0 to $V_{cc}$(min) and 200 µs wait time after $V_{cc}$ stabilization.
8. Tested initially and after any design or process changes that may affect these parameters.

## Thermal Resistance

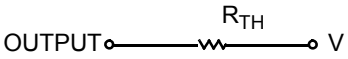
| Parameter | Description | Test Conditions | VFBGA Package | Unit |
|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal Resistance (Junction to Ambient)[8] | Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board | 75 | °C/W |
| $\Theta_{JC}$ | Thermal Resistance (Junction to Case)[8] | | 10 | °C/W |

## AC Test Loads and Waveforms




Equivalentto: THEVENIN EQUIVALENT

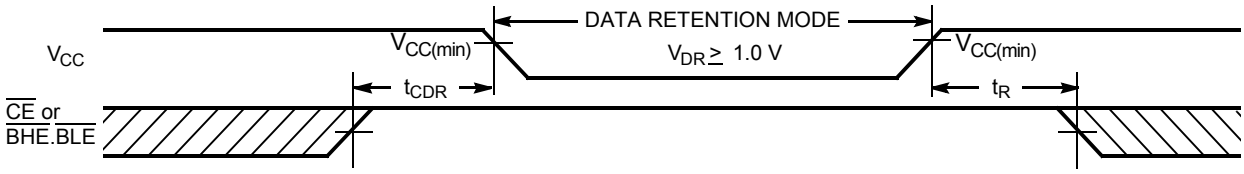



| Parameters | 1.80V | Unit |
|---|---|---|
| R1 | 13500 | Ω |
| R2 | 10800 | Ω |
| $R_{TH}$ | 6000 | Ω |
| $V_{TH}$ | 0.80 | V |

## Data Retention Characteristics (Over the Operating Range)

| Parameter | Description | Conditions | Min. | Typ.[4] | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{CC}$ for Data Retention | | 1.0 | | | V |
| $I_{CCDR}$ | Data Retention Current | $V_{CC}$= 1.0V<br>$\overline{CE} \geq V_{CC} - 0.2V$,<br>$V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ | | 0.5 | 3 | µA |
| $t_{CDR}$[7] | Chip Deselect to Data Retention Time | | 0 | | | ns |
| $t_R$[9] | Operation Recovery Time | | $t_{RC}$ | | | ns |

## Data Retention Waveform[10]




**Notes:**
9. Full device operation requires linear $V_{CC}$ ramp from $V_{DR}$ to $V_{CC(min.)} \geq 100$ µs or stable at $V_{CC(min.)} \geq 100$µs.
10. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Chip can be deselected by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

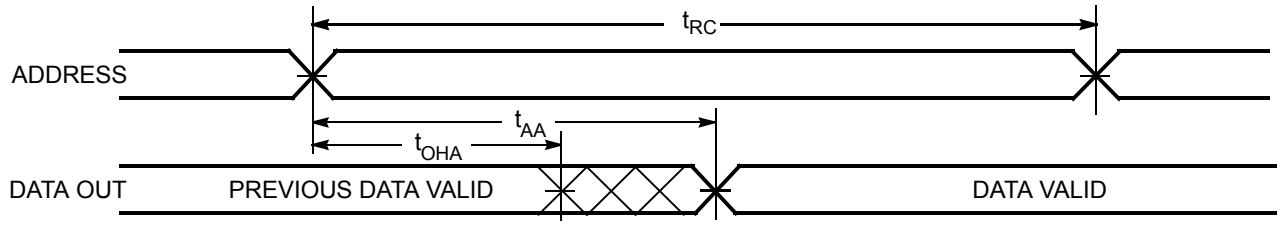
## Switching Characteristics (Over the Operating Range) [11]

| Parameter | Description | 45 ns | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| **Read Cycle** | | | | |
| $t_{RC}$ | Read Cycle Time | 45 | | ns |
| $t_{AA}$ | Address to Data Valid | | 45 | ns |
| $t_{OHA}$ | Data Hold from Address Change | 10 | | ns |
| $t_{ACE}$ | $\overline{CE}$ LOW to Data Valid | | 45 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to Data Valid | | 22 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to LOW Z[12] | 5 | | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to High Z[12, 13] | | 18 | ns |
| $t_{LZCE}$ | $\overline{CE}$ LOW to Low Z[12] | 10 | | ns |
| $t_{HZCE}$ | $\overline{CE}$ HIGH to High Z[12, 13] | | 18 | ns |
| $t_{PU}$ | $\overline{CE}$ LOW to Power-up | 0 | | ns |
| $t_{PD}$ | $\overline{CE}$ HIGH to Power-down | | 45 | ns |
| $t_{DBE}$ | $\overline{BLE}/\overline{BHE}$ LOW to Data Valid | | 45 | ns |
| $t_{LZBE}$ | $\overline{BLE}/\overline{BHE}$ LOW to Low Z[12 ] | 10 | | ns |
| $t_{HZBE}$ | $\overline{BLE}/\overline{BHE}$ HIGH to HIGH Z[12, 13] | | 18 | ns |
| **Write Cycle**[14] | | | | |
| $t_{WC}$ | Write Cycle Time | 45 | | ns |
| $t_{SCE}$ | $\overline{CE}$ LOW to Write End | 35 | | ns |
| $t_{AW}$ | Address Set-up to Write End | 35 | | ns |
| $t_{HA}$ | Address Hold from Write End | 0 | | ns |
| $t_{SA}$ | Address Set-up to Write Start | 0 | | ns |
| $t_{PWE}$ | $\overline{WE}$ Pulse Width | 35 | | ns |
| $t_{BW}$ | $\overline{BLE}/\overline{BHE}$ LOW to Write End | 35 | | ns |
| $t_{SD}$ | Data Set-up to Write End | 25 | | ns |
| $t_{HD}$ | Data Hold from Write End | 0 | | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to High-Z[12, 13] | | 18 | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to Low-Z[12] | 10 | | ns |

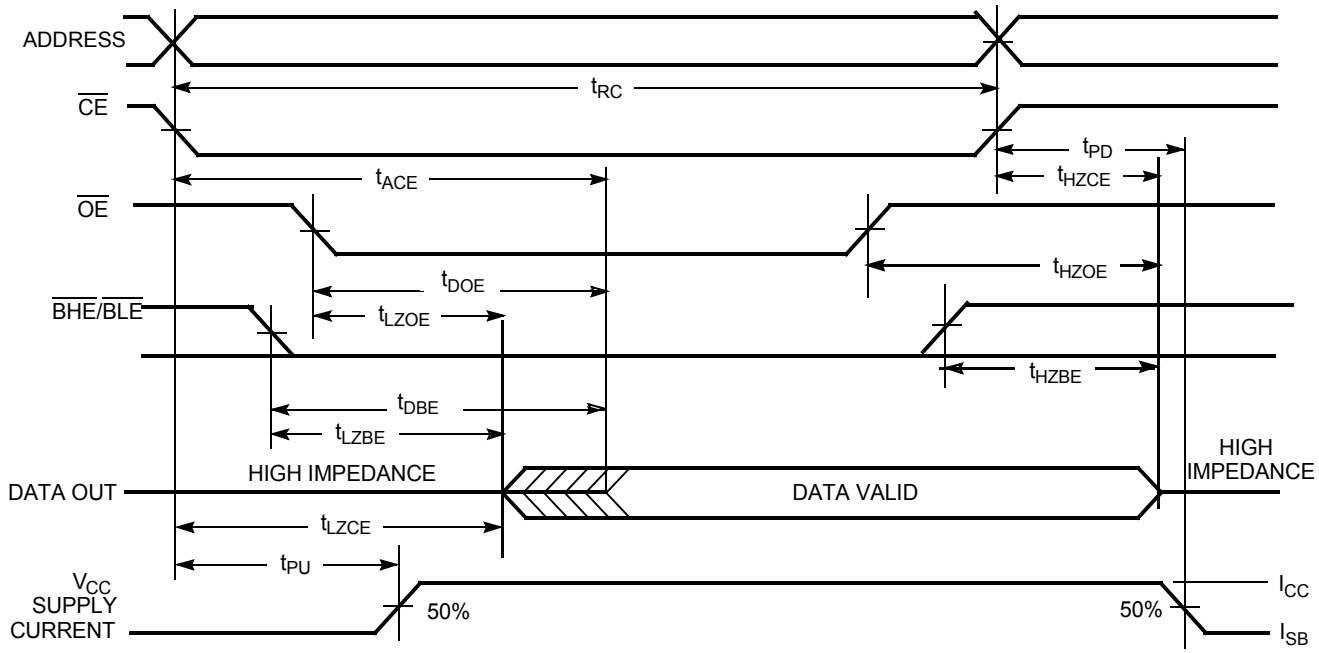
**Notes:**
11. Test conditions for all parameters other than three-state parameters assume signal transition time of 1V/ns or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified $I_{OL}/I_{OH}$ as shown in the “AC Test Loads and Waveforms” section.
12. At any given temperature and voltage condition, $t_{HZCE}$ is less than $t_{LZCE}$, $t_{HZBE}$ is less than $t_{LZBE}$, $t_{HZOE}$ is less than $t_{LZOE}$, and $t_{HZWE}$ is less than $t_{LZWE}$ for any given device.
13. $t_{HZOE}$, $t_{HZCE}$, $t_{HZBE}$, and $t_{HZWE}$ transitions are measured when the outputs enter a high impedence state
14. The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = $V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE}$ = $V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

## Switching Waveforms

### Read Cycle 1 (Address Transition Controlled)[15, 16]



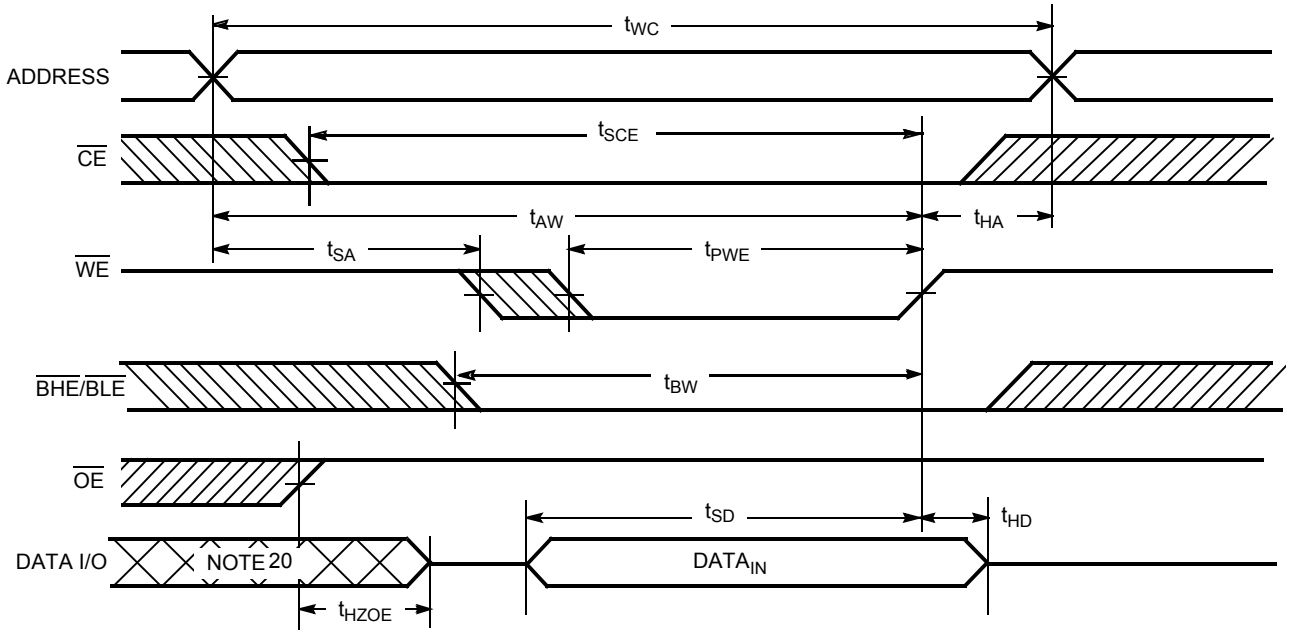

### Read Cycle No. 2 ($\overline{OE}$ Controlled)[16, 17]



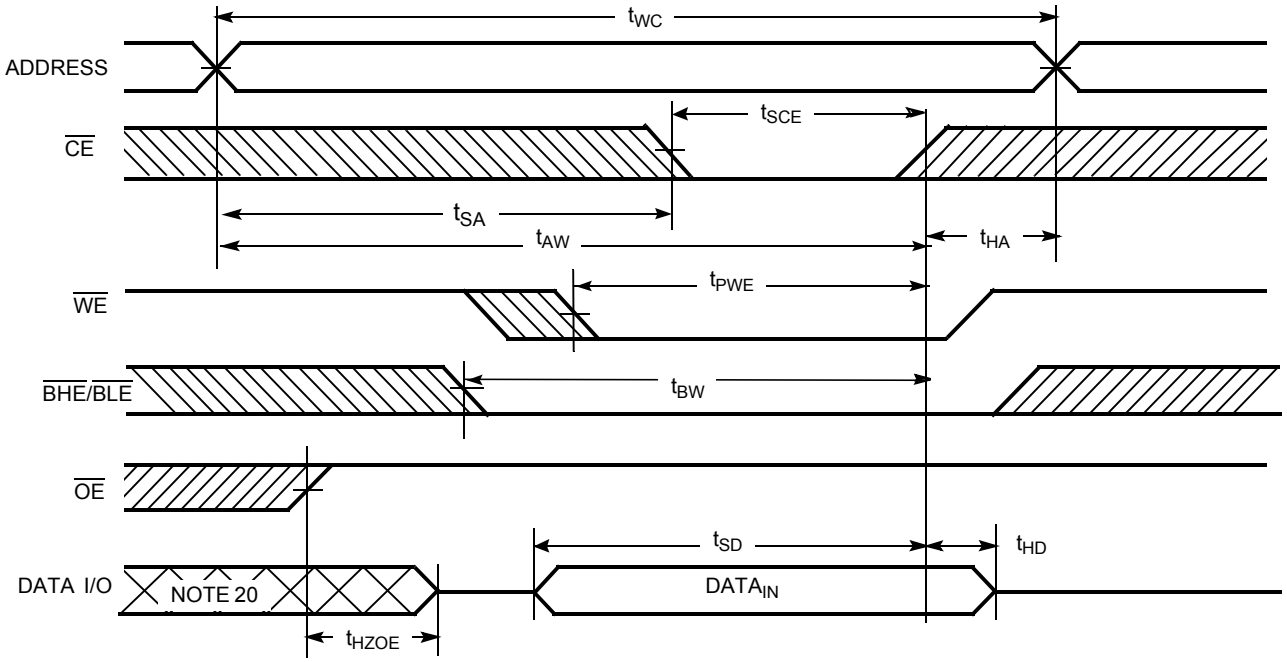

**Notes:**
15. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = $V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE}$ = $V_{IL}$.
16. $\overline{WE}$ is HIGH for read cycle.
17. Address valid prior to or coincident with $\overline{CE}$ and $\overline{BHE}$, $\overline{BLE}$ transition LOW.

## Switching Waveforms (continued)

### Write Cycle No. 1 (WE Controlled)[14, 18, 19]



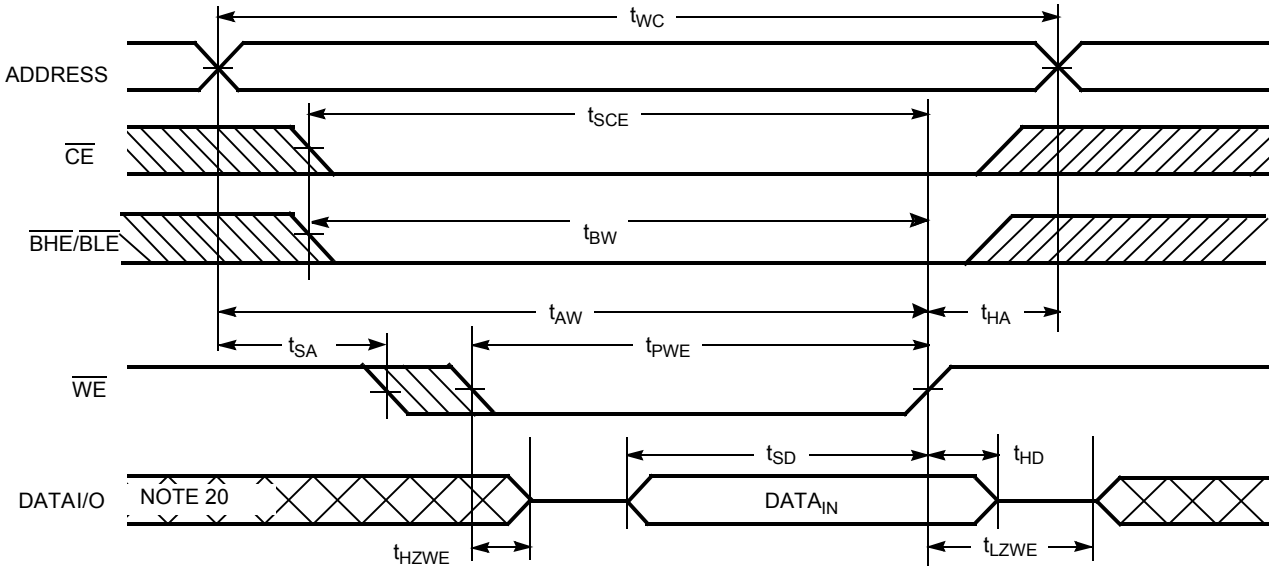

### Write Cycle No. 2 (CE Controlled)[14, 18, 19]



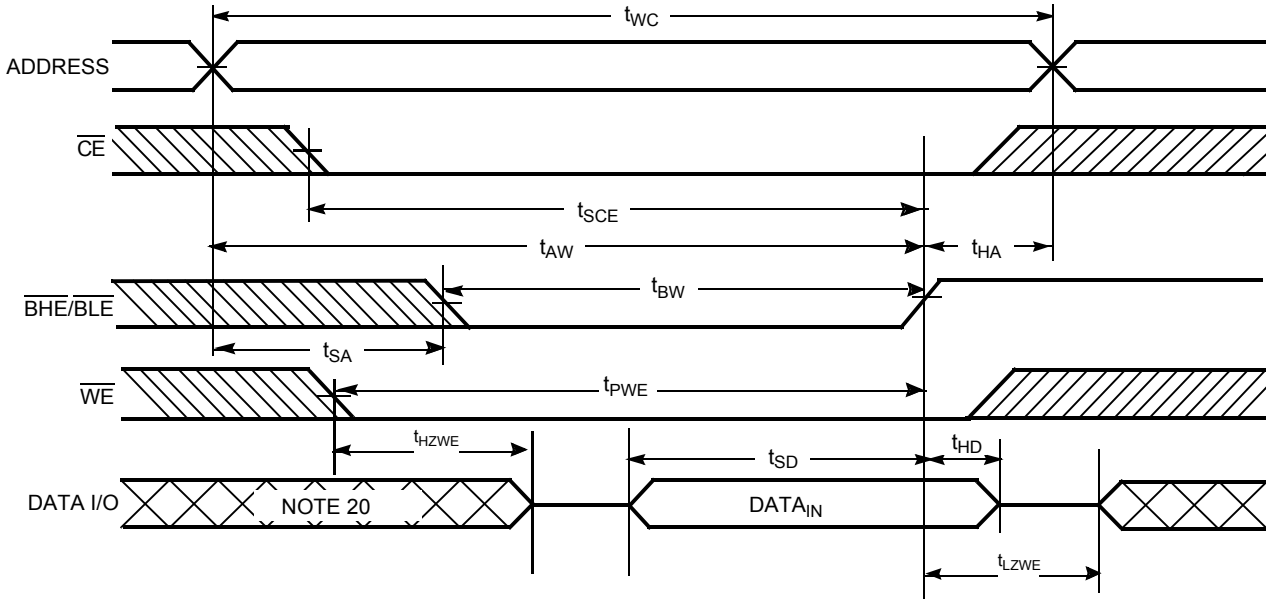

**Notes:**
18. Data I/O is high impedance if $\overline{OE}$ = $V_{IH}$.
19. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ = $V_{IH}$, the output remains in a high-impedance state.
20. During this period, the I/Os are in output state and input signals should not be applied.

## Switching Waveforms (continued)

### Write Cycle No. 3 (WE Controlled, OE LOW)[19]




### Write Cycle No. 4 (BHE/BLE Controlled, OE LOW)[19]



## Truth Table

| $\overline{CE}$ | $\overline{WE}$ | $\overline{OE}$ | $\overline{BHE}$ | $\overline{BLE}$ | Inputs/Outputs | Mode | Power |
|---|---|---|---|---|---|---|---|
| H | X | X | X | X | High Z | Deselect/Power-down | Standby ($I_{SB}$) |
| L | X | X | H | H | High Z | Deselect/Power-down | Standby ($I_{SB}$) |
| L | H | L | L | L | Data Out ($I/O_O$–$I/O_{15}$) | Read | Active ($I_{CC}$) |
| L | H | L | H | L | Data Out ($I/O_O$–$I/O_7$); $I/O_8$–$I/O_{15}$ in High Z | Read | Active ($I_{CC}$) |
| L | H | L | L | H | Data Out ($I/O_8$–$I/O_{15}$); $I/O_0$–$I/O_7$ in High Z | Read | Active ($I_{CC}$) |
| L | H | H | L | L | High Z | Output Disabled | Active ($I_{CC}$) |
| L | H | H | H | L | High Z | Output Disabled | Active ($I_{CC}$) |
| L | H | H | L | H | High Z | Output Disabled | Active ($I_{CC}$) |
| L | L | X | L | L | Data In ($I/O_O$–$I/O_{15}$) | Write | Active ($I_{CC}$) |
| L | L | X | H | L | Data In ($I/O_O$–$I/O_7$); $I/O_8$–$I/O_{15}$ in High Z | Write | Active ($I_{CC}$) |
| L | L | X | L | H | Data In ($I/O_8$–$I/O_{15}$); $I/O_0$–$I/O_7$ in High Z | Write | Active ($I_{CC}$) |

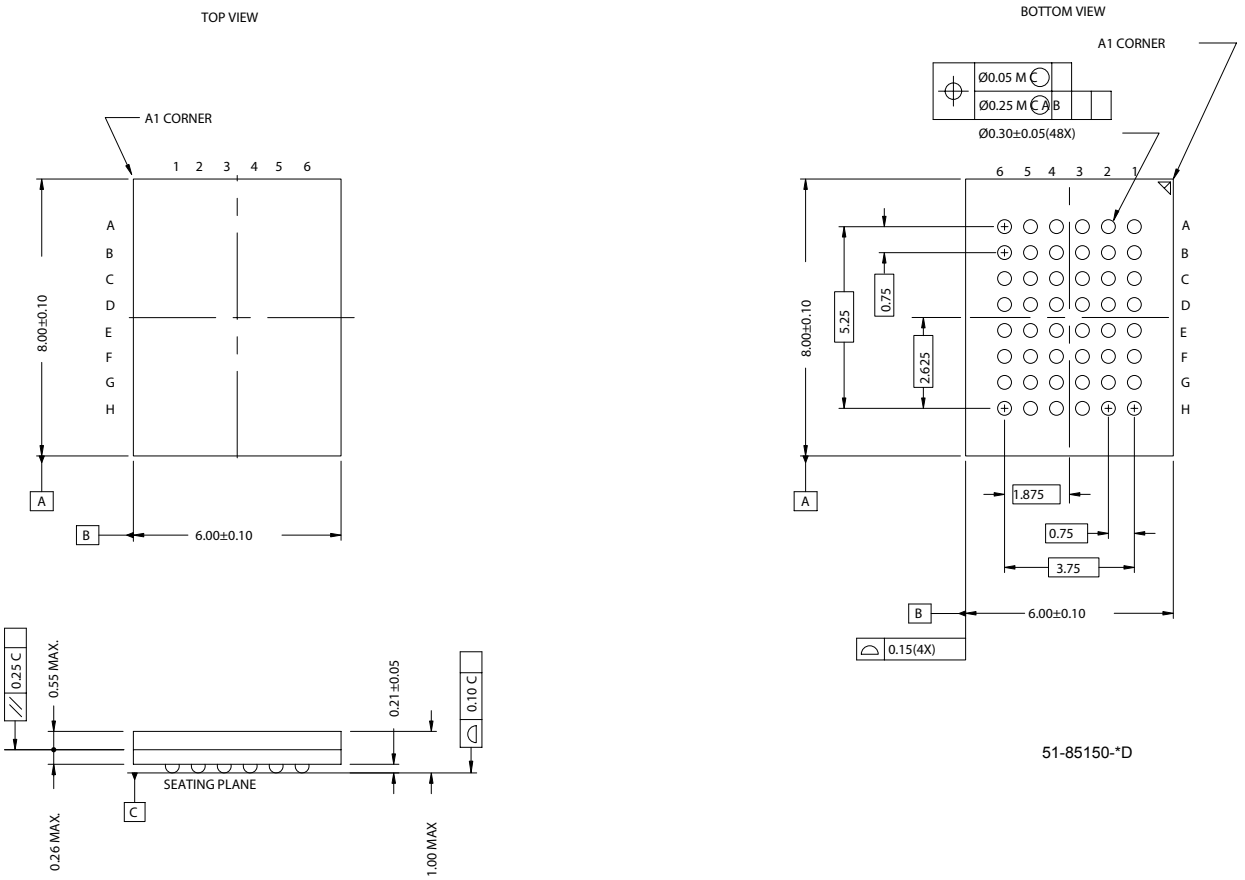
## Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|---|
| 45 | CY62147EV18LL-45BVXI | 51-85150 | 48-ball Very Fine Pitch Ball Grid Array Pb-Free | Industrial |

Please contact your local Cypress sales representative for availability of other parts

## Package Diagram

**48-pin VFBGA (6 x 8 x 1 mm) (51-85150)**



## Document History Page

| Document Title:CY62147EV18 MoBL2™ 4-Mbit (256K x 16) Static RAM<br>Document Number: 38-05441 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN NO.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 201580 | 01/08/04 | AJU | New Data Sheet |
| *A | 247009 | See ECN | SYT | Changed from Advance Information to Preliminary<br>Moved Product Portfolio to Page 2<br>Changed $V_{CCMax}$ from 2.20 to 2.25 V<br>Changed $V_{CC}$ stabilization time in footnote #8 from 100 μs to 200 μs<br>Removed Footnote #15 ($t_{LZBE}$) from Previous Revision<br>Changed $I_{CCDR}$ from 2.0 μA to 2.5 μA<br>Changed typo in Data Retention Characteristics ($t_R$) from 100 μs to $t_{RC}$ ns<br>Changed $t_{OHA}$ from 6 ns to 10 ns for both 35 ns and 45 ns Speed Bin<br>Changed $t_{HZOE}$, $t_{HZBE}$, $t_{HZWE}$ from 12 to 15 ns for 35 ns Speed Bin and 15 to 18 ns for 45 ns Speed Bin<br>Changed $t_{SCE}$ and $t_{BW}$ from 25 to 30 ns for 35 ns Speed Bin and 40 to 35 ns for 45 ns Speed Bin<br>Changed $t_{HZCE}$ from 12 to 18 ns for 35 ns Speed Bin and 15 to 22 ns for 45 ns Speed Bin<br>Changed $t_{SD}$ from 15 to 18 ns for 35 ns Speed Bin and 20 to 22 ns for 45 ns Speed Bin<br>Changed $t_{DOE}$ from 15 to 18 ns for 35 ns Speed Bin<br>Changed Ordering Information to include Pb-Free Packages |
| *B | 414820 | See ECN | ZSD | Changed from Preliminary to Final<br>Changed the address of Cypress Semiconductor Corporation on Page #1 from “3901 North First Street” to “198 Champion Court”<br>Removed 35ns Speed Bin<br>Removed “L” version of CY62147EV18<br>Changed ball E3 from DNU to NC<br>Changed $I_{CC}$ (Typ) value from 1.5 mA to 2 mA at f=1 MHz<br>Changed $I_{CC}$ (Max) value from 2 mA to 2.5 mA at f=1 MHz<br>Changed $I_{CC}$ (Typ) value from 12 mA to 15 mA at f=$f_{max}$<br>Changed $I_{SB1}$ and $I_{SB2}$ Typ. values from 0.7 μA to 1 μA and Max. values from 2.5 μA to 7 μA.<br>Extended undershoot limit to -2V in footnote #5<br>Changed $I_{CCDR}$ Max. from 2.5 μA to 3 μA.<br>Added $I_{CCDR}$ typical value.<br>Changed $t_{LZOE}$ from 3 ns to 5 ns<br>Changed $t_{LZCE}$, $t_{LZBE}$ and $t_{LZWE}$ from 6 ns to 10 ns<br>Changed $t_{HZCE}$ from 22 ns to 18 ns<br>Changed $t_{PWE}$ from 30 ns to 35 ns.<br>Changed $t_{SD}$ from 22 ns to 25 ns.<br>Updated the package diagram 48-pin VFBGA from *B to *D<br>Updated the ordering information table and replaced Package Name column with Package Diagram |