

## FEATURES

- Single Chip With Easy Interface Between UART and Serial-Port Connector of IBM™ PC/AT™ and Compatibles
- Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards
- Supports Data Rates up to 120 kbit/s
- ESD Protection Meets or Exceeds 10 kV on RS-232 Pins and 3.5 kV on All Other Pins (Human-Body Model)
- Pin-to-Pin Compatible With the SN75C185

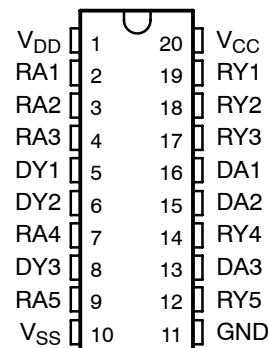
## DESCRIPTION/ORDERING INFORMATION

The SN75185 combines three drivers and five receivers from the TI SN75188 and SN75189 bipolar quadruple drivers and receivers, respectively. The pinout matches the flow-through design of the SN75C185 to decrease the part count, reduce the board space required, and allow easy interconnection of the UART and serial-port connector of IBM™ PC/AT™ and compatibles. The bipolar circuits and processing of the SN75185 provide a rugged low-cost solution for this function at the expense of quiescent power and external passive components relative to the SN75C185.

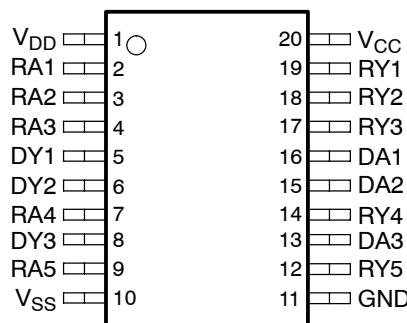
The SN75185 complies with the requirements of the TIA/EIA-232-F and ITU v.28 standards. These standards are for data interchange between a host computer and peripheral at signaling rates up to 20 kbit/s. The switching speeds of the SN75185 are fast enough to support rates up to 120 kbit/s with lower capacitive loads (shorter cables). Interoperability at the higher signaling rates cannot be assured unless the designer has design control of the cable and the interface circuits at both ends. For interoperability at signaling rates to 120 kbit/s, use of TIA/EIA-423-B (ITU v.10) and TIA/EIA-422-B (ITU v.11) standards is recommended.

The SN75185 is characterized for operation over the temperature range of 0°C to 70°C.

**N PACKAGE  
(TOP VIEW)**



**DB, DW, OR PW PACKAGE  
(TOP VIEW)**



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**SN75185**  
**MULTIPLE RS-232 DRIVERS AND RECEIVERS**

SLLS181D—DECEMBER 1994—REVISED JANUARY 2006

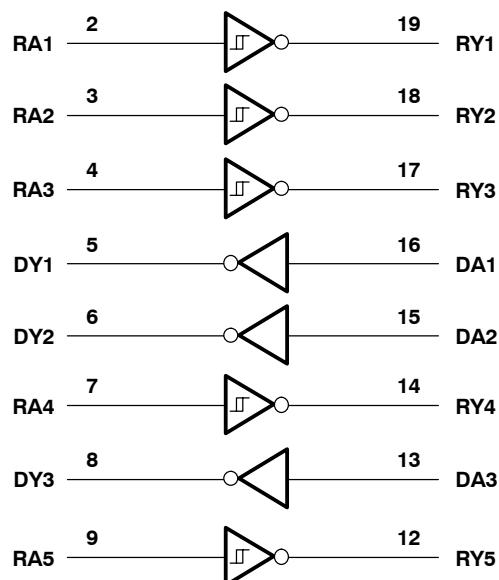
 **TEXAS  
INSTRUMENTS**  
[www.ti.com](http://www.ti.com)

**ORDERING INFORMATION**

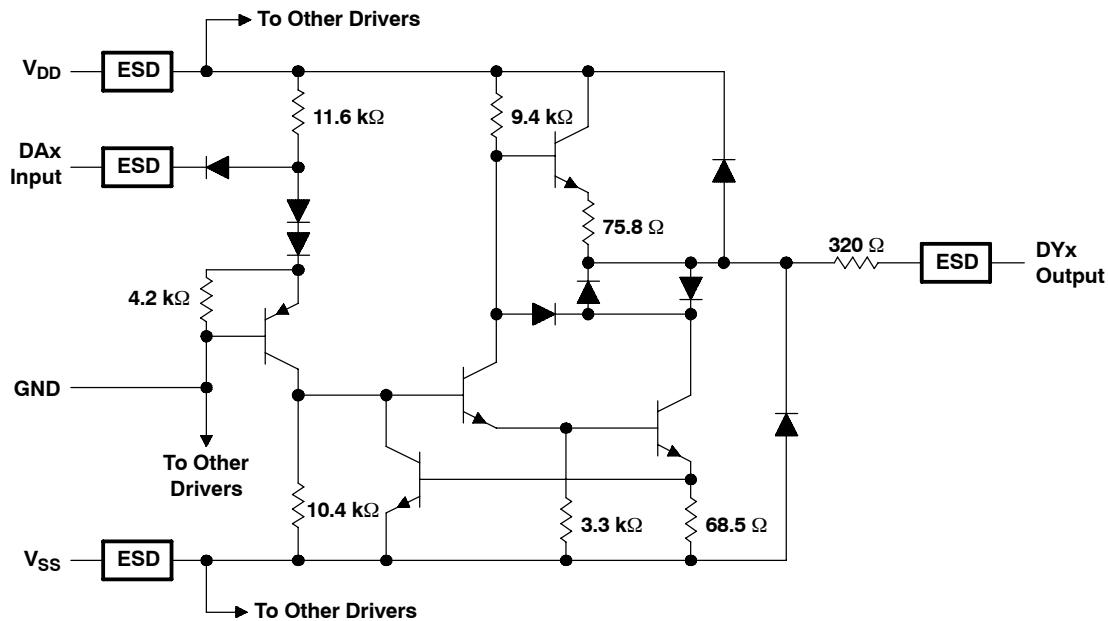
<b>T<sub>A</sub></b>	<b>PACKAGE<sup>(1)</sup></b>		<b>ORDERABLE PART NUMBER</b>	<b>TOP-SIDE MARKING</b>
0°C to 70°C	PDIP – N	Tube of 20	SN75185N	SN75185N
	SOIC – DW	Tube of 25	SN75185DW	
		Reel of 2000	SN75185DWR	SN75185
	SSOP – DB	Tube of 70	SN75185DB	
		Reel of 2000	SN75185DBR	A185
	TSSOP – PW	Tube of 70	SN75185PW	
		Reel of 2000	SN75185PWR	A185

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

**LOGIC DIAGRAM (POSITIVE LOGIC)**

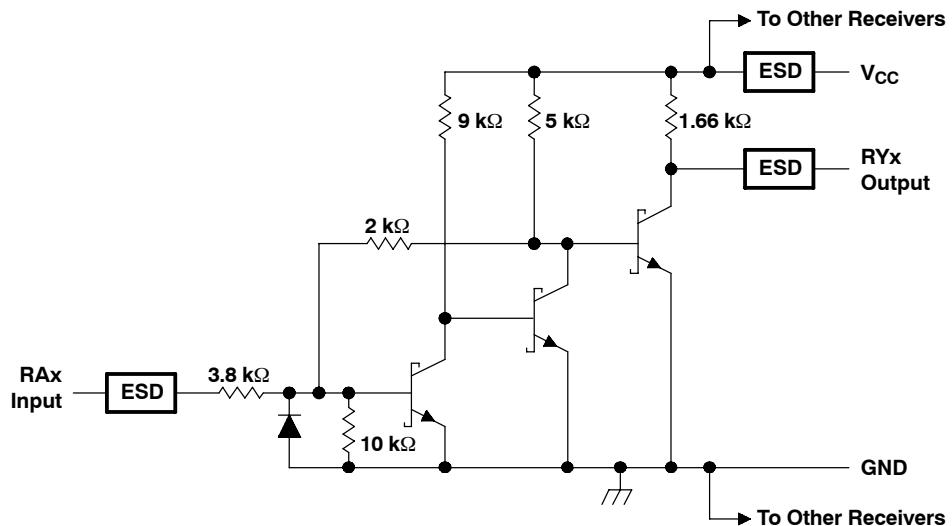


SCHEMATIC OF DRIVERS



Resistor values shown are nominal.

SCHEMATIC (EACH RECEIVER)



Resistor values shown are nominal.

**SN75185**  
**MULTIPLE RS-232 DRIVERS AND RECEIVERS**

SLLS181D—DECEMBER 1994—REVISED JANUARY 2006



**Absolute Maximum Ratings<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage <sup>(2)</sup>		10	V
$V_{DD}$	Supply voltage <sup>(2)</sup>		15	V
$V_{SS}$	Supply voltage <sup>(2)</sup>		-15	V
Input voltage range	Driver	-15	7	V
	Receiver	-30	30	
Driver output voltage range		-15	15	V
Receiver low-level output current			20	mA
$\theta_{JA}$	Package thermal impedance <sup>(3)(4)</sup>	DB package	70	°C/W
		DW package	58	
		N package	69	
		PW package	83	
$T_J$	Operating virtual junction temperature		150	°C
Electrostatic discharge	Human-Body Model	RS-232 pins, class 3, A <sup>(5)</sup>	10	kV
		All pins, class 3, A <sup>(6)</sup>	3.5	
	Machine Model	RS-232 pins, class 3, B <sup>(7)</sup>	600	V
		All pins, class 3, B <sup>(5)</sup>	250	
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to the network ground terminal.
- (3) Maximum power dissipation is a function of  $T_J$ (max),  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\max) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) RS-232 pins are tested with respect to ground and to each other.
- (6) Per MIL-PRF-38535
- (7) RS-232 pins are tested with respect to ground.

**Recommended Operating Conditions**

			MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage		4.5	5	5.5	V
$V_{DD}$	Supply voltage		7.5	9	15	V
$V_{SS}$	Supply voltage		-7.5	-9	-15	V
$V_{IH}$	High-level input voltage (drivers only)		1.9			V
$V_{IL}$	Low-level input voltage (drivers only)			0.8		V
$I_{OH}$	High-level output current	Drivers		-6		mA
		Receivers		-0.5		
$I_{OL}$	Low-level output current	Drivers		6		mA
		Receivers		16		
$T_A$	Operating free-air temperature		0	70		°C

**Supply Currents**

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
$I_{CC}$	Supply current from $V_{CC}$	All inputs at 5 V,	No load,	$V_{CC} = 5$ V		30	mA
	All inputs at 1.9 V,	No load	$V_{DD} = 9$ V, $V_{SS} = -9$ V		15	mA	
			$V_{DD} = 12$ V, $V_{SS} = -12$ V		19		
			$V_{DD} = 15$ V, $V_{SS} = -15$ V		25		
	All inputs at 0.8 V,	No load	$V_{DD} = 9$ V, $V_{SS} = -9$ V		4.5		
			$V_{DD} = 12$ V, $V_{SS} = -12$ V		5.5		
			$V_{DD} = 15$ V, $V_{SS} = -15$ V		9		
$I_{DD}$	Supply current from $V_{DD}$	All inputs at 1.9 V,	No load	$V_{DD} = 9$ V, $V_{SS} = -9$ V		-15	mA
				$V_{DD} = 12$ V, $V_{SS} = -12$ V		-19	
				$V_{DD} = 15$ V, $V_{SS} = -15$ V		-25	
		All inputs at 0.8 V,	No load	$V_{DD} = 9$ V, $V_{SS} = -9$ V		-3.2	
				$V_{DD} = 12$ V, $V_{SS} = -12$ V		-3.2	
				$V_{DD} = 15$ V, $V_{SS} = -15$ V		-3.2	
$I_{SS}$	Supply current from $V_{SS}$	All inputs at 1.9 V,	No load	$V_{DD} = 9$ V, $V_{SS} = -9$ V		-3.2	mA
				$V_{DD} = 12$ V, $V_{SS} = -12$ V		-3.2	
				$V_{DD} = 15$ V, $V_{SS} = -15$ V		-3.2	
		All inputs at 0.8 V,	No load	$V_{DD} = 9$ V, $V_{SS} = -9$ V		-3.2	
				$V_{DD} = 12$ V, $V_{SS} = -12$ V		-3.2	
				$V_{DD} = 15$ V, $V_{SS} = -15$ V		-3.2	

## DRIVER SECTION

### Electrical Characteristics

over recommended operating free-air temperature range,  $V_{DD} = 9$  V,  $V_{SS} = -9$  V,  $V_{CC} = 5$  V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH}$ High-level output voltage	$V_{IL} = 0.8$ V, $R_L = 3$ k $\Omega$ , See Figure 1	6	7.5		V
$V_{OL}$ Low-level output voltage <sup>(1)</sup>	$V_{IH} = 1.9$ V, $R_L = 3$ k $\Omega$ , See Figure 1		-7.5	-6	V
$I_{IH}$ High-level input current	$V_I = 5$ V, See Figure 2			10	$\mu$ A
$I_{IL}$ Low-level input current	$V_I = 0$ , See Figure 2			-1.6	mA
$I_{OS(H)}$ High-level short-circuit output current <sup>(2)</sup>	$V_{IL} = 0.8$ V, $V_O = 0$ , See Figure 1	-4.5	-12	-19.5	mA
$I_{OS(L)}$ Low-level short-circuit output current	$V_{IH} = 2$ V, $V_O = 0$ , See Figure 1	4.5	12	19.5	mA
$r_o$ Output resistance <sup>(3)</sup>	$V_{CC} = V_{DD} = V_{SS} = 0$ , $V_O = -2$ V to 2 V	300			$\Omega$

- (1) The algebraic convention, in which the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only (e.g., if -10 V is maximum, the typical value is a more negative voltage).
- (2) Output short-circuit conditions must maintain the total power dissipation below absolute maximum ratings.
- (3) Test conditions are those specified by TIA/EIA-232-F and as listed above.

### Switching Characteristics

$V_{CC} = 5$  V,  $V_{DD} = 12$  V,  $V_{SS} = -12$  V,  $T_A = 25^\circ\text{C}$  (see Figure 3)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$ Propagation delay time, low- to high-level output	$R_L = 3$ k $\Omega$ to 7 k $\Omega$ , $C_L = 15$ pF		315	500	ns
$t_{PHL}$ Propagation delay time, high- to low-level output	$R_L = 3$ k $\Omega$ to 7 k $\Omega$ , $C_L = 15$ pF		75	175	ns
$t_{TLH}$ Transition time, low- to high-level output	$R_L = 3$ k $\Omega$ to 7 k $\Omega$	$C_L = 15$ pF	60	100	ns
		$C_L = 2500$ pF <sup>(1)</sup>	1.7	2.5	$\mu$ s
$t_{THL}$ Transition time, high- to low-level output	$R_L = 3$ k $\Omega$ to 7 k $\Omega$	$C_L = 15$ pF	40	75	ns
		$C_L = 2500$ pF <sup>(2)</sup>	1.5	2.5	$\mu$ s

- (1) Measured between -3-V and 3-V points of the output waveform (TIA/EIA-232-F conditions); all unused inputs are tied either high or low.
- (2) Measured between 3-V and -3-V points of the output waveform (TIA/EIA-232-F conditions); all unused inputs are tied either high or low.

## RECEIVER SECTION

### Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>T+</sub>	Positive-going threshold voltage	See Figure 5	T <sub>A</sub> = 25°C	1.75	1.9	2.3	V
			T <sub>A</sub> = 0°C to 70°C	1.55		2.3	
V <sub>T-</sub>	Negative-going threshold voltage			0.75	0.97	1.25	V
V <sub>hys</sub>	Input hysteresis (V <sub>T+</sub> – V <sub>T-</sub> )			0.5			V
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = –0.5 mA	V <sub>IH</sub> = 0.75 V	2.6	4	5	V
			Inputs open	2.6			
V <sub>OL</sub>	Low-level input voltage	I <sub>OL</sub> = 10 mA	V <sub>I</sub> = 3 V		0.2	0.45	V
I <sub>IH</sub>	High-level input current	V <sub>I</sub> = 25 V,	See Figure 5	3.6		8.3	mA
		V <sub>I</sub> = 3 V,	See Figure 5	0.43			
I <sub>IL</sub>	Low-level output current	V <sub>I</sub> = –25 V,	See Figure 5	–3.6		–8.3	mA
		V <sub>I</sub> = –3 V,	See Figure 5	–0.43			
I <sub>os</sub>	Short-circuit output current	See Figure 4			–3.4	–12	mA

(1) All typical values are at T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5 V, V<sub>DD</sub> = 9 V, and V<sub>SS</sub> = –9 V.

### Switching Characteristics

V<sub>CC</sub> = 5 V, V<sub>DD</sub> = 12 V, V<sub>SS</sub> = –12 V, T<sub>A</sub> = 25°C (see Figure 6)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	Propagation delay time, low- to high-level output	C <sub>L</sub> = 50 pF,	R <sub>L</sub> = 5 kΩ		107	500	ns
t <sub>PHL</sub>	Propagation delay time, high- to low-level output	C <sub>L</sub> = 50 pF,	R <sub>L</sub> = 5 kΩ		42	150	ns
t <sub>TLH</sub>	Transition time, low- to high-level output	C <sub>L</sub> = 50 pF,	R <sub>L</sub> = 5 kΩ		175	525	ns
t <sub>THL</sub>	Transition time, high- to low-level output	C <sub>L</sub> = 50 pF,	R <sub>L</sub> = 5 kΩ		16	60	ns

PARAMETER MEASUREMENT INFORMATION

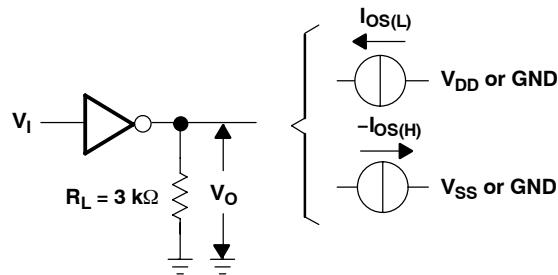


Figure 1. Driver Test Circuit for  $V_{OH}$ ,  $V_{OL}$ ,  $I_{OS(H)}$ , and  $I_{OS(L)}$

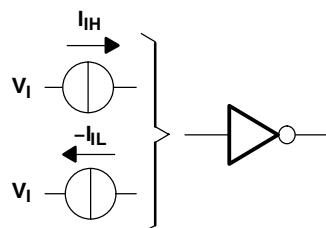


Figure 2. Driver Test Circuit for  $I_{IH}$  and  $I_{IL}$

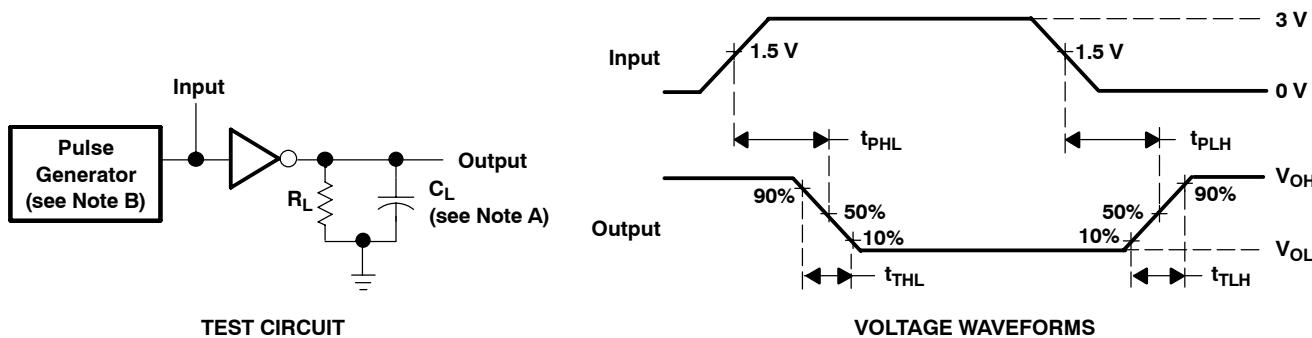


Figure 3. Driver Test Circuit and Voltage Waveforms

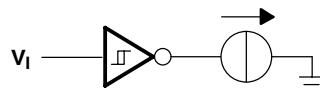


Figure 4. Receiver Test Circuit for  $I_{OS}$

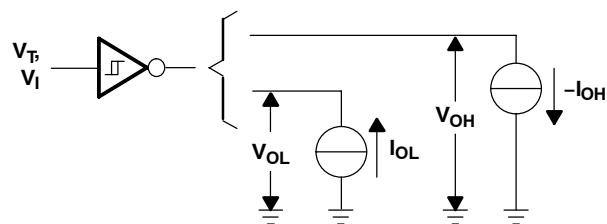
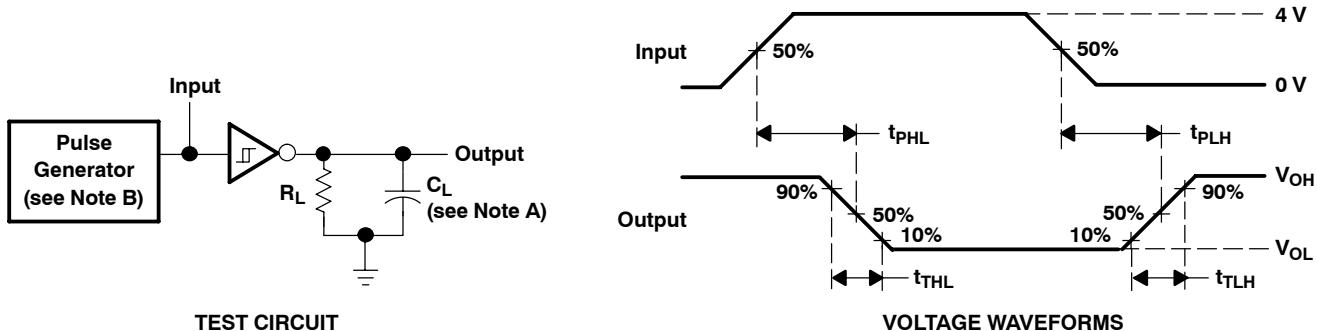


Figure 5. Receiver Test Circuit for  $V_T$ ,  $V_{OH}$ , and  $V_{OL}$

PARAMETER MEASUREMENT INFORMATION (continued)



- A.  $C_L$  includes probe and jig capacitance.
- B. The pulse generator has the following characteristics:  $t_w = 25 \mu s$ , PRR = 20 kHz,  $Z_O = 50 \Omega$ ,  $t_r = t_f < 50 \text{ ns}$ .

Figure 6. Receiver Propagation and Transition Times

TYPICAL CHARACTERISTICS

DRIVER SECTION

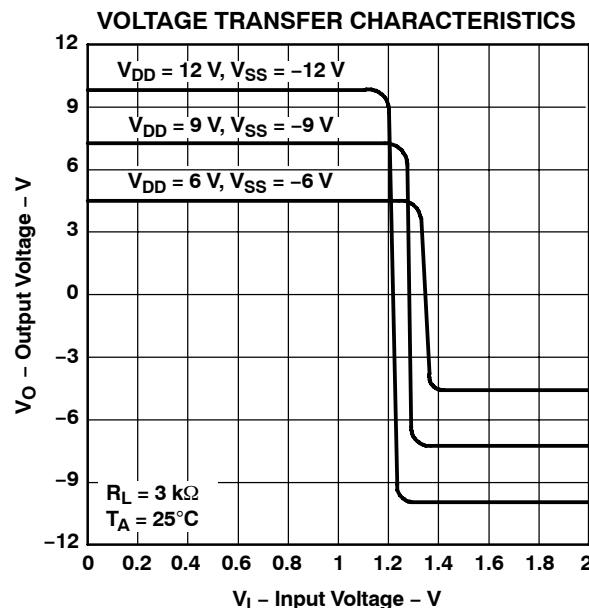


Figure 7.

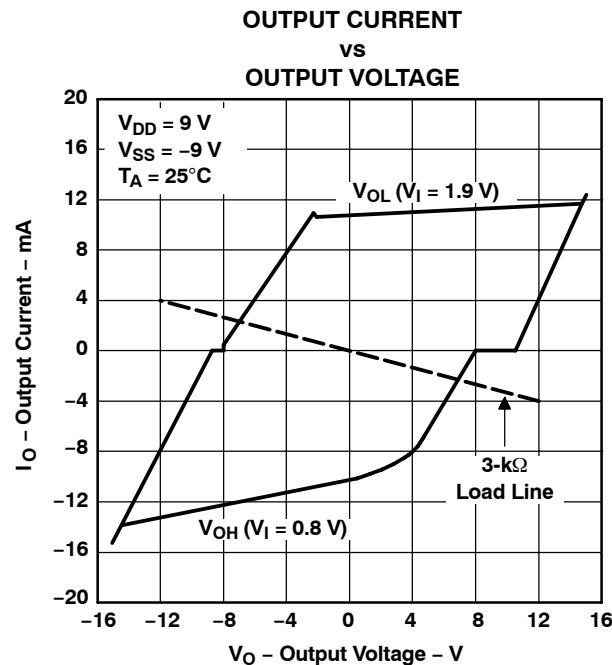


Figure 8.

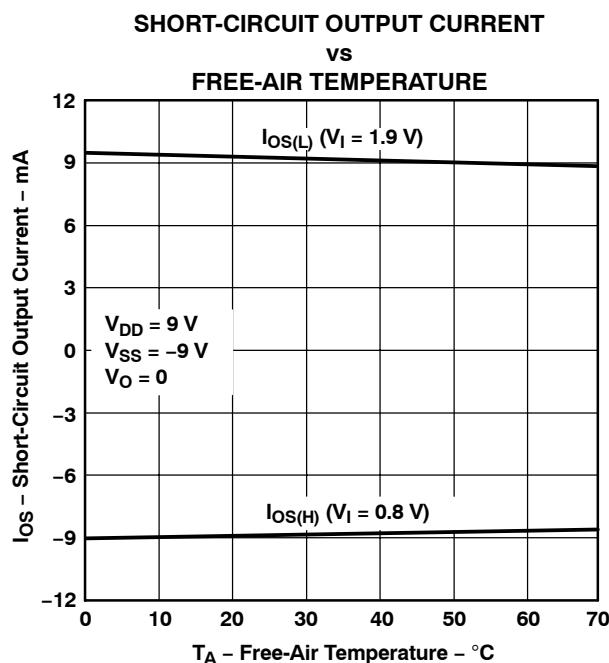


Figure 9.

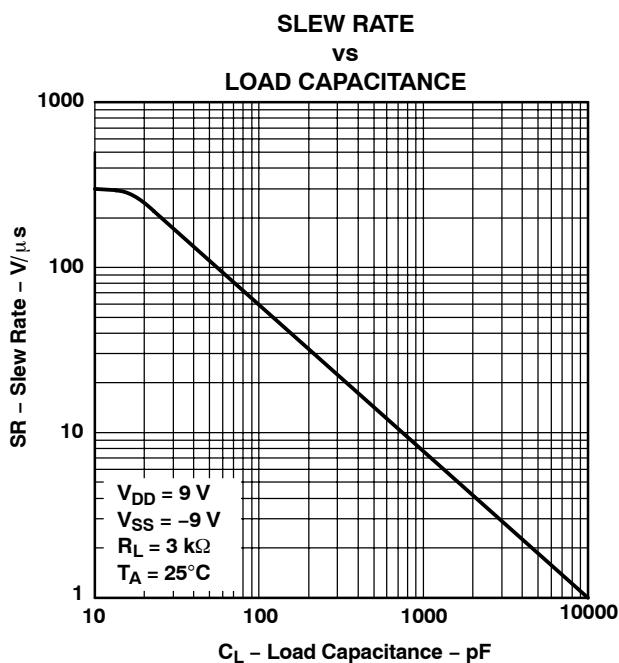


Figure 10.

## TYPICAL CHARACTERISTICS

### RECEIVER SECTION

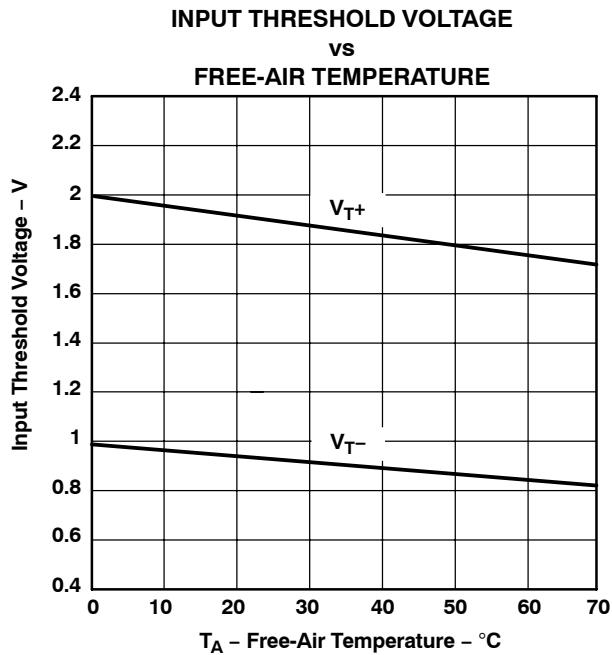


Figure 11.

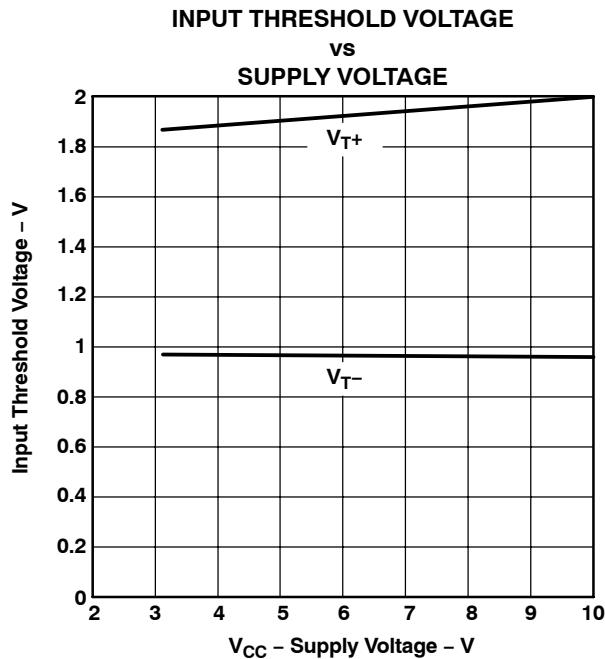
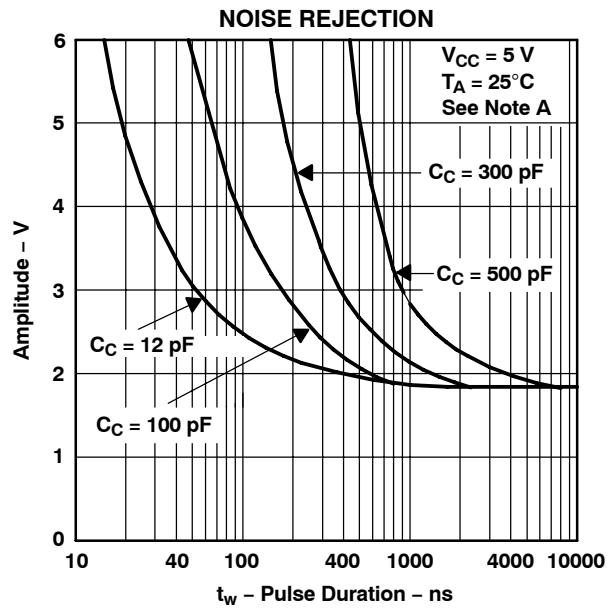


Figure 12.



NOTE A: This figure shows the maximum amplitude of a positive-going pulse that, starting from 0 V, will not cause a change in the output level.

Figure 13.

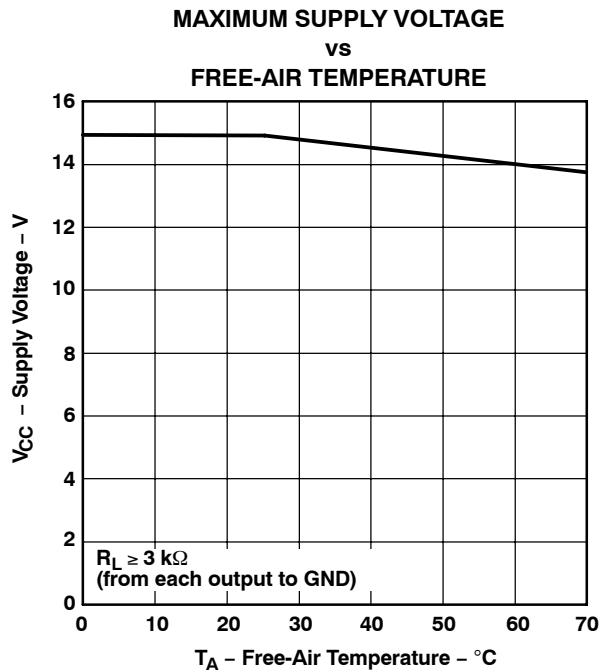
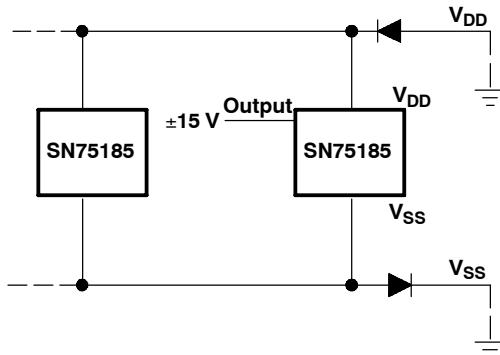


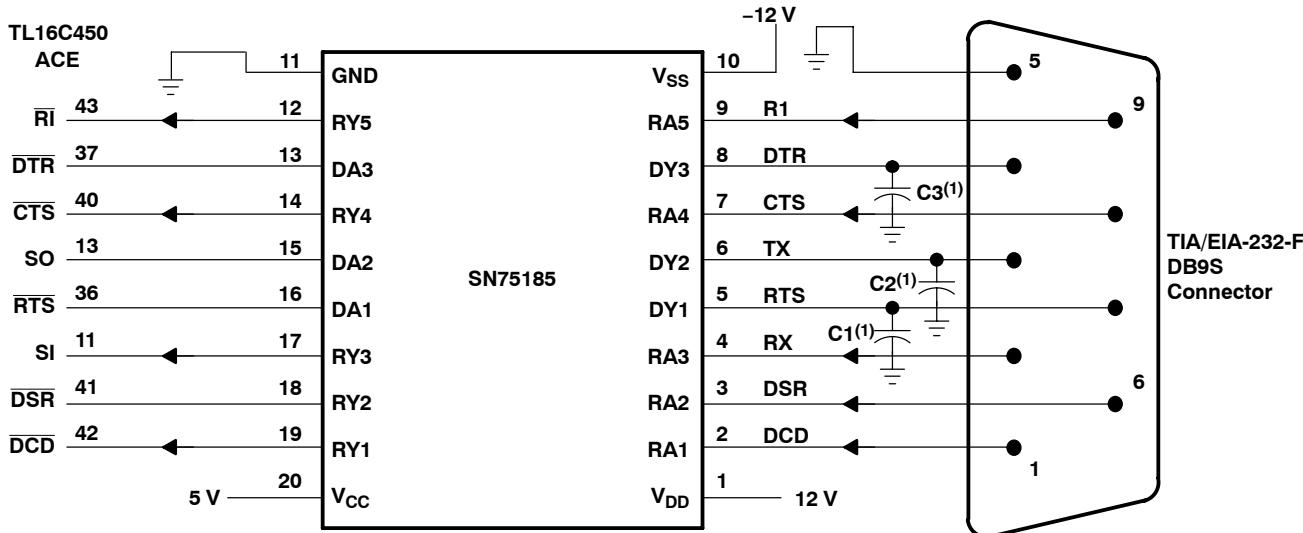
Figure 14.

## APPLICATION INFORMATION

Diodes placed in series with the  $V_{DD}$  and  $V_{SS}$  leads protect the SN75185 in the fault condition. In the fault condition, the device outputs are shorted to  $\pm 15$  V, and the power supplies are at low and provide low-impedance paths to ground (see Figure 15).



**Figure 15. Power-Supply Protection to Meet Power-Off Fault Conditions of TIA/EIA-232-F**



(1) See Figure 10 to select the correct values for the loading capacitors ( $C_1$ ,  $C_2$ , and  $C_3$ ), which are required to meet the RS-232 maximum slew-rate requirement of  $30 \text{ V}/\mu\text{s}$ . The value of the loading capacitors required depends on the line length and desired slew rate, but typically is  $330 \text{ pF}$ .

**Figure 16. Typical Connection**

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75185DB	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	A185	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN75185DBE4	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	A185	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN75185DBG4	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	A185	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN75185DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	A185	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN75185DBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	A185	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN75185DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75185	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN75185DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75185	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN75185DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75185	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN75185DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75185	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN75185DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75185	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN75185DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75185	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN75185N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75185N	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN75185NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75185N	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN75185PWG4	OBsolete	TSSOP	PW	20		TBD	Call TI	Call TI	0 to 70	A185	
SN75185PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	A185	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN75185PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	A185	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

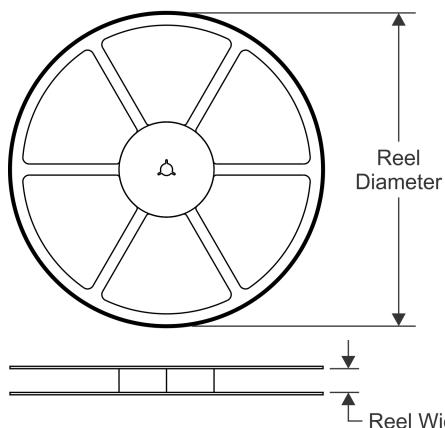
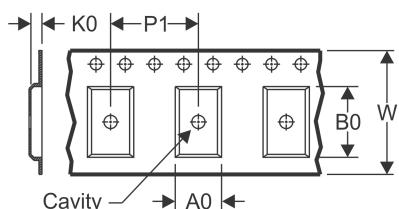
**(3)** MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

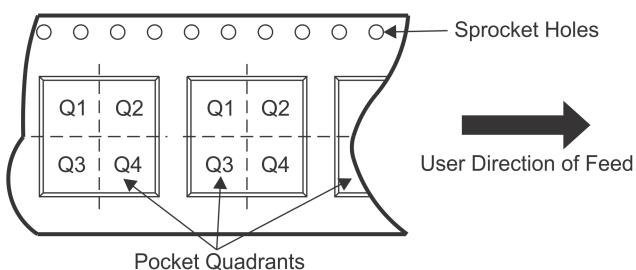
**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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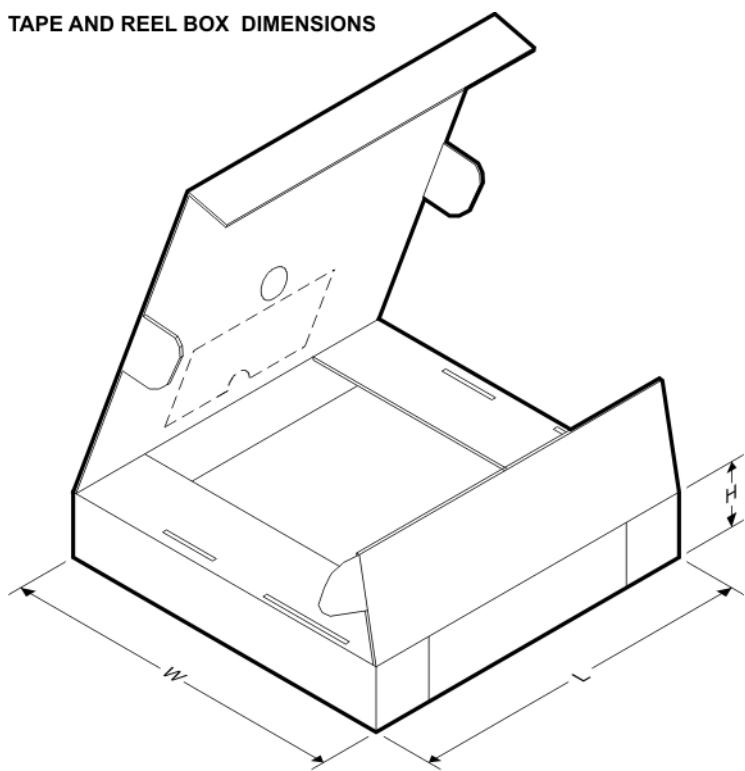
**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75185DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN75185DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN75185DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN75185PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75185DBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN75185DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN75185DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN75185PWR	TSSOP	PW	20	2000	367.0	367.0	38.0

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



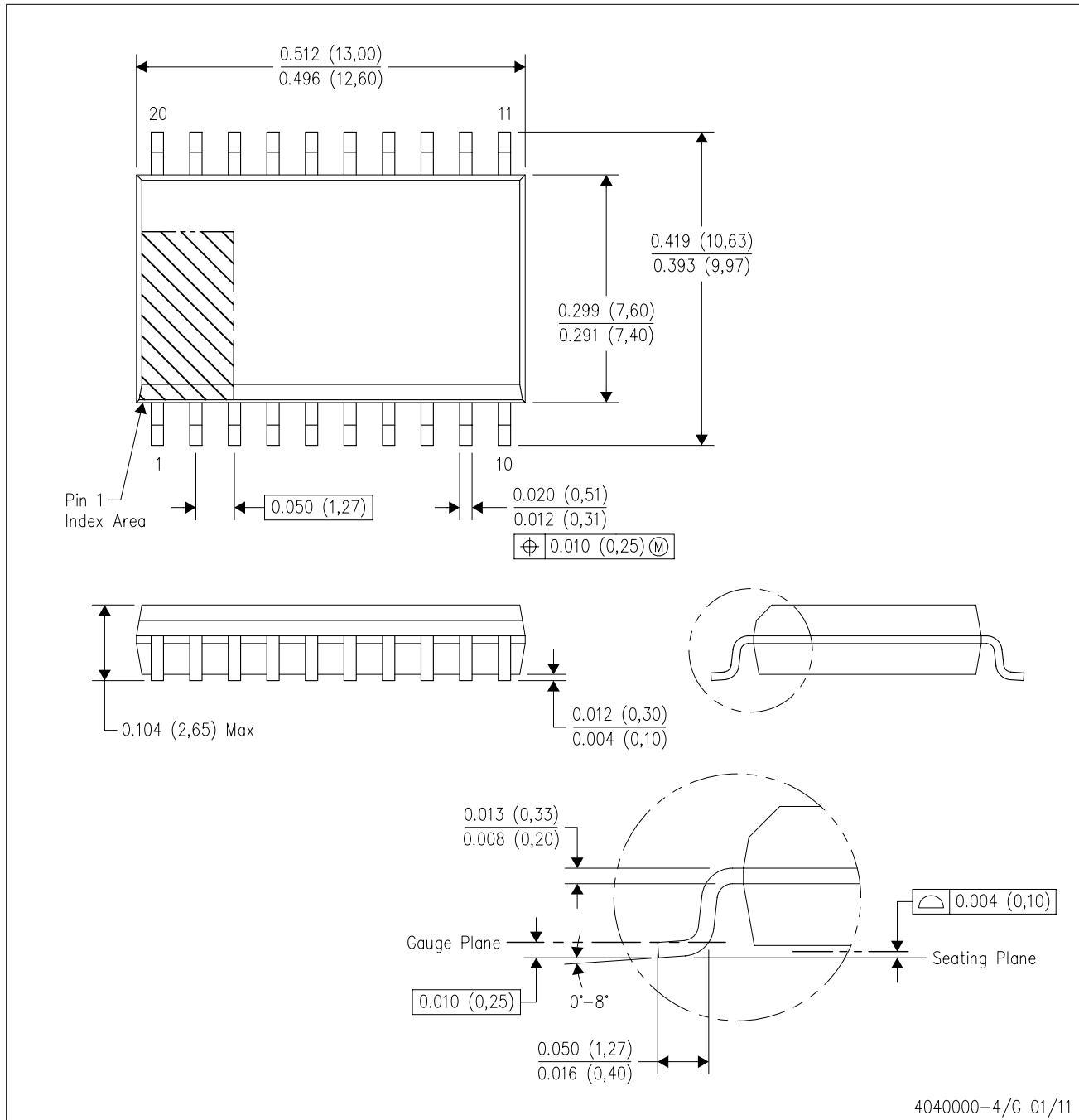
NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

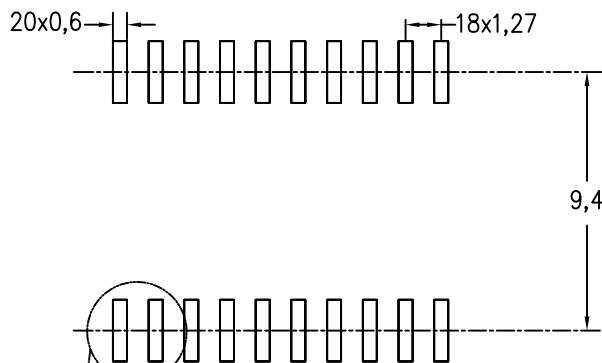
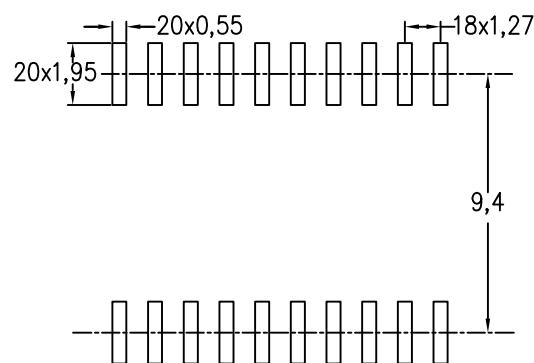


NOTES:

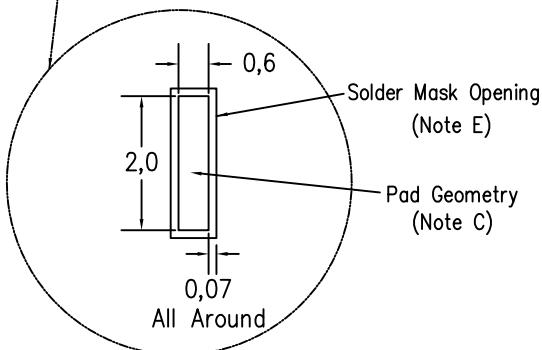
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
- Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

Example Board Layout  
(Note C)Stencil Openings  
(Note D)

Non Solder Mask Define Pad



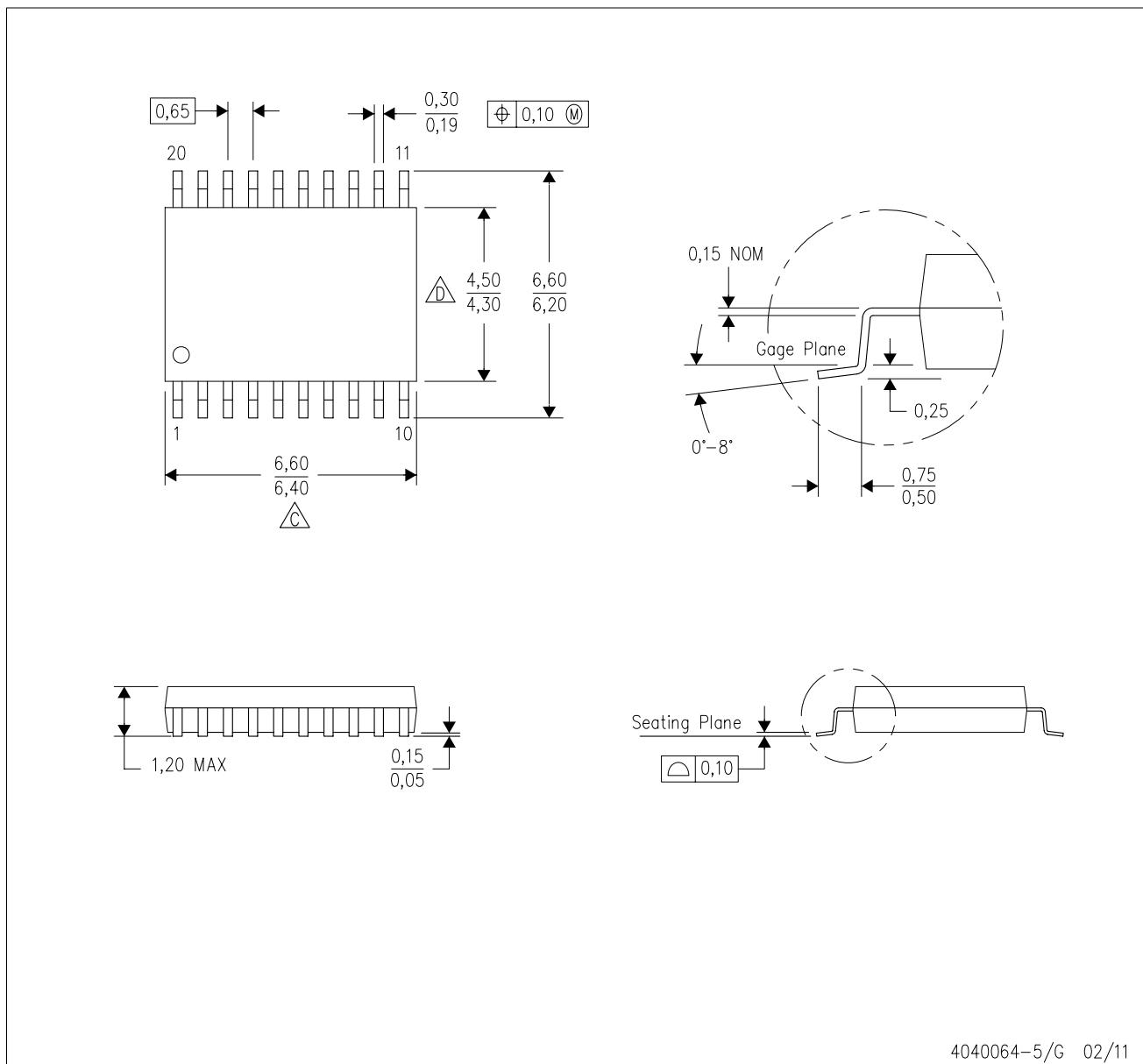
4209202-4/F 08/13

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Refer to IPC7351 for alternate board design.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

 D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153

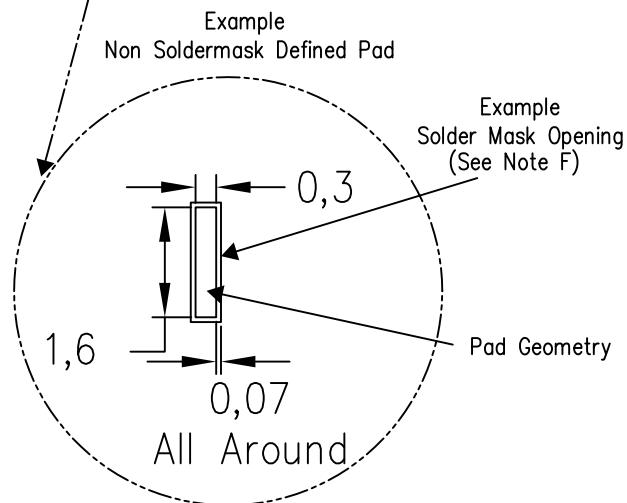
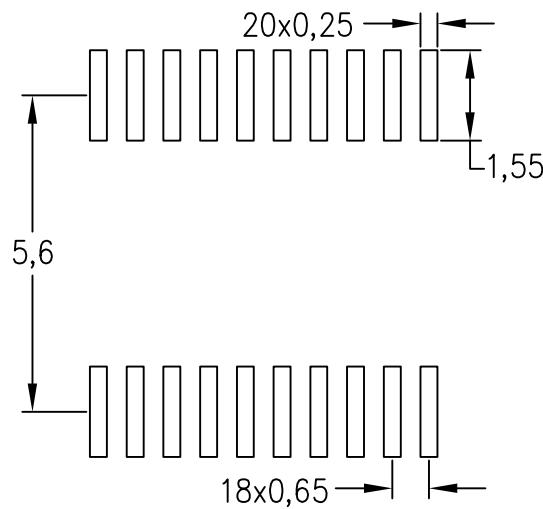
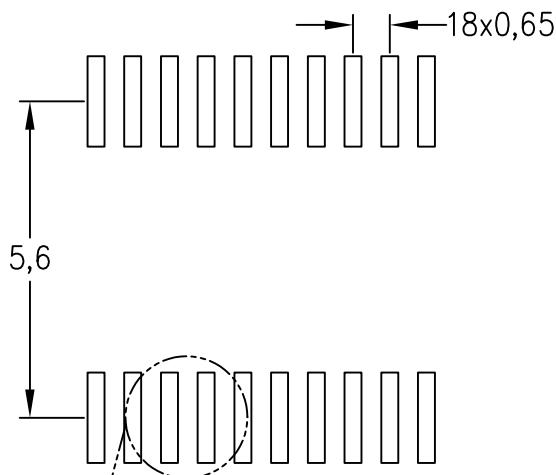
4040064-5/G 02/11

## PW (R-PDSO-G20)

## PLASTIC SMALL OUTLINE

## Example Board Layout

Based on a stencil thickness  
of .127mm (.005inch).



4211284-5/F 12/12

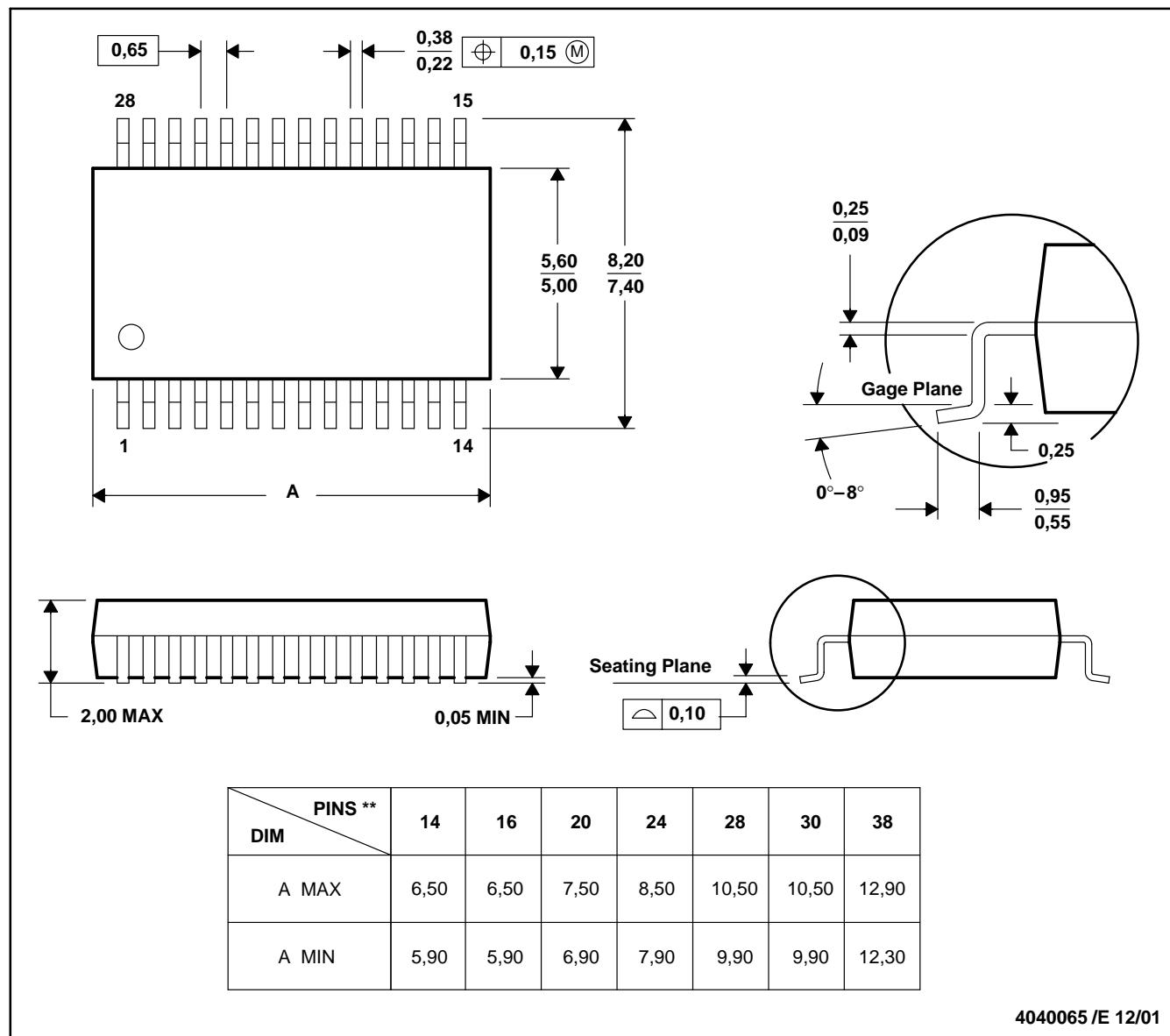
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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