High-performance Video Signal Switchers

Ultra Wide Band Triple Circuits Video Signal Switchers

BA7657F,BH7659FS

No.11066EAT03

●Description

The BA7657F, and BH7659FS are ICs that have been developed for use in PC monitors, HDTVs (high definition televisions), and other high-resolution display devices. In addition to their wide-range switching circuits for RGB signals, HD signals, and VD signals, the A7657F feature a separation (BUNRI) circuit for the synchronization signal that is superposed on the G signal, while the BH7659FS features an on-chip switch for I^2C bus signals (SDA and SCL). These ICs can be used to simplify the input block configuration in advanced display devices.

●Features

1) Operates on 5 V single power supply.
2) Built-in wide-range RGB signal switches. (BA7657F :fc = 230 MHz)
   (BH7659FS:fc = 250 MHz)
3) Built-in switching circuit for HD signal and VD signal.
4) Built-in separation (BUNRI) circuit for synchronization signal superposed on G signal. (BA7657F)
5) Built-in switch for I^2C bus signals (SDA and SCL). (BH7659FS)
6) Built-in power saving function. (BH7659FS)

●Applications

PC monitors, Plasma displays, LCD monitors, and Other devices that use wide-range RGB signal switching.

●Line up matrix

Parameter	BA7657F	BH7659FS
Circuit current (mA)	35	25
Circuit current during low-power mode (mA)	—	14
RGB signal SW block frequency characteristics (MHz)	230	250
Synchronization signal SW block circuit configuration	2 digital switching circuits	4 CMOS analog switching circuits
Synchronization signal separation circuit	✔	—
Package	SOP24	SSOP-A32

●Absolute Maximum Ratings(Ta=25℃)

Parameter		Symbol	Ratings	Unit
Supply voltage		VCC	8.0	V
Power dissipation	BA7657F	Pd	550	mW
	BH7659FS		800	
Operating temperature		Topr	-25～+75	℃
Storage temperature		Tstg	-55～+125	℃

※Deratings is done at 5.5mW/℃ (BA7657F), 8mW/℃ (BA7659FS) above Ta=25℃.

●Operating Range(Ta=25℃)

Parameter	Symbol	Ratings			Unit
		Min.	Typ.	Max.	
Supply voltage	VCC	4.5	5.0	5.5	V

※This product is not designed for protection against radioactive rays.

●Electrical characteristics

○BA7657F(Unless otherwise noted, Ta=25℃, Vcc=5.0V)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Circuit current	ICC	20	35	50	mA	—
〈Analog SW block〉						
Maximum output level	Vom	2.8	—	—	V_{P-P}	f=1kHz
Voltage gain	G_V	-1.0	-0.5	0	dB	f=1MHz,V_{IN}=1V_{P-P}
Input pin voltage gain differential	$\triangle G_{VI}$	-0.2	0	0.2	dB	f=1MHz,V_{IN}=1V_{P-P}
Inter block voltage gain differential	G_{VB}	-0.2	0	0.2	dB	f=1MHz,V_{IN}=1V_{P-P}
Input pin cross talk1	CTI1	—	-50	-40	dB	f=10MHz,V_{IN}=1V_{P-P}
Interblock crosstalk1	CTB1	—	-50	-40	dB	f=10MHz,V_{IN}=1V_{P-P}
〈Digital SW block〉						
“H” level input voltage	V_{IH}	1.8	—	—	V	—
“L” level input voltage	V_{IL}	—	—	1.2	V	—
“H” level input current	I_{IH}	80	100	130	μA	V_{IN}=5.0V
“L” level input current	I_{IL}	-3	-1	—	μA	V_{IN}=0V
Rise time	T_R	—	30	50	ns	—
Fall time	T_F	—	30	50	ns	—
Rise delay time	T_{RD}	—	50	80	ns	—
Fall delay time	T_{FD}	—	30	50	ns	—
“H” level output voltage	V_{OH}	3.0	3.7	—	V	—
“L” level output voltage	V_{OL}	—	0.2	0.4	V	—
“H” level output current	I_{OH}	-400	—	—	μA	—
“L” level output current	I_{OL}	5	—	—	mA	—
〈Synchronization signal separation block〉						
Minimum SYNC separation level	$V_{SMin.}$	-50	—	50	mV_{P-P}	—
“H” level output voltage	V_{OH}	4.5	5.0	—	V	—
“L” level output voltage	V_{OL}	—	0.2	0.5	V	—
“L” level output current	I_{OL}	2	—	—	mA	—
Rise time	T_R	—	80	130	ns	—
Fall time	T_F	—	30	80	ns	—
Rise delay time	T_{RD}	—	100	150	ns	—
Fall delay time	T_{FD}	—	100	150	ns	—
〈Control block〉						
“H” level input voltage	V_{IH}	1.8	—	—	V	—
“L” level input voltage	V_{IL}	—	—	1.2	V	—
“H” level input current	I_{IH}	80	100	130	μA	—
“L” level input current	I_{IL}	-3	-1	—	μA	—

○**BH7659FS**(Unless otherwise noted, Ta=25℃, Vcc=5.0V)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
〈Entire device〉						
Circuit current	ICC	15	25	35	mA	—
Circuit current during power save	IPSV	7	14	22	mA	PS="H"
〈R,G,B video SW〉						
Voltage gain	GV	-1.0	-0.5	0	dB	f=10MHz
Interchannel relative gain	△GVC	-0.5	0	0.5	dB	f=10MHz
Interblock relative gain	△GVB	-0.5	0	0.5	dB	f=10MHz
Output dynamic range	VOM	2.6	—	—	VP-P	f=1kHz
〈C-MOS analog SW〉						
On-resistance	RON	—	200	400	Ω	VIN=2.5V
Interchannel ON resistance differential	△RON	—	20	40	Ω	VIN=2.5V
Interchannel cross talk	CT	—	-70	-55	dB	f=150kHz
Transmission delay time	tD	—	20	—	ns	RL=100Ω,CL=50pF
〈Control block〉						
"H" level voltage	VH	3.5	—	—	V	—
"L" level voltage	VL	—	—	1.5	V	—

●Guaranteed design parameters

○BA7657F(Unless otherwise noted, Ta=25℃, Vcc=5.0V)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
〈Analog SW block〉						
Input pin cross talk 2	CTI2	—	-30	-15	dB	f=230kHz, V_{IN}=1V_{P-P}
Interblock cross talk 2	CTB2	—	-30	-15	dB	f=230MHz,V_{IN}=1V_{P-P}
Frequency characteristic	Gf	-6	-3	-1	dB	f=1MHz/230MHz, V_{IN}=1V_{P-P}
Input pin frequency differential	△GfI	-1	0	+1	dB	f=1MHz/100MHz, V_{IN}=1V_{P-P}
Interblock frequency characteristic differential	△GfB	-1	0	+1	dB	f=1MHz/100MHz, V_{IN}=1V_{P-P}
〈SYNC separation block〉						
SYNC separation frequency	fH-R	200	—	—	kHz	Input waveform ※1
SYNC separation pulse width 1	pwH1	3.0	—	—	μs	Input waveform ※2 fH=20kHz
SYNC separation pulse width 2	pwH2	0.5	—	—	μs	Input waveform ※2 fH=100kHz
SYNC separation pulse width 3	pwH3	0.3	—	—	μs	Input waveform ※2 fH=200kHz
SYNC separation level 1	VS1	300	—	—	μs	Input waveform ※3 fH=20kHz
SYNC separation level 2	VS2	100	—	—	μs	Input waveform ※3 fH=100kHz
SYNC separation level 3	VS3	60	—	—	μs	Input waveform ※3 fH=200kHz

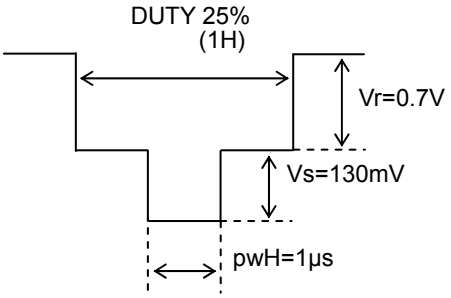
〈Input waveform〉

※1 VS and pwH are variable. VS and pwH are inter-related. See the characteristics diagram.

※2 VS = 130 mW and pwH are variable.

※3 pwH = 1 μs and VS are variable.

Period of horizontal synchronization signal



○BH7659FS(Unless otherwise noted, Ta=25℃, Vcc=5.0V)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
〈R/G/B video SW〉						
Frequency characteristics 1	f_1	-3.0	0	+1.0	dB	f=50MHz
Frequency characteristics 2	f_2	-6.0	-3	-1.0	dB	f=250MHz
Interchannel relative frequency characteristics	△f_C	-0.5	0	0.5	dB	f=50MHz
Interblock relative frequency characteristics	△f_B	-0.5	0	0.5	dB	f=50MHz
Interchannel cross talk 1	CT_{C1}	—	-50	-35	dB	f=50kHz
Interchannel cross talk 2	CT_{C2}	—	-30	-15	dB	f=250MHz
Interblock cross talk 1	CT_{B1}	—	-50	-35	dB	f=50MHz
Interblock cross talk 2	CT_{B2}	—	-30	-15	dB	f=250MHz

●Block diagram

○BA7657F

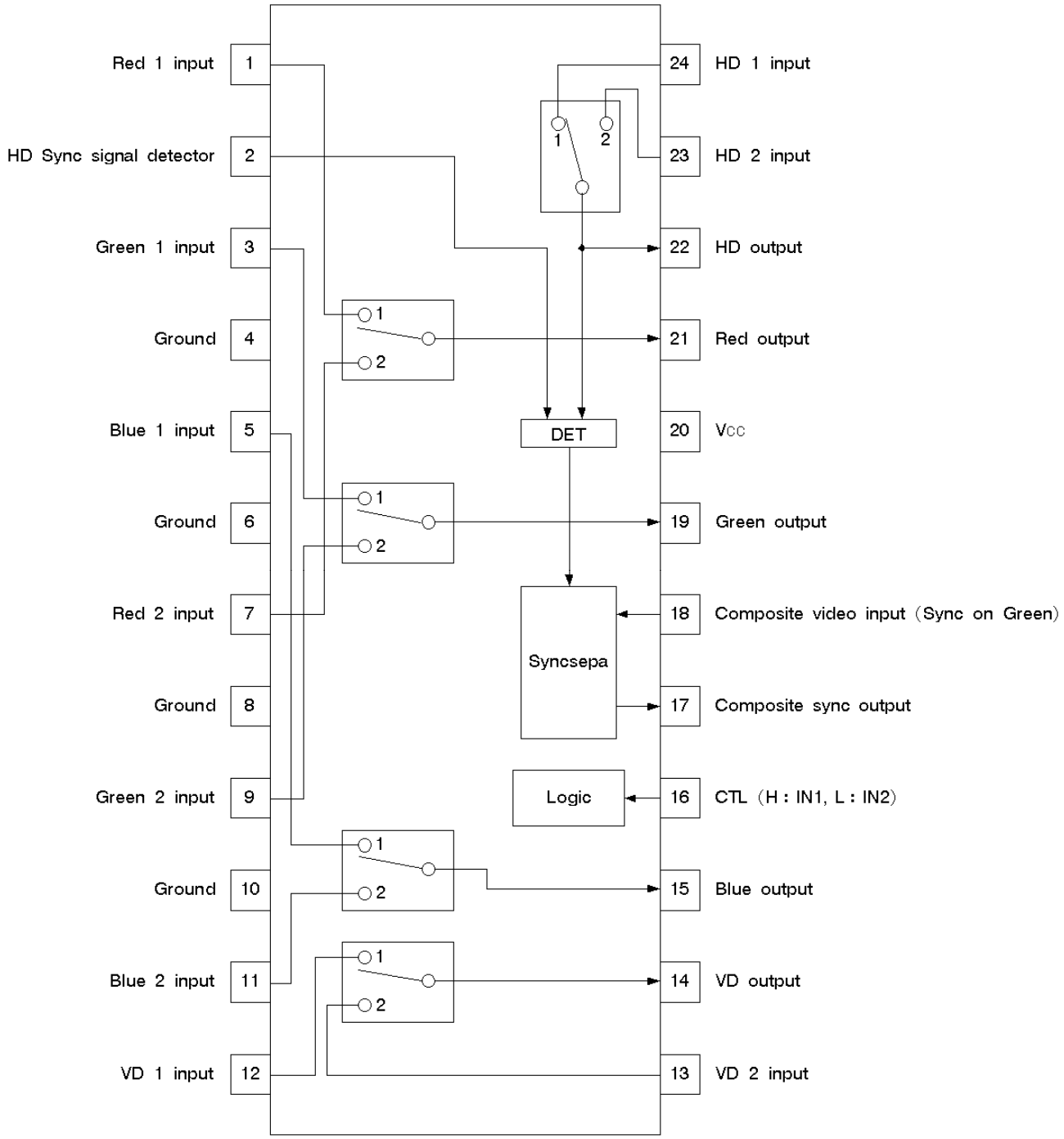


Fig.1

○BH7659FS

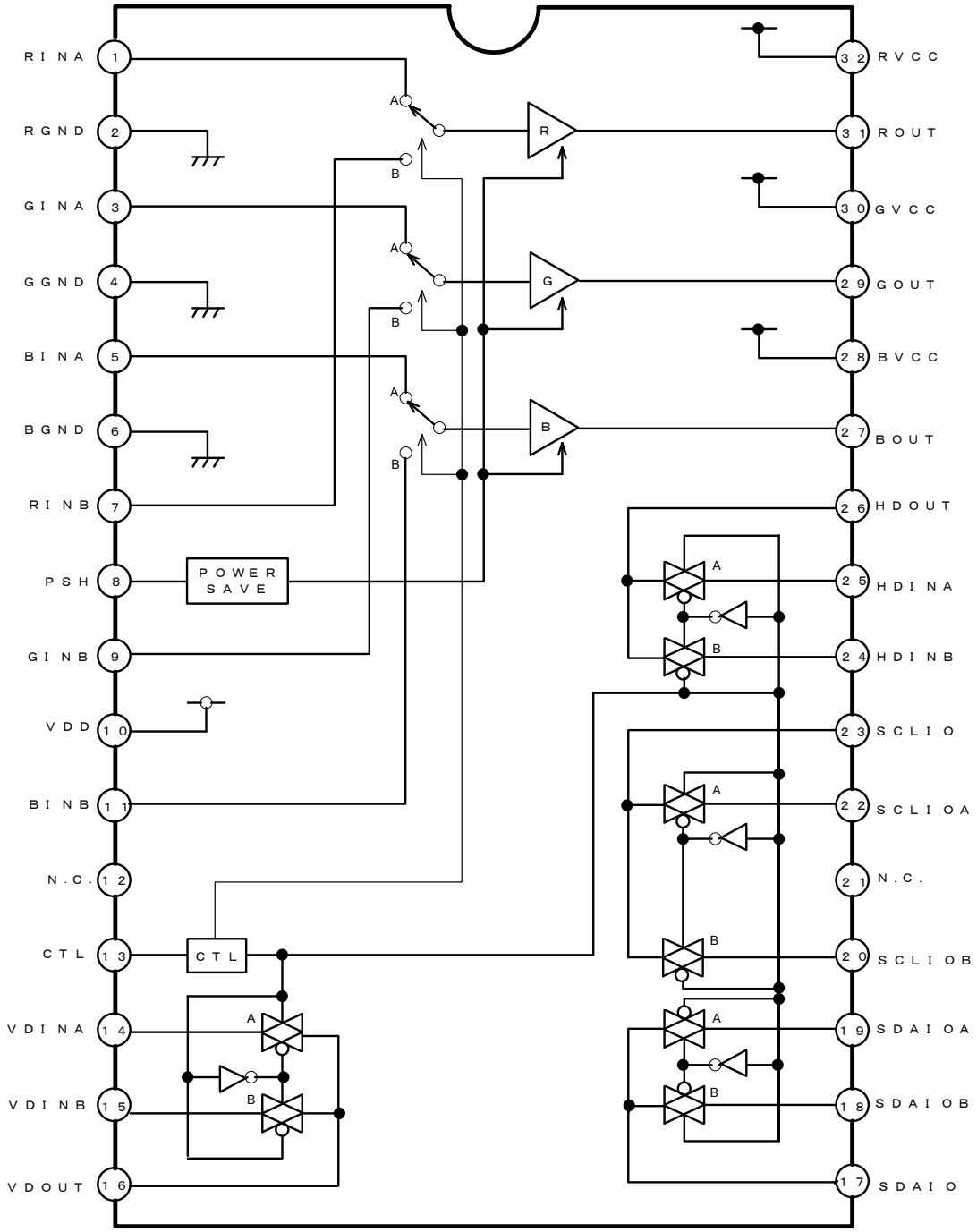
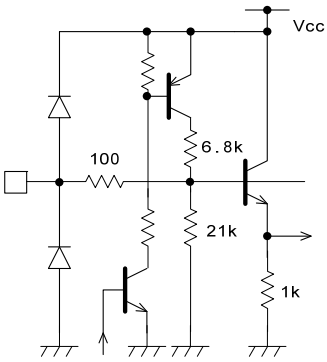
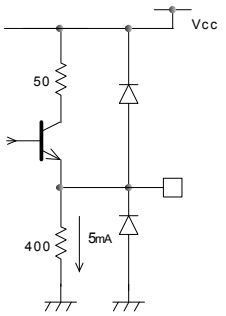
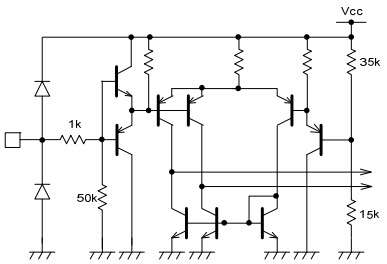
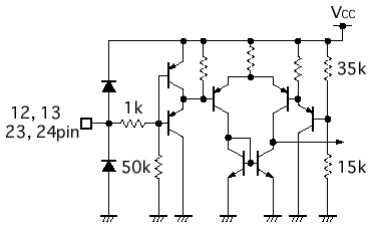
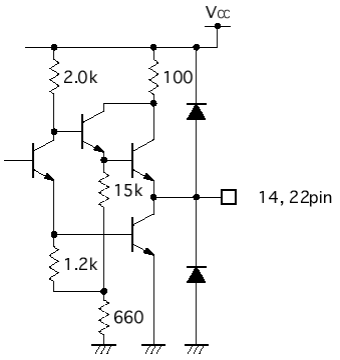


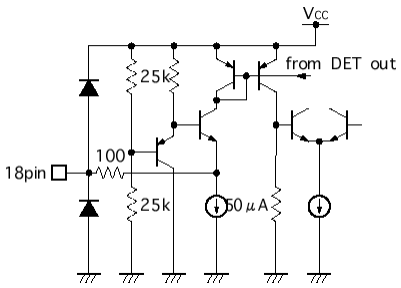
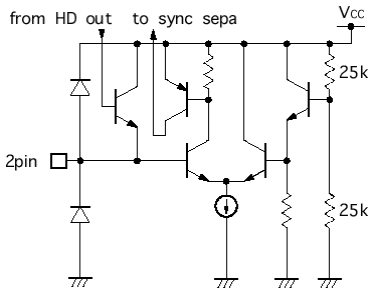
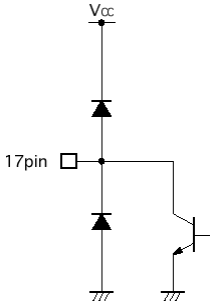
Fig.2

●Pin descriptions (BA7657F)

○BA7657F

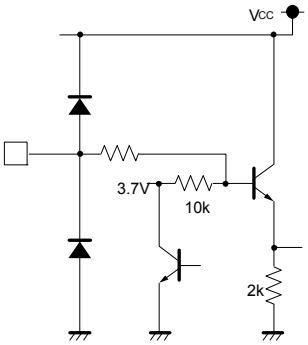
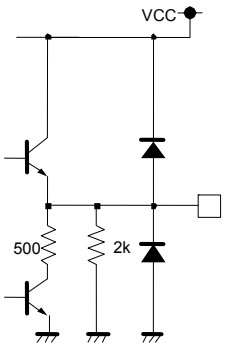
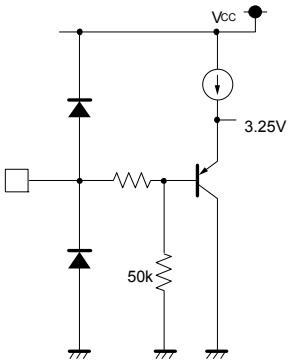
Pin No.	Pin name	Reference potential	Equivalent circuit	Function
1 3 5 7 9 11	Red1 Input Green1 Input Blue1 Input Red2 Input Green2 Input Blue2 Input	3.7V when selected 0V when not selected		2-channel switching of R, G, and B signals. Select between: CTL: H input1 CTL: L input2
15 19 21	Blue output Green output Red output	2.0V		Output pins for RGB signals. Insert resistance from 100 to 300 Ω near the pins to suppress f peaks at high frequencies.
16	Control	H≧1.8V L≦1.2V		CTL pins Select between: CTL: H input1 CTL: L input2
12 13 23 24	VD1 input VD2 input HD2 input HD1 input	H≧1.8V L≦1.2V		2-channel switching of VD and HD signals. Select between: CTL: H input1 CTL: L input2
14 22	VD output HD output	VOH≧3.0V VOL≦10.5V		Output pins for vertical synchronization signal (VD) And horizontal synchronization signal (HD).

○BA7657F

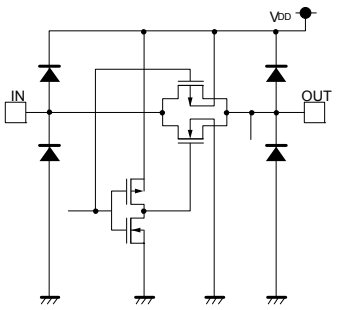
Pin No.	Pin name	Reference potential	Equivalent circuit	Function
18	Composite Video input	2.5V		Input pin for composite signal (Sync on Green).
2	HD Sync Signal detector	—		This pin is used to detect whether or not the HD signal is being input. When the HD signal is being input, the synchronization signal separation circuit is stopped.
17	Composite sync output	—		Synchronization signal output pin Synchronization separation is performed for the input signal from pin 18 if the HD signal is not being input.
20	Vcc	5V	—	Insert a decoupling capacitor near the pin.
4 6 8	GND	0V	—	Use as large a GND pattern area as possible.

●Pin descriptions (BH7659FS)

○BH7659FS

Pin NO	Pin name	Reference potential	Equivalent circuit	Function
1 3 5 7 9 11	R chroma signal input pin A (RINA) G chroma signal input pin A (GINA) B chroma signal input pin A (BINA) R chroma signal input pin B (RINB) G chroma signal input pin B (GINB) B chroma signal input pin B (BINB)	3.5V when selected 0V when not selected		RGB signals are switched in two channels. When selected by SW, the DC potential is approximately 3.5V, and when not selected, the DC potential is about 0 V.
27 29 31	B chroma signal input pin (BOUT) G chroma signal input pin (GOUT) R chroma signal input pin (ROUT)	1.85V		Power save function is used when PSH pin is set to high level.
8 13	Power save input pin (PSH) Control input pin (CTL)	0V		PSH Pin Power save off ≦1.5V Power save on ≧3.5V CTL Pin Input A≧3.5V Input B≦1.5V

○BH7659FS

Pin No.	Pin name	Reference potential	Equivalent circuit	Function
14 15 16 17 18 19 20 22 23 24 25 26	V_D signal input pin A (V_DINA) V_D signal input pin B (V_DINB) VD signal output pin (VDOUT) SDA signal output pin (SDAIO) SDA signal input pin B (SDAIOB) SDA signal input pin A (SDAIOA) SCL signal input pin B (SCLIOB) SCL signal input pin A (SCLIOA) SCL signal output pin (SCLIO) HD signal input pin B (HDINB) HD signal input pin A (HDINA) HD signal output pin (HDOUT)	0V		V_D, H_D, SDA, and SCL are switched in two channels. Bidirectional access (I/O) is enabled by the CMOS analog SW.
2	R GND pin (RGND)	0V	—	This is the GND pin for the R video SW block.
4	G GND pin (GGND)	0V	—	This is the GND pin for the B video SW block.
6	B GND pin (BGND)	0V	—	This is the GND pin for the G video SW block , C-MOS SW block.
10	C-MOS supply voltage pin (V_{DD})	5V	—	This is the V_{DD} pin for the C-MOS SW block.
28	B supply voltage pin (BV_{CC})	5V	—	This is the Vcc pin for the B video SW block
30	G supply voltage pin (GV_{CC})	5V	—	This is the Vcc pin for the G video SW block
32	R supply voltage pin (RV_{CC})	5V	—	This is the Vcc pin for the R video SW block

●Description of operations

○BA7657F

1) Analog SW block
Two channels of RGB signals can be switched. IN1 can be selected when high-level voltage is applied to the CTL pin, and IN2 can be selected when low level voltage is applied.

2) Digital SW block
This block switches between two channels of HD and VD ynchronization signals. HD and VD synchronization signals are output for IN1 when high-level voltage is applied to the CTL pin, and these signals are output for IN2 when a low-level voltage is applied to the CTL pin.

3) Synchronization signal separation block
This block separates composite signals (Sync on Green) and synchronization signals and outputs positive-electrode composite synchronization signals. When an HD signal is being input, the synchronization signal detector operates and stops the synchronization signal separation circuit. A low-level output voltage is used for output. The time at which the synchronization signal separation circuit will be stopped can be set using external time constants for the circuit detection pin.

I/O relations

Input			Output		
HD	VD	Sync on Green	HD	VD	Composite Sync
–	–	○	–	–	○
○	–	○	○	–	–
–	○	○	–	○	○
○	○	○	○	○	–
○	–	–	○	–	–
–	○	–	–	○	–
○	○	–	○	○	–

○BH7659FS

1) Analog SW block
R, G, and B chroma signals are switched in two channels. INA is selected by applying a high-level voltage to the CTL pin, and INB is selected by applying a low-level voltage. When the power save pin (pin 8) is set to high level, the current to the SW block's output transistors is reduced to lower the circuit current. Even during low power mode, signal switching can be performed normally as long as there is no drop in frequency characteristics.

2) CMOS analog SW block
SDA and SDC signals are switched via an I^2C bus to handle two channels of HD and VD synchronization signals, and to exchange information bidirectional between a computer and a monitor. The switching circuits used by this IC handle are configured as CMOS analog switches in order to handle I^2C BUS signals and to transmit input and output signals bidirectional. (ON resistance: Ron 200 Ω typ.)

●Application circuit

○BA7657F

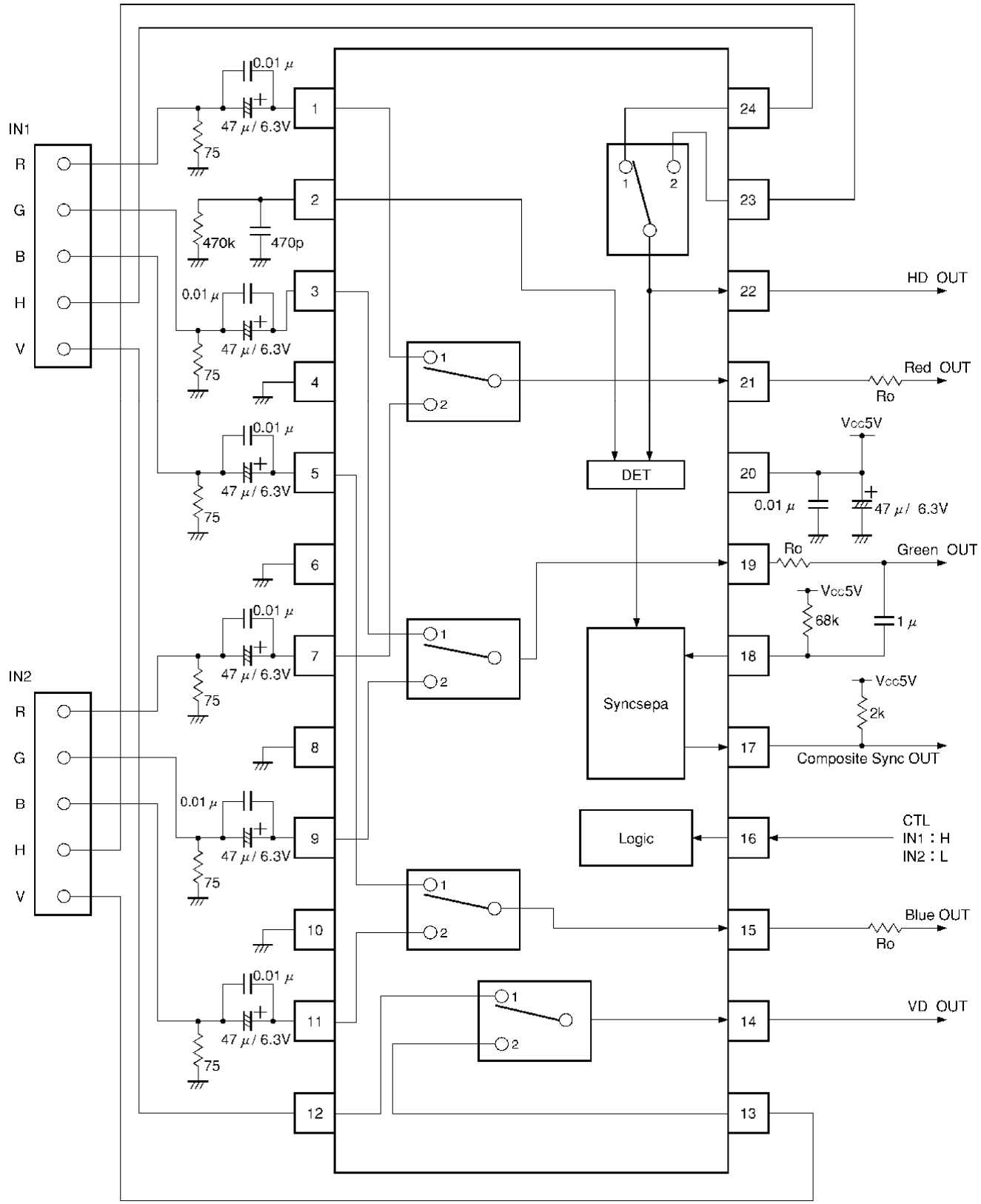


Fig.3

○BH7659FS

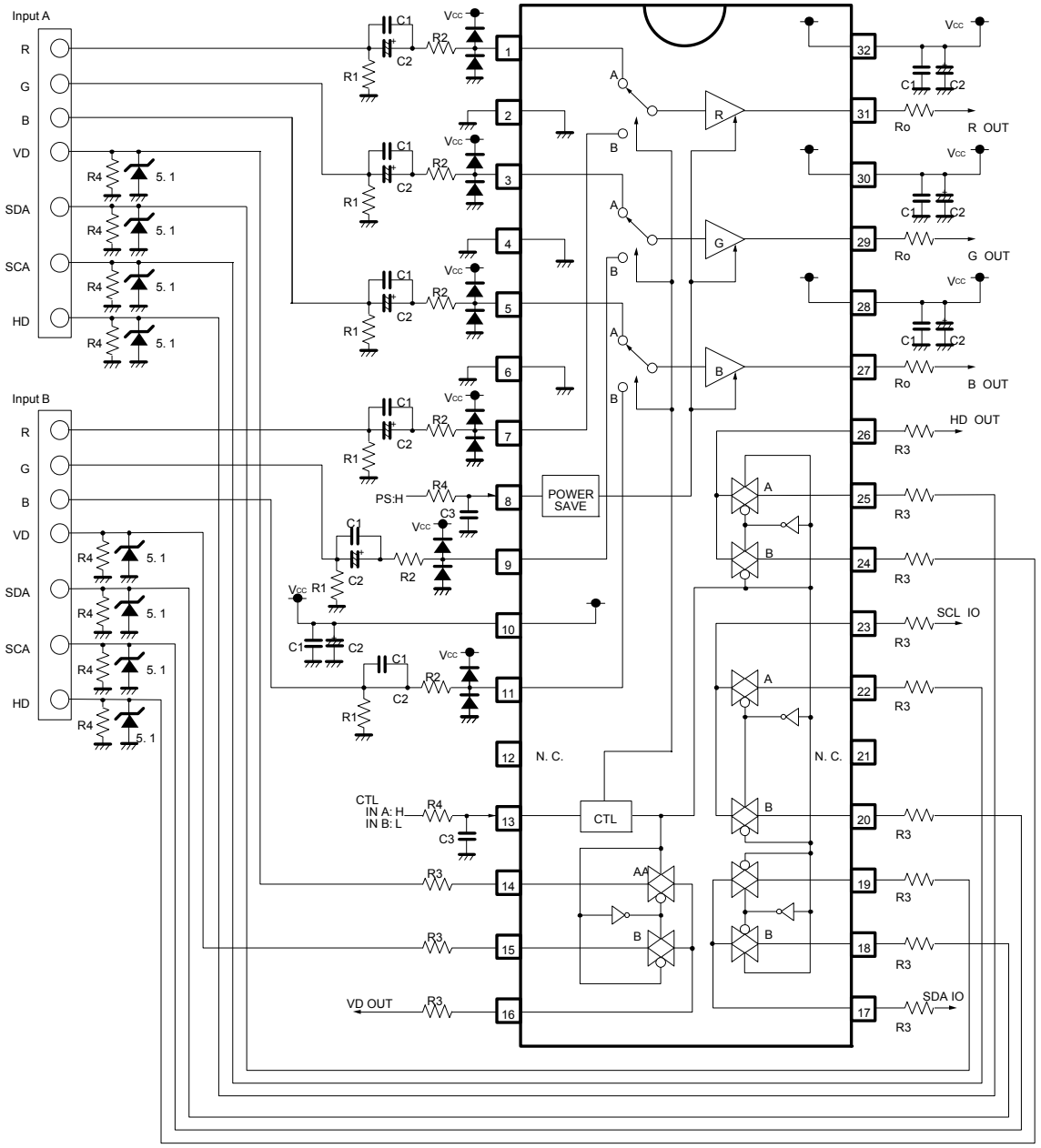


Fig.4

●Reference data

○BA7657F

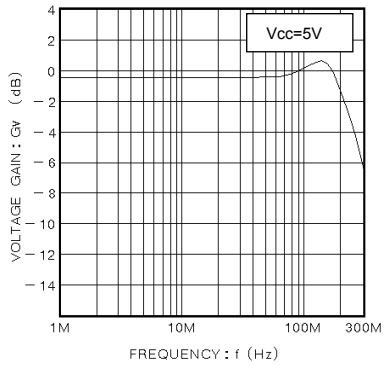


Fig.5 Frequency characteristic

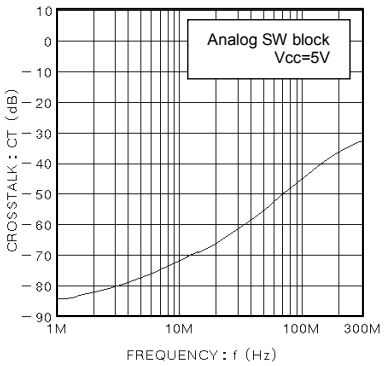


Fig.6 Interchannel crosstalk

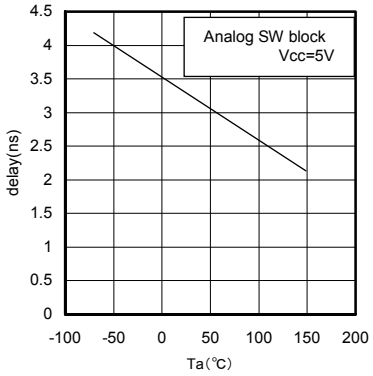


Fig.7 Input/output delay timevs. Temperatur

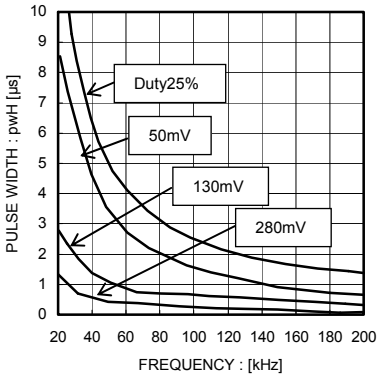


Fig.8 Minimum SYNC separation characteristic

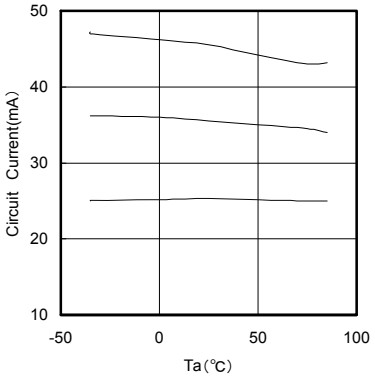


Fig.9 Quiescent current vs. Temperature

○BH7659FS

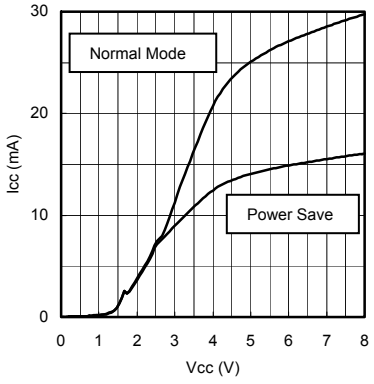


Fig.10 Circuit current vs. Supply voltage

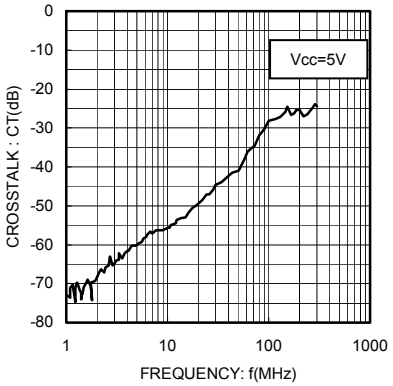


Fig.11 interchannel crosstalk

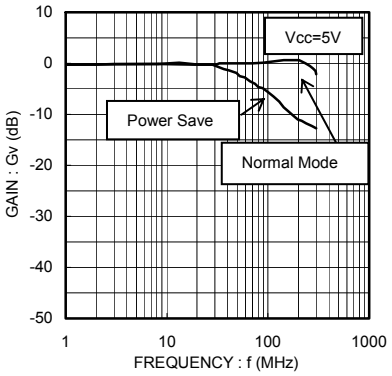


Fig.12 Frequency characteristics

●Notes for use

○BA7657F, BH7659FS

1) Numbers and data in entries are representative design values and are not guaranteed values of the items.

2) Although we are confident in recommending the sample application circuits, carefully check their characteristics further when using them. When modifying externally attached component constants before use, determine them so that they have sufficient margins by taking into account variations in externally attached components and the Rohm LSI, not only for static characteristics but also including transient characteristics.

3) Absolute maximum ratings
If applied voltage, operating temperature range, or other absolute maximum ratings are exceeded, the LSI may be damaged. Do not apply voltages or temperatures that exceed the absolute maximum ratings. If you think of a case in which absolute maximum ratings are exceeded, enforce fuses or other physical safety measures and investigate how not to apply the conditions under which absolute maximum ratings are exceeded to the LSI.

4) GND potential
Make the GND pin voltage such that it is the lowest voltage even when operating below it. Actually confirm that the voltage of each pin does not become a lower voltage than the GND pin, including transient phenomena.

5) Thermal design
Perform thermal design in which there are adequate margins by taking into account the allowable power dissipation in actual states of use.

6) Shorts between pins and misinstallation
When mounting the LSI on a board, pay adequate attention to orientation and placement discrepancies of the LSI. If it is misinstalled and the power is turned on, the LSI may be damaged. It also may be damaged if it is shorted by a foreign substance coming between pins of the LSI or between a pin and a power supply or a pin and a GND.

7) Operation in strong magnetic fields
Adequately evaluate use in a strong magnetic field, since there is a possibility of malfunction.

○BA7657F

8) External resistance for analog SW block
The frequency characteristics of analog switches vary according to the output load capacity. Set an external resistance value of R0 to keep frequency characteristics as flat as possible.

9) Polarity of input coupling capacitor
When this IC is switched, variation is approximately 3.7 V when the input pin's DC voltage has been selected, but is 0 V when the input pin's DC voltage has not been selected. Therefore, the input coupling capacitor's polarity should be set so as to avoid applying a reverse voltage to capacitors, whether the input pin's DC voltage has been selected or not.

10) High-frequency characteristics of input coupling capacitor
Since this IC handles signals at very high frequencies, when using an electrolytic capacitor as a coupling capacitor for input, be sure to insert high-frequency oriented ceramic capacitors (approximately 0.01 μF) in parallel.

11) Layout of target board
Since this IC handles signals at very high frequencies, be sure to insert the power supply pin's decoupling capacitor close to the IC's power supply pin. Also, use as large a GND pattern as possible.

12) Switching speed
Since this IC changes the DC voltage of input pins when switching, some time is required for switching. The amount of switching time can be determined by time constants that are in turn determined by the capacity of the coupling capacitor connected to the input pin, and the IC's internal input resistance. When using the recommended input coupling capacitor whose capacitance is 47 μF, the switching time is approximately 0.5 seconds.

○BH7659FS

13) External resistance for analog SW block
The frequency characteristics of analog switches vary according to the output load capacity. Set an external resistance value of R0 to keep frequency characteristics as flat as possible.

14) Polarity of input coupling capacitor
When this IC is switched, variation is approximately 3.5 V when the input pin's DC voltage has been selected, but is 0 V when the input pin's DC voltage has not been selected. Therefore, the input coupling capacitor's polarity should be set so as to avoid applying a reverse voltage to capacitors, whether the input pin's DC voltage has been selected or not.

15) High frequency characteristics of input coupling capacitor
Since this IC handles signals at very high frequencies, when using an electrolytic capacitor as a coupling capacitor for input, be sure to insert high-frequency oriented ceramic capacitors (approximately 0.01 μF) in parallel.

16) Layout of target board
Since this IC handles signals at very high frequencies, be sure to insert the power supply pin's decoupling capacitor close to the IC's power supply pin. Also, use as large a GND pattern as possible.

●Ordering part number

B	H		7	6	5	9		F	S	-	E	2

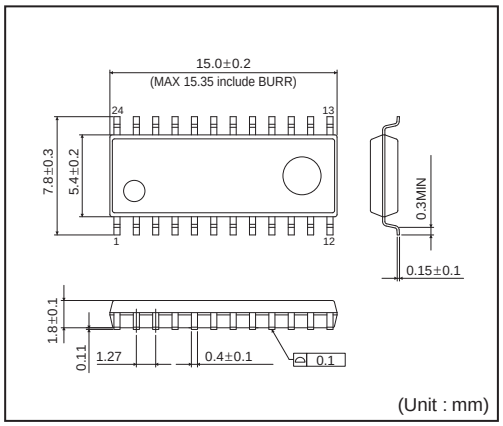
Part No.
BA
BH

Part No.
7657
7659

Package
F : SOP24
FS: SSOP-A32

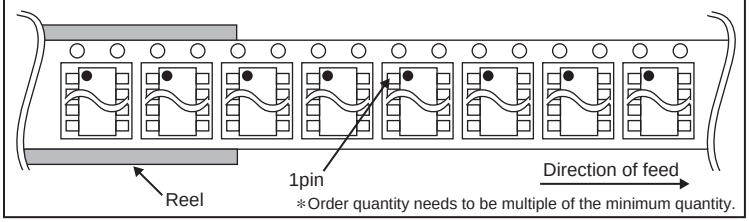
Packaging and forming specification
E2: Embossed tape and reel

SOP24



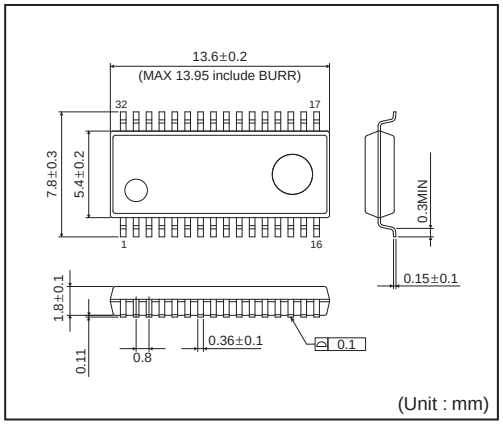
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



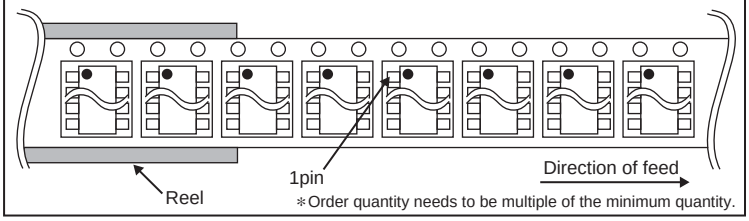
∗Order quantity needs to be multiple of the minimum quantity.

SSOP-A32



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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