Jameco Part Number 1748766

8-Channel Analog Multiplexer with Serial Interface

FEATURES

- **3-Wire Serial Digital Interface**
- Data Retransmission Allows Series Connection with Serial A/D Converters
- **Single 3V to ±5V Supply Operation**
- Analog Inputs May Extend to Supply Rails
- **Low Charge Injection**
- Low R_{ON}: 75Ω Max
- Low Leakage: ±5nA Max
- Guaranteed Break-Before-Make
- TTL/CMOS Compatible for All Digital Inputs
- Cascadable to Allow Additional Channels
- Can Be Used as a Demultiplexer

APPLICATIONS

- Data Acquisition Systems
- Communication Systems
- Signal Multiplexing/Demultiplexing

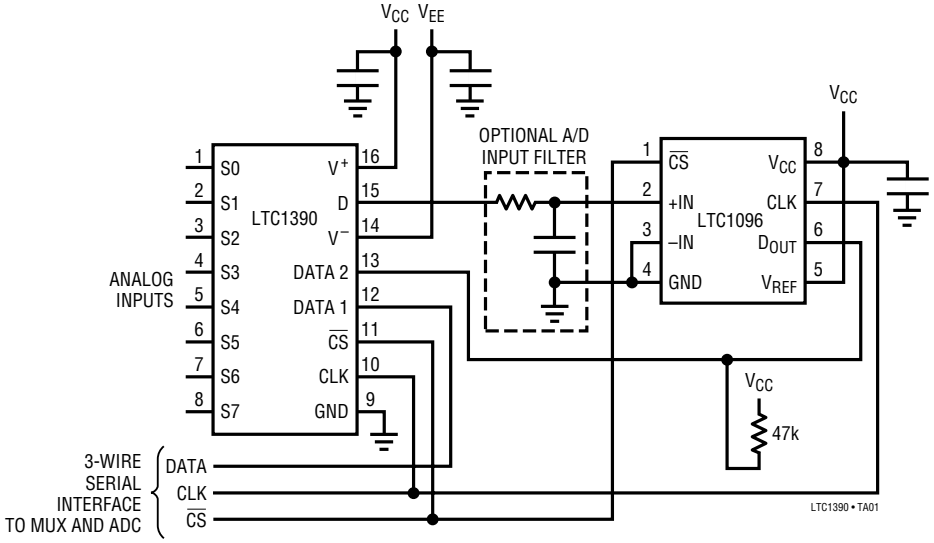
DESCRIPTION

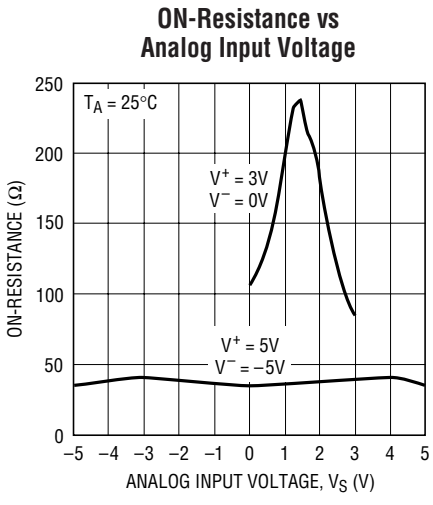
The LTC®1390 is a high performance CMOS 8-to-1 analog multiplexer. It features a 3-wire digital interface with a bidirectional data retransmission feature, allowing it to be wired in series with a serial A/D converter while using only one serial port. The interface also allows several LTC1390s to be wired in series or parallel, increasing the number of MUX channels available using only a single digital port. All the above features are also valid when LTC1390 operates as a demultiplexer such as with a D/A converter.

The LTC1390 features a typical R_{ON} of 45Ω, typical switch leakage of 50pA, and guaranteed break-before-make operation. Charge injection is ±10pC maximum. All digital inputs are TTL and CMOS compatible when operated from single or dual supplies. The inputs can withstand 100mA fault currents.

The LTC1390 is available in 16-pin PDIP and narrow SO packages.

TYPICAL APPLICATION



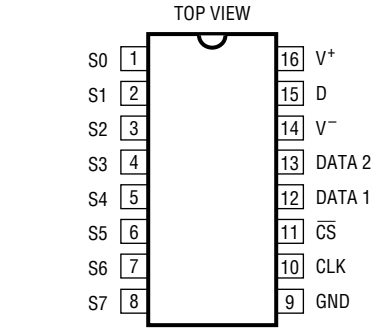


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-) 15V
Input Voltage
  Analog Inputs ..... V^- – 0.3V to V^+ + 0.3V
  Digital Inputs ..... –0.3V to 15V
  Digital Outputs ..... –0.3V to V^+ + 0.3V
Power Dissipation 500mW
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N PACKAGE
16-LEAD PDIP

S PACKAGE
16-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 70°C/W (N)
T_{JMAX} = 150°C, θ_{JA} = 100°C/W (S)

ORDER PART NUMBER
LTC1390CN LTC1390CS

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V^+ = 5V, V^- = –5V, GND = 0V, T_A = operating temperature unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switch							
V_{ANALOG}	Analog Signal Range	(Note 2)	●	–5		5	V
R_{ON}	On Resistance	V_S = ±3.5V, I_D = 1mA					
		T_{MIN}				75	Ω
		25°C			45	75	Ω
		T_{MAX}				120	Ω
	ΔR_{ON} vs V_S				20		%
	ΔR_{ON} vs Temperature				0.5		%/°C
$I_{S(OFF)}$	Off Input Leakage	V_S = 4V, V_D = –4V; V_S = –4V, V_D = 4V			0.05	±5	nA
		Channel Off	●			±50	nA
$I_{D(OFF)}$	Off Output Leakage	V_S = 4V, V_D = –4V; V_S = –4V, V_D = 4V			0.05	±5	nA
		Channel Off	●			±50	nA
$I_{D(ON)}$	On Channel Leakage	V_S = V_D = ±4V			0.05	±5	nA
		Channel On	●			±50	nA
Input							
V_{INH}	High Level Input Voltage	V^+ = 5.25V	●	2.4			V
V_{INL}	Low Level Input Voltage	V^+ = 4.75V	●			0.8	V
I_{INL}, I_{INH}	Low or High Level Current	V_{IN} = 5V, V_{IN} = 0V	●			±1	µA
V_{OH}	High Level Output Voltage	V^+ = 4.75V, I_O = 10µA			4.74		V
		V^+ = 4.75V, I_O = 360µA	●	2.4	4.50		V
V_{OL}	Low Level Output Voltage	V^+ = 4.75V, I_O = 0.5mA	●		0.16	0.8	V

ELECTRICAL CHARACTERISTICS

V^+ = 5V, V^- = –5V, GND = 0V, T_A = operating temperature unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Dynamic							
f_{CLK}	Clock Frequency					5	MHz
t_{ON}	Enable Turn-On Time	V_S = 2.5V, R_L = 1k, C_L = 35pF			260	400	ns
t_{OFF}	Enable Turn-Off Time	V_S = 2.5V, R_L = 1k, C_L = 35pF			100	200	ns
t_{OPEN}	Break-Before-Make Interval			35	155		ns
OIRR	Off Isolation	$V_S = 2V_{P-P}$, R_L = 1k, f = 100kHz			70		dB
O_{INJ}	Charge Injection	R_S = 0, C_L = 1000pF, V_S = 1V (Note 2)			±2	±10	pC
$C_{S(OFF)}$	Source Off Capacitance				5		pF
$C_{D(OFF)}$	Drain Off Capacitance				10		pF
Supply							
I^+	Positive Supply Current	All Logic Inputs Tied Together, V_{IN} = 0V or V_{IN} = 5V	●		15	40	µA
I^-	Negative Supply Current	All Logic Inputs Tied Together, V_{IN} = 0V or V_{IN} = 5V	●		15	40	µA

V^+ = 3V, V^- = GND = 0V, T_A = operating temperature unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switch							
V_{ANALOG}	Analog Signal Range	(Note 2)	●	0		3	V
R_{ON}	On Resistance	V_S = 1.2V, I_D = 1mA					
		T_{MIN}				255	Ω
		25°C			200	255	Ω
		T_{MAX}				300	Ω
	ΔR_{ON} vs V_S				20		%
	ΔR_{ON} vs Temperature				0.5		%/°C
$I_{S(OFF)}$	Off Input Leakage	V_S = 2.5V, V_D = 0.5V; V_S = 0.5V, V_D = 2.5V (Note 3)			±0.05	±5	nA
		Channel Off	●			±50	nA
$I_{D(OFF)}$	Off Output Leakage	V_S = 2.5V, V_D = 0.5V; V_S = 0.5V, V_D = 2.5V (Note 3)			±0.05	±5	nA
		Channel Off	●			±50	nA
$I_{D(ON)}$	On Channel Leakage	$V_S = V_D$ = 0.5V, $V_S = V_D$ = 2.5V (Note 3)			±0.05	±5	nA
		Channel On	●			±50	nA
Input							
V_{INH}	High Level Input Voltage	V^+ = 3.3V	●	2.4			V
V_{INL}	Low Level Input Voltage	V^+ = 2.7V	●			0.8	V
I_{INL}, I_{INH}	Low or High Level Current	V_{IN} = 3V, V_{IN} = 0V	●			±1	µA
V_{OH}	High Level Output Voltage	V^+ = 2.7V, I_O = 20µA			2.68		V
		V^+ = 2.7V, I_O = 400µA	●	2	2.27		V
V_{OL}	Low Level Output Voltage	V^+ = 2.7V, I_O = 20µA			0.01		V
		V^+ = 2.7V, I_O = 300µA	●		0.15	0.8	V

ELECTRICAL CHARACTERISTICS

V^+ = 3V, V^- = GND = 0V, T_A = operating temperature unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Dynamic							
f_{CLK}	Clock Frequency					5	MHz
t_{ON}	Enable Turn-On Time	V_S = 1.5V, R_L = 1k, C_L = 35pF (Note 4)			490	700	ns
t_{OFF}	Enable Turn-Off Time	V_S = 1.5V, R_L = 1k, C_L = 35pF (Note 4)			190	300	ns
t_{OPEN}	Break-Before-Make Interval	(Note 4)		125	290		ns
OIRR	Off Isolation	$V_S = 2V_{P-P}$, R_L = 1k, f = 100kHz			70		dB
O_{INJ}	Charge Injection	R_S = 0, C_L = 1000pF, V_S = 1V (Note 2)			±1	±5	pC
$C_{S(OFF)}$	Source Off Capacitance				5		pF
$C_{D(OFF)}$	Drain Off Capacitance				10		pF
Supply							
I^+	Positive Supply Current	All Logic Inputs Tied Together, V_{IN} = 0V or V_{IN} = 3V	●		0.2	2	µA

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute maximum ratings are those beyond which the safety of the device may be impaired.

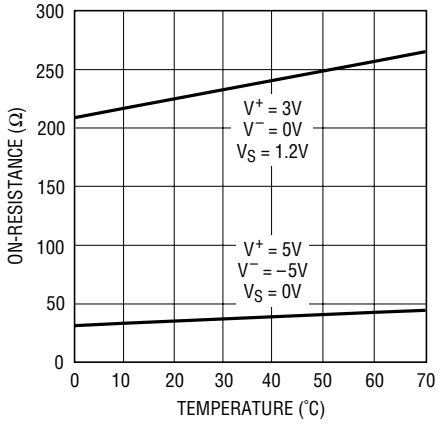
Note 2: Guaranteed by design.

Note 3: Leakage current with a single 3V supply is guaranteed by correlation with the leakage current of the ±5V supply.

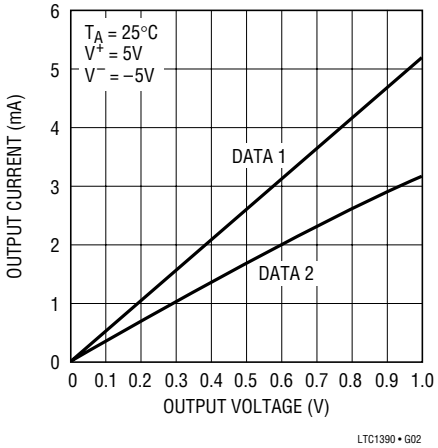
Note 4: Timing specifications with a single 3V supply is guaranteed by correlation with the timing specifications of the ±5V supply.

TYPICAL PERFORMANCE CHARACTERISTICS

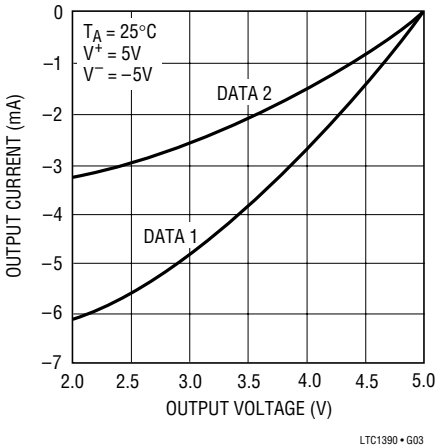
ON-Resistance vs Temperature



Driver Output Low Voltage vs Output Current



Driver Output High Voltage vs Output Current



PIN FUNCTIONS

S0 to S7 (Pins 1 to 8): Analog Multiplexer Inputs/Analog Demultiplexer Outputs.

GND (Pin 9): Digital Ground. Connect to system ground.

CLK (Pin 10): System Clock (TTL/CMOS Compatible). The clock synchronizes the channel selection bits and the serial data transfer from Data 1 to Data 2.

PIN FUNCTIONS

$\overline{CS}$ (Pin 11): Chip Select Input (TTL/CMOS Compatible). A logic high on this input enables LTC1390 to read in the channel selection bits and allow data transfer from Data 1 to Data 2. A logic low enables the desired channel for analog signal transmission and allows data transfer from Data 2 to Data 1.

Data 1 (Pin 12): Bidirectional Digital Input/Output (TTL/CMOS Compatible). Input for the channel selection bits.

Data 2 (Pin 13): Bidirectional Digital Input/Output (TTL/CMOS Compatible).

V^- (Pin 14): Negative Supply. For ±5V dual supply applications, $|V^-|$ should not exceed $|V^+|$ by more than 20% for proper channel selection.

D (Pin 15): Analog Multiplexer Output/Analog Demultiplexer Input.

V^+ (Pin 16): Positive Supply.

APPLICATIONS INFORMATION

Multiplexer Operation

Figure 1 shows the block diagram of the components within the LTC1390 required for MUX operation. The LTC1390 uses Data 1 to select its 8 channels and a chip select input $\overline{CS}$ to switch on the selected channel as shown in Figure 2.

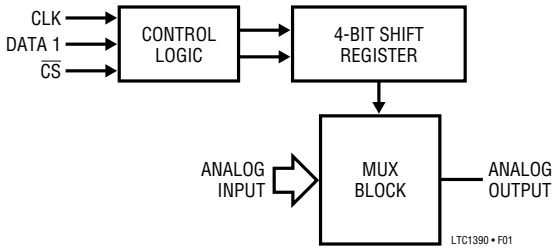


Figure 1: Simplified Block Diagram of the MUX Operation

When $\overline{CS}$ is high, the input data on the Data 1 pin is latched into the 4-bit shift register on each rising clock edge. The input data consists of an "EN" bit and a string of three bits for channel selection. If "EN" bit is logic high as illustrated in the first input data sequence, it enables the selected channel. To ensure correct operation, the $\overline{CS}$ must be pulled low before the next rising clock edge.

Once the $\overline{CS}$ is pulled low, all channels are simultaneously switched off to ensure a break-before-make interval. After a delay of t_{ON}, the selected channel is switched on allowing signal transmission. The selected channel remains on until the next falling edge of $\overline{CS}$, and after a delay of t_{OFF}, it terminates the analog signal transmission and subsequently allows the selection of the next channel. If "EN" bit is logic low, as illustrated in the second data sequence, it disables all channels and there will be no analog signal

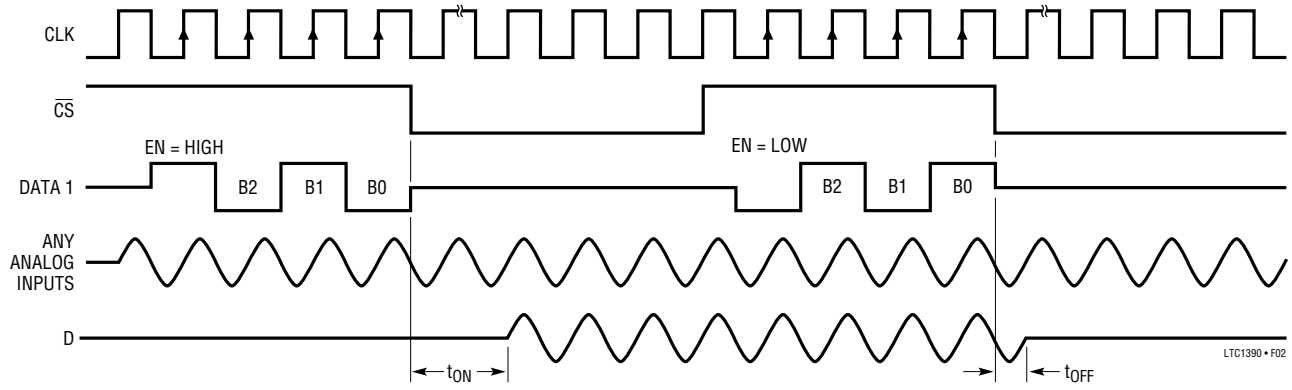


Figure 2: Multiplexer Operation

APPLICATIONS INFORMATION

transmission. Table 1 shows the various bit combinations for channel selection.

Table 1. Logic Table for Channel Selection

CHANNEL STATUS	EN	B2	B1	B0
All Off	0	X	X	X
S0	1	0	0	0
S1	1	0	0	1
S2	1	0	1	0
S3	1	0	1	1
S4	1	1	0	0
S5	1	1	0	1
S6	1	1	1	0
S7	1	1	1	1

Digital Data Transfer Operation

The block diagram of Figure 3 shows the components contained within the LTC1390 required for digital data transfer. Digital data transfer operation can be performed from Data 1 to Data 2 and vice versa as shown in Figure 4. When $\overline{CS}$ is high, Buffer 1 is enabled and Buffer 2 is disabled. The digital input data is fed into the 4-bit shift register and then shifted to the MUX switches for channel selection or to Data 2 via Buffer 1 for data transfer. Data appears at Data 2 after the fourth rising edge of the clock. When $\overline{CS}$ is low, Buffer 2 is enabled and Buffer 1 is disabled, thus digital input data is directly transferred from Data 2 to Data 1 without any clock delay.

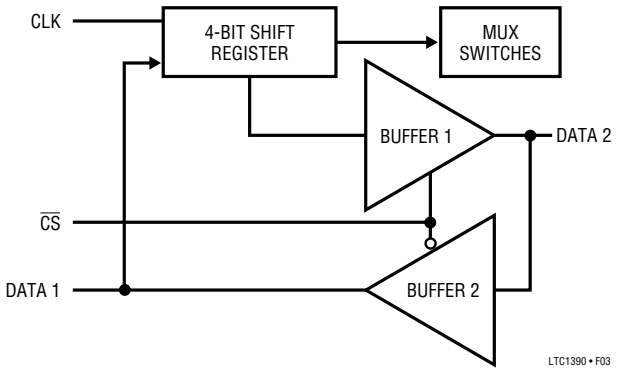


Figure 3. Simplified Block Diagram of the Digital Data Transfer Operation

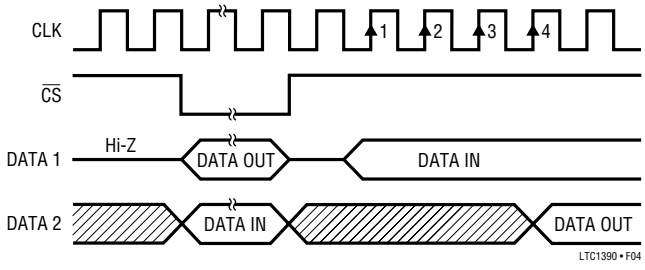


Figure 4. Digital Data Transfer Operation

Multiplexer Expansion

Several LTC1390s can be daisy-chained to expand the number of multiplexer inputs. No additional interface ports are required for the expansion. Figure 5 shows two LTC1390s connected at their analog outputs to form a 16-to-1 multiplexer at the input to an LTC1286 A/D converter.

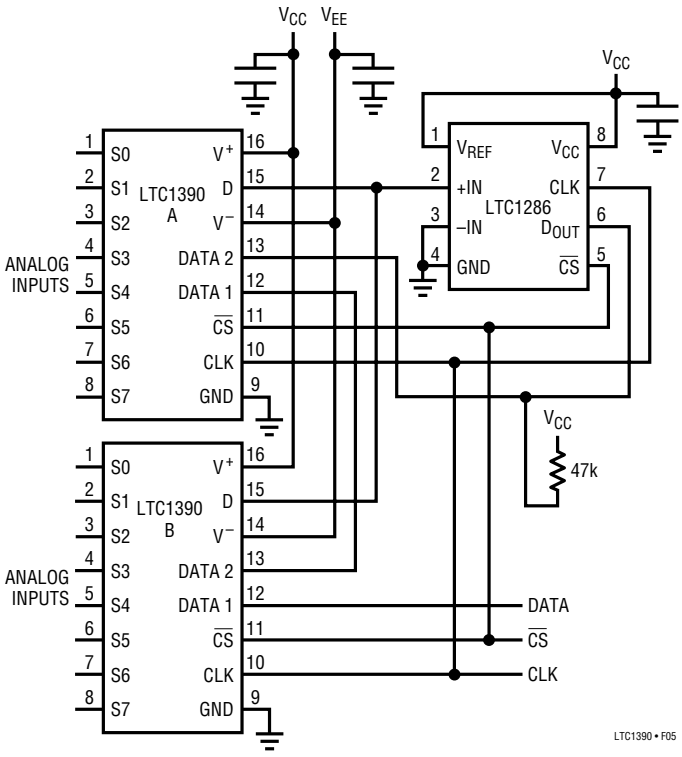


Figure 5. Daisy-Chaining Two LTC1390s for Expansion

To ensure that only one channel is switched on at any one time, two sets of channel selection bits are needed for Data as shown in Figure 6. The first data sequence is used to switch off one MUX and the second data sequence is used to select one channel from the other MUX, or vice versa. In other words, if bit "ENA" is high and bit "ENB" is low, one channel of MUX A is switched on and all channels of MUX B are switched off. If bit "ENA" is low and bit "ENB" is high, all channels of MUX A are switched off and one channel of MUX B is switched on.

APPLICATIONS INFORMATION

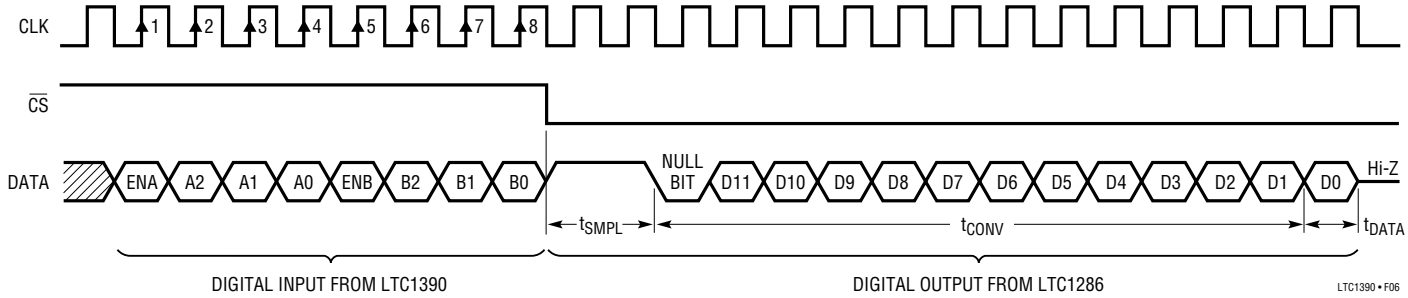
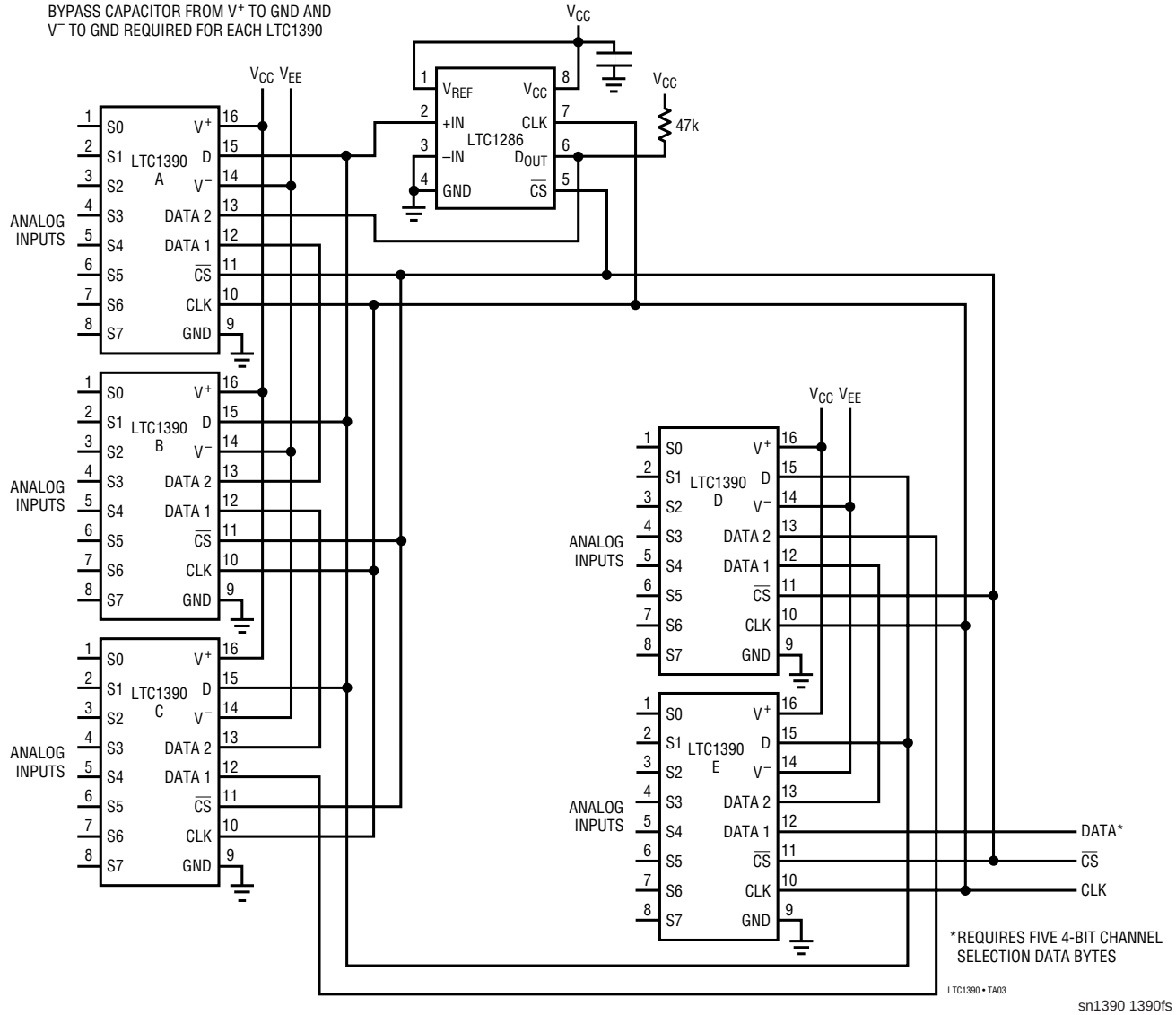


Figure 6. Timing Diagram for Figure 5

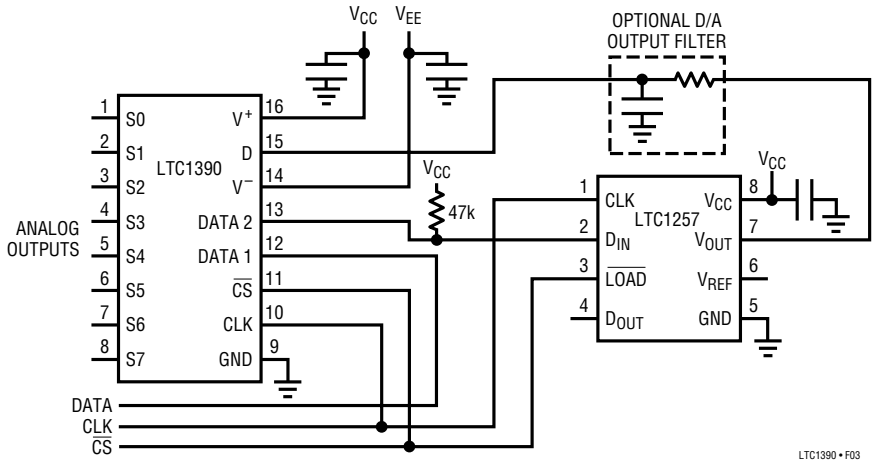
TYPICAL APPLICATIONS

Daisy-Chaining Five LTC1390s



TYPICAL APPLICATIONS

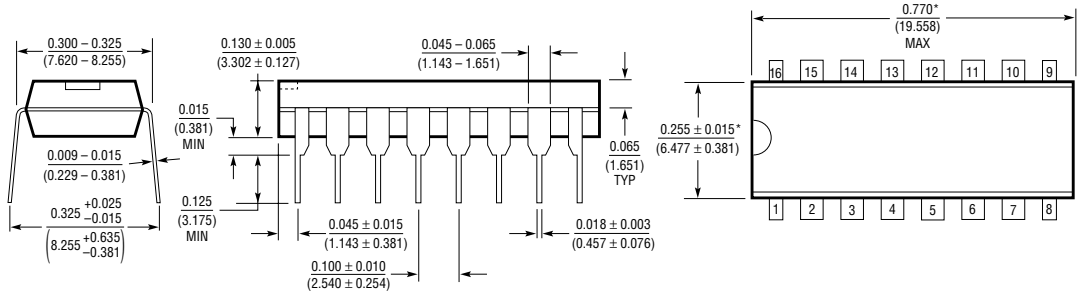
Interfacing LTC1390 with LTC1257 for Demultiplex Operation



PACKAGE DESCRIPTION

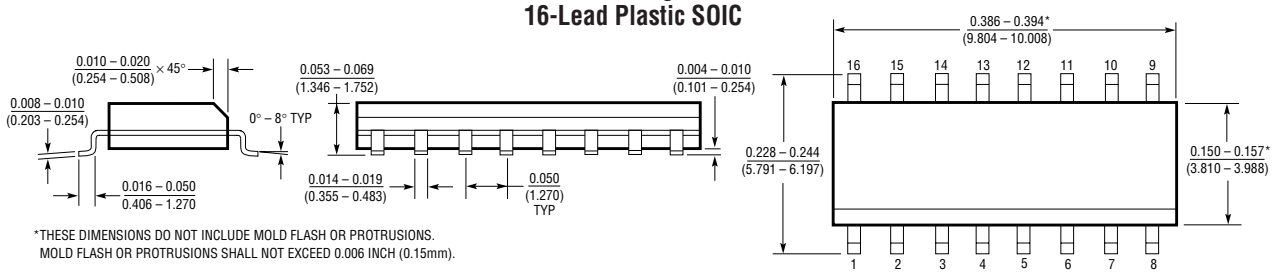
Dimensions in inches (millimeters) unless otherwise noted.

N Package
16-Lead Plastic DIP



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm).

S Package
16-Lead Plastic SOIC



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCH (0.15mm).

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC201A/LTC202/LTC203	Micropower, Low Charge Injection, Quad CMOS Analog Switches	Each Channel is Independently Controlled
LTC221/LTC222	Micropower, Low Charge Injection, Quad CMOS Analog Switches with Data Latches	Parallel Controlled with Data Latches
LTC128x/LTC129x	Serial A/Ds with Integral MUXs	

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