RDS / RBDS decoder

BU1920 / BU1920F / BU1920FS

The BU1920, BU1920F and BU1920FS are RDS / RBDS decoders that employ a digital PLL. It has a built-in anti-aliasing filter and an eight-stage BPF (switched-capacitor filter). Linear CMOS circuitry is used for low current dissipation.

●Applications

RDS/RBDS compatible FM receivers for Europe and North America, car stereo systems, home stereo systems and FM pagers.

●Features

1) Low current dissipation.
2) Two-stage anti-aliasing filter.
3) 57kHz bandpass filter.
4) DSB demodulation (digital PLL).
5) ARI signal discrimination.
6) Quality indication output for demodulated data.

●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{DD}	−0.3～+7.0	V
Maximum input voltage	$V_{MAX.}$	−0.3～V_{DD}+0.3*1	V
Maximum output current	$I_{MAX.}$	±4.0*2	mA
Power dissipation	P_d	350*3	mW
Operating temperature	T_{opr}	−40～+85	℃
Storage temperature	T_{stg}	−55～+125	℃

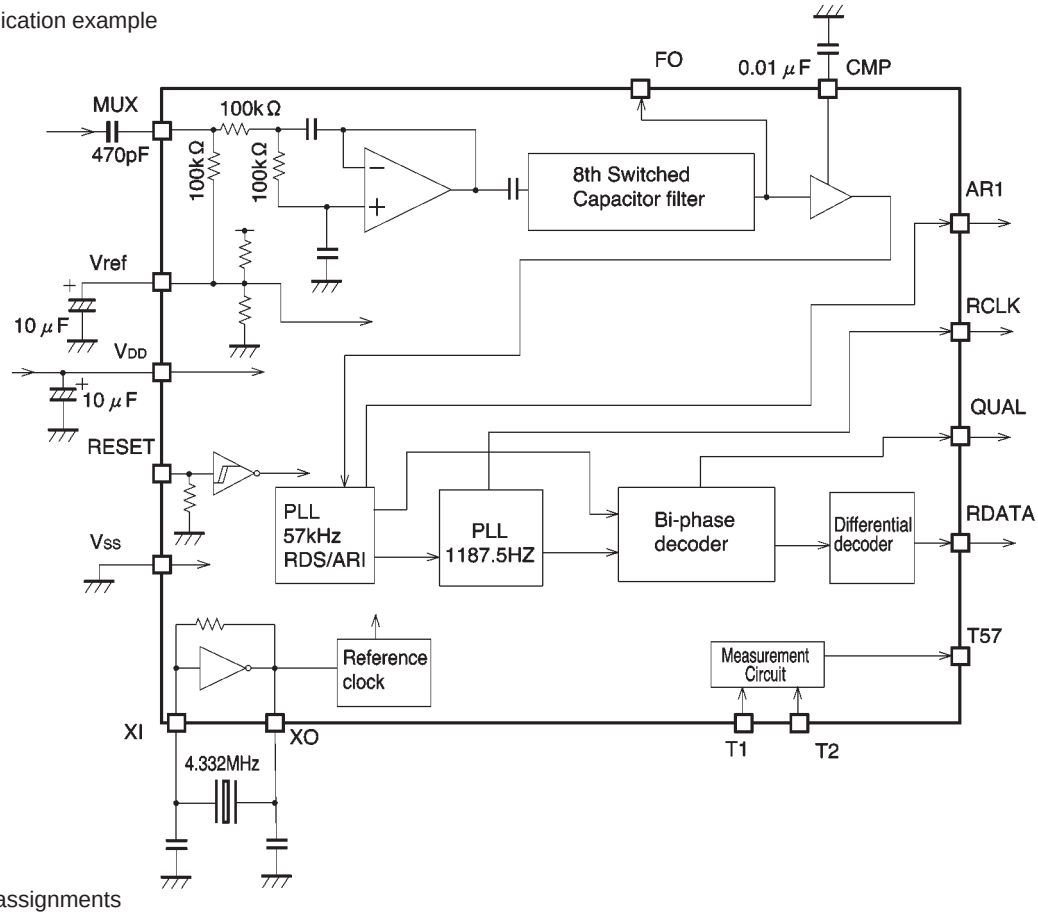
*1 All input / output pins.
*2 All output pins.
*3 Reduced by 3.5mW for each increase in Ta of 1°C over 25°C.

●Recommended operating conditions (Ta = 25°C)

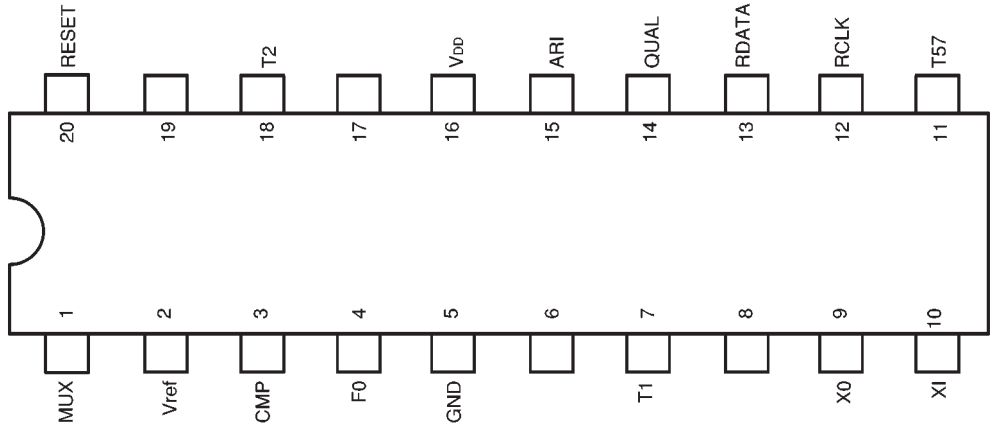
Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	4.5	−	5.5	V

●Block diagram

Application example



Pin assignments

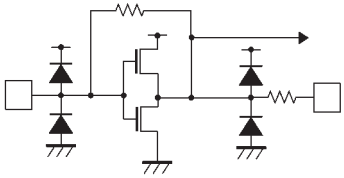


●Pin descriptions

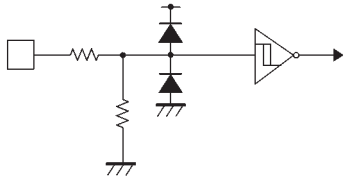
Pin No.	Symbol	Pin name	Function	Input/output type
1	MUX	Input	Composite signal input (refer to the circuit example)	Type F
2	Vref	Reference voltage	1/2 VDD1 (refer to the circuit example)	Type G
3	CMP	Comparator	Refer to the circuit example	Type H
4	FO	Output	Open, for monitoring the filter output	Type I
5	GND	—	—	—
6	(N.C.)	—	Not connected (floating)	—
7	T1	Test input	Open or connected to GND	Type B
8	(N.C.)	—	Not connected (floating)	—
9	XO	Crystal oscillator	Connects to 4.332MHz oscillator (refer to the circuit example)	Type A
10	XI			
11	T57	Test output	Open	Type E
12	RCLK	Demodulator clock	1187.5kHz clock (refer to the timing diagram)	
13	RDATA	Demodulator data	Refer to the timing diagram	
14	QUAL	Demodulator quality	Good data: HI, bad data: LO	
15	ARI	ARI signal discrimination	ARI + RDS: HI, RDS: LO, no signal: unstable	
16	V_{DD}	Power supply	4.5~5.5V	—
17	(N.C.)	—	Not connected (floating)	—
18	T2	Test input	Open or connected to GND	Type B
19	(N.C.)	—	Not connected (floating)	—
20	RESET	Reset	HI: reset, open/LO: operating	Type B

●Input/output circuits

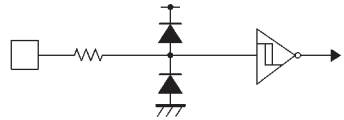
Type A



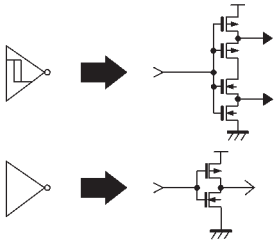
Type B



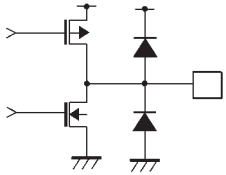
Type C



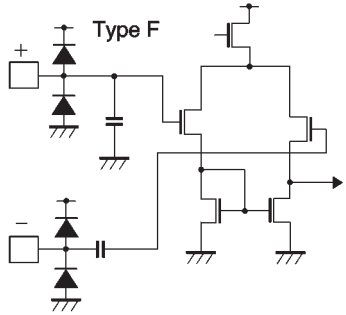
Type D



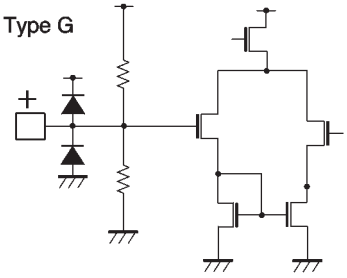
Type E



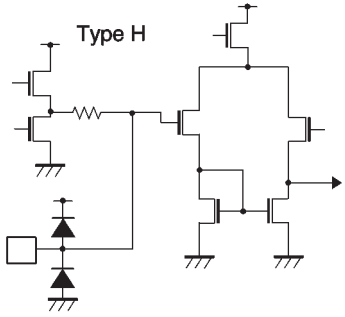
Type F



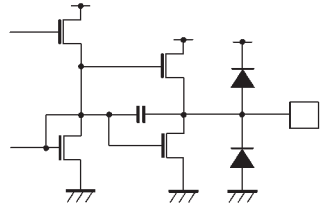
Type G



Type H



Type I



●Electrical characteristics (unless otherwise noted, Ta = 25°C, V_{DD} = 5.0V and GND = 0.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating power suppply current	I_{DD}	—	4.5	7.0	mA	I_{DD}
Reset current	I_{DD}	—	2.0	4.0	mA	I_{DD}
Reference voltage	Vref	—	1/2V_{DD1}	—	V	Pin 2
Input current 1	I_{IN1}	—	—	1.0	μA	MUX V_{IN}=V_{DD}
Output current 1	I_{OUT1}	—	—	1.0	μA	MUX V_{IN}=V_{DD}
Input current 2	I_{IN2}	—	—	1.0	μA	RESET XI V_{IN}=V_{DD}
Output current 2	I_{OUT2}	—	—	1.0	μA	RESET XI V_{IN}=V_{DD}
Output high level voltage 1	V_{OH1}	V_{DD2} −1.0	V_{DD2} −0.3	—	V	RCLK RDATA QUAL ARI I_O=−1.0mA
Output low level voltage 1	V_{OL1}	—	0.2	1.0	V	RCLK RDATA QUAL ARI I_O=1.0mA
Input high level voltage	V_{IH}	0.8V_{DD2}	—	—	—	RESET
Intput low level voltage	V_{IL}	—	—	0.2V_{DD2}	V	RESET

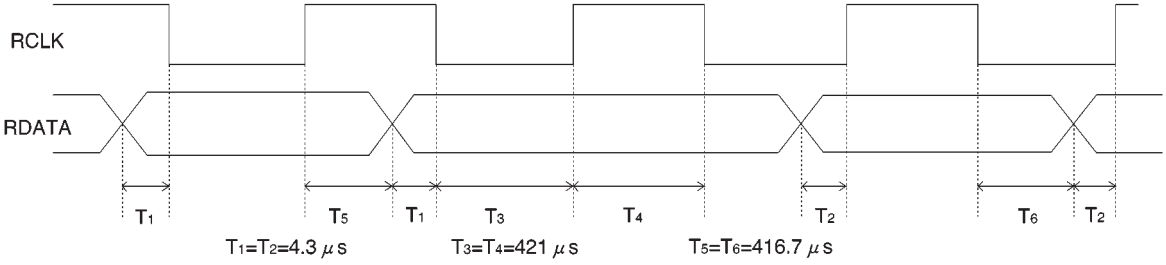
Filter block

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Center frequency	FC	56.5	57.0	57.5	kHz	
Gain	GA	18	20	22	dB	F=57.0kHz
Attenuation 1	ATT1	18	22	—	dB	57kHz±4kHz
Attenuation 2	ATT2	50	80	—	dB	38kHz
Attenuation 3	ATT3	35	50	—	dB	67kHz
S / N ratio	SN	30	40	—	dB	57kHz V_{IN}=3mV_{rms}
Maximum input level	VMAX1	—	—	500	mV_{rms}	

Demodulator block

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
RDS detector sensitivity	SRDS	—	0.5	1.0	mV_{rms}	
RDS maximum input level	MRDS	—	—	300	mV_{rms}	
ARI detector sensitivity	SARI	—	1.5	3.0	mV_{rms}	
ARI maximum input level	MARI	—	—	500	mV_{rms}	
Lockup time (RDS)	TL	—	100	200	ms	
Data rate	DRATE	—	1187.5	—	Hz	
Clock transient vs. data	CT	—	4.3	—	μs	

●Output data timing



The clock (RCLK) frequency is 1187.5Hz. Depending on the state of the internal PLL clock, the data (RDATA) is replaced in synchronous with either the rising or falling edge of the clock. To read the data, you may choose either the rising or falling edge of the clock as the reference. The data is valid for 416.7μs, after the reference clock edge.

QUAL pin operation: Indicates the quality of the demodulated data.

(1) Good data : HI
(2) Poor data : LO

ARI pin operation: ARI/RDS discrimination.

(1) ARI : LO
(2) RDS + ARI : LO
(3) RDS : HI
(4) No signal : unstable

●Electrical characteristics curve

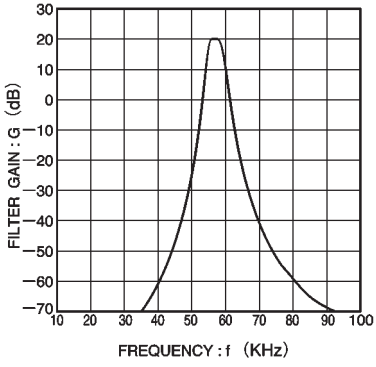


Fig. 1 Bandpass filter characteristics