LAN9500/LAN9500i
LAN9500A/LAN9500Ai

USB 2.0 to 10/100 Ethernet Controller

PRODUCT FEATURES

Datasheet

Highlights

- Single Chip Hi-Speed USB 2.0 to 10/100 Ethernet Controller
- Integrated 10/100 Ethernet MAC with Full-Duplex Support
- Integrated 10/100 Ethernet PHY with HP Auto-MDIX support
- Integrated USB 2.0 Hi-Speed Device Controller
- Integrated USB 2.0 Hi-Speed PHY
- Implements Reduced Power Operating Modes

Target Applications

- Embedded Systems
- Set-Top Boxes
- PVR's
- CE Devices
- Networked Printers
- USB Port Replicators
- Standalone USB to Ethernet Dongles
- Test Instrumentation
- Industrial

Key Features

- USB Device Controller
  - Fully compliant with Hi-Speed Universal Serial Bus Specification Revision 2.0
  - Supports HS (480 Mbps) and FS (12 Mbps) modes
  - Four endpoints supported
  - Supports vendor specific commands
  - Integrated USB 2.0 PHY
  - Remote wakeup supported
- High-Performance 10/100 Ethernet Controller
  - Fully compliant with IEEE802.3/802.3u
  - Integrated Ethernet MAC and PHY
  - 10BASE-T and 100BASE-TX support
  - Full- and half-duplex support
  - Full- and half-duplex flow control
  - Preamble generation and removal
  - Automatic 32-bit CRC generation and checking
  - Automatic payload padding and pad removal
  - Loop-back modes
  - TCP/UDP/IP/ICMP checksum offload support
  - Flexible address filtering modes
    - One 48-bit perfect address
    - 64 hash-filtered multicast addresses
    - Pass all multicast
    - Promiscuous mode
    - Inverse filtering
    - Pass all incoming with status report
  - Wakeup packet support
  - Integrated Ethernet PHY
    - Auto-negotiation
    - Automatic polarity detection and correction
    - HP Auto-MDIX support
    - Link status change wake-up detection
  - Support for 3 status LEDs
  - External MII and Turbo MII support HomePNA™ and HomePlug® PHY
- Power and I/Os
  - Various low power modes
  - NetDetach feature increases battery life [1]
  - Supports PCI-like PME wake [1]
  - 11 GPIOs
  - Supports bus-powered and self-powered operation
  - Integrated power-on reset circuit
  - Single external 3.3v I/O supply
    - Internal core regulator
- Miscellaneous Features
  - EEPROM Controller
  - Supports custom operation without EEPROM [1]
  - IEEE 1149.1 (JTAG) Boundary Scan
  - Requires single 25 MHz crystal
- Software
  - Windows XP/Vista Driver
  - Linux Driver
  - Win CE Driver
  - MAC OS Driver
  - EEPROM Utility
- Packaging
  - 56-pin QFN (8x8 mm) Lead-Free RoHS Compliant
- Environmental
  - Commercial Temperature Range (0°C to +70°C)
  - Industrial Temperature Range (-40°C to +85°C)

[1] = LAN9500A/LAN9500Ai only

Order Numbers:

LAN9500-ABZJ (Tray) for 56-pin, QFN lead-free RoHS compliant package (0 to +70°C temp range)

LAN9500-ABZJ-TR (Tape & Reel) for 56-pin, QFN lead-free RoHS compliant package (0 to +70°C temp range)

LAN9500i-ABZJ (Tray) for 56-pin, QFN lead-free RoHS compliant package (-40 to +85°C temp range)

LAN9500i-ABZJ-TR (Tape & Reel) for 56-pin, QFN lead-free RoHS compliant package (-40 to +85°C temp range)

LAN9500A-ABZJ (Tray) for 56-pin, QFN lead-free RoHS compliant package (0 to +70°C temp range)

LAN9500A-ABZJ-TR (Tape & Reel) for 56-pin, QFN lead-free RoHS compliant package (0 to +70°C temp range)

LAN9500Ai-ABZJ (Tray) for 56-pin, QFN lead-free RoHS compliant package (-40 to +85°C temp range)

LAN9500Ai-ABZJ-TR (Tape & Reel) for 56-pin, QFN lead-free RoHS compliant package (-40 to +85°C temp range)

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

Please contact your SMSC sales representative for additional documentation related to this product such as application notes, anomaly sheets, and design guidelines.

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Chapter 1 LAN950x Family Differences Overview

The SMSC LAN950x is a family of high performance Hi-Speed USB 2.0 to 10/100 Ethernet controllers. The “x” in the part number is a generic term referring to the entire family, which includes the following devices:

- LAN9500
- LAN9500i
- LAN9500A
- LAN9500Ai

Device specific features that do no pertain to the entire LAN950x family are called out independently throughout this document. Table 1.1 provides a summary of the feature differences between family members.

Table 1.1 LAN950x Family Differences

PART NUMBER	PME WAKE	NET DETACH	SUSPEND3 STATE	GOOD PACKET WAKEUP	PHY BOOST	CUSTOM OPERATION WITHOUT EEPROM	INCREASED WAKEUP FRAME FILTER	0^{o} TO $70^{o}C$	-40^{o} TO $85^{o}C$
LAN9500								**X**	
LAN9500i									**X**
LAN9500A	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	
LAN9500Ai	**X**	**X**	**X**	**X**	**X**	**X**	**X**		**X**

The LAN9500/LAN9500i and LAN9500A/LAN9500Ai are pin compatible. However, the value of the required EXRES resistor and other system components differ between devices. Refer to Figure 1.1 and the LAN950x reference schematics for additional information.

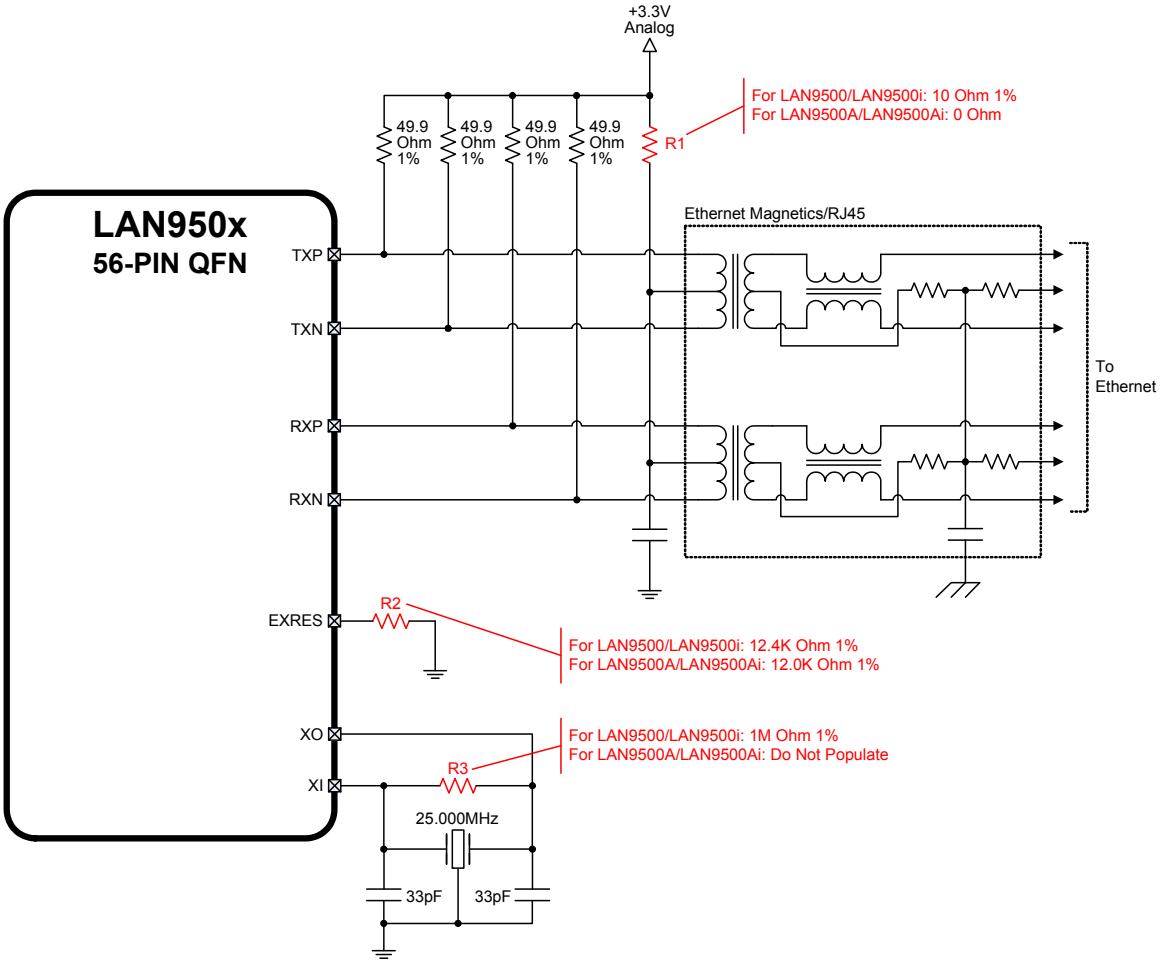


Figure 1.1 System Component Differences

Chapter 2 Introduction

2.1 Block Diagram

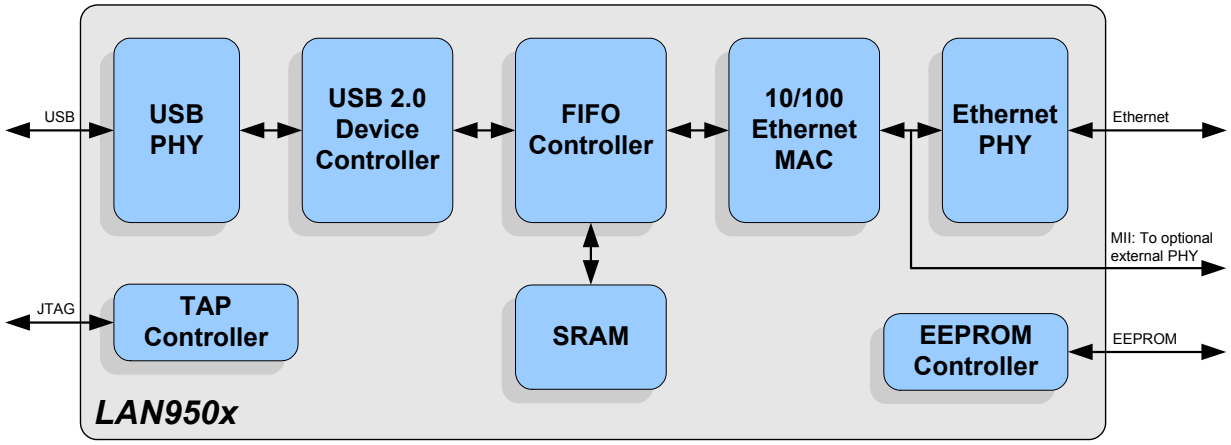


Figure 2.1 System Diagram

2.1.1 Overview

The LAN950x is a high performance Hi-Speed USB 2.0 to 10/100 Ethernet controller. With applications ranging from embedded systems, set-top boxes, and PVR's, to USB port replicators, USB to Ethernet dongles, and test instrumentation, the device is a high performance and cost competitive USB to Ethernet connectivity solution.

The LAN950x contains an integrated 10/100 Ethernet PHY, USB PHY, Hi-Speed USB 2.0 device controller, 10/100 Ethernet MAC, TAP controller, EEPROM controller, and a FIFO controller with a total of 30 KB of internal packet buffering.

The internal USB 2.0 device controller and USB PHY are compliant with the USB 2.0 Hi-Speed standard. The device implements Control, Interrupt, Bulk-in, and Bulk-out USB Endpoints.

The Ethernet controller supports auto-negotiation, auto-polarity correction, HP Auto-MDIX, and is compliant with the IEEE 802.3 and IEEE 802.3u standards. An external MII interface provides support for an external Fast Ethernet PHY, HomePNA, and HomePlug functionality.

Multiple power management features are provided, including various low power modes and "Magic Packet", "Wake On LAN", and "Link Status Change" wake events. These wake events can be programmed to initiate a USB remote wakeup.

An internal EEPROM controller exists to load various USB configuration information and the device MAC address. The integrated IEEE 1149.1 compliant TAP controller provides boundary scan via JTAG.

2.1.2 USB

The USB portion of the LAN950x integrates a Hi-Speed USB 2.0 device controller and USB PHY.

The USB device controller contains a USB low-level protocol interpreter which implements the USB bus protocol, packet generation/extraction, PID/Device ID parsing, and CRC coding/decoding, with autonomous error handling. The USB device controller is capable of operating in USB 2.0 Hi-Speed and Full-Speed compliant modes and contains autonomous protocol handling functions such as handling of suspend/resume/reset conditions, remote wakeup, and stall condition clearing on Setup packets. The USB device controller also autonomously handles error conditions such as retry for CRC and data toggle errors, and generates NYET, STALL, ACK and NACK handshake responses, depending on the endpoint buffer status.

The LAN950x implements four USB endpoints: Control, Interrupt, Bulk-in, and Bulk-out. The Bulk-in and Bulk-out Endpoints allow for Ethernet reception and transmission respectively. Implementation of vendor-specific commands allows for efficient statistics gathering and access to the device's system control and status registers.

2.1.3 FIFO Controller

The FIFO controller uses an internal SRAM to buffer RX and TX traffic. Bulk-out packets from the USB controller are directly stored into the TX buffer. Ethernet Frames are directly stored into the RX buffer and become the basis for bulk-in packets.

2.1.4 Ethernet

The LAN950x integrates an IEEE 802.3 PHY for twisted pair Ethernet applications and a 10/100 Ethernet Media Access Controller (MAC).

The PHY can be configured for either 100 Mbps (100BASE-TX) or 10 Mbps (10BASE-T) Ethernet operation in either full- or half-duplex configurations and includes auto-negotiation, auto-polarity correction, and Auto-MDIX. Minimal external components are required for the utilization of the Integrated PHY.

Optionally, an external PHY may be used via the MII (Media Independent Interface) port, effectively bypassing the internal PHY. This option allows support for HomePNA and HomePlug applications.

The Ethernet MAC/PHY supports numerous power management wakeup features, including "Magic Packet", "Wake on LAN", and "Link Status Change". Eight wakeup frame filters are provided by LAN9500A/LAN9500Ai, while LAN9500/LAN9500i support four.

2.1.5 Power Management

The LAN950x features four (Note 2.1) variations of USB suspend: SUSPEND0, SUSPEND1, SUSPEND2, and SUSPEND3. These modes allow the application to select the ideal balance of remote wakeup functionality and power consumption.

- **SUSPEND0:** Supports GPIO, "Wake On LAN", and "Magic Packet" remote wakeup events. This suspend state reduces power by stopping the clocks of the MAC and other internal modules.
- **SUSPEND1:** Supports GPIO and "Link Status Change" for remote wakeup events. This suspend state consumes less power than SUSPEND0.
- **SUSPEND2:** Supports only GPIO assertion for a remote wakeup event. This is the default suspend mode for the device.
- **SUSPEND3:** (Note 2.1) Supports GPIO and "Good Packet" remote wakeup event. A "Good Packet" is a received frame passing certain filtering constraints independent of those imposed on "Wake On LAN" and "Magic Packet" frames. This suspend state consumes power at a level similar to the NORMAL state, however, it allows for power savings in the Host CPU.

Note 2.1 All four SUSPEND states are supported by LAN9500A/LAN9500Ai. SUSPEND3 is not supported by LAN9500/LAN9500i.

2.1.6 EEPROM Controller

The LAN950x contains an EEPROM controller for connection to an external EEPROM. This allows for the automatic loading of static configuration data upon power-on reset, pin reset, or software reset. The EEPROM can be configured to load USB descriptors, USB device configuration, and MAC address.

Custom operation without EEPROM is also provided (LAN9500A/LAN9500Ai only).

2.1.7 General Purpose I/O

When configured for internal PHY mode, up to eleven GPIOs are supported. All GPIOs can serve as remote wakeup events when the LAN950x is in a suspended state.

Chapter 3 Pin Description and Configuration

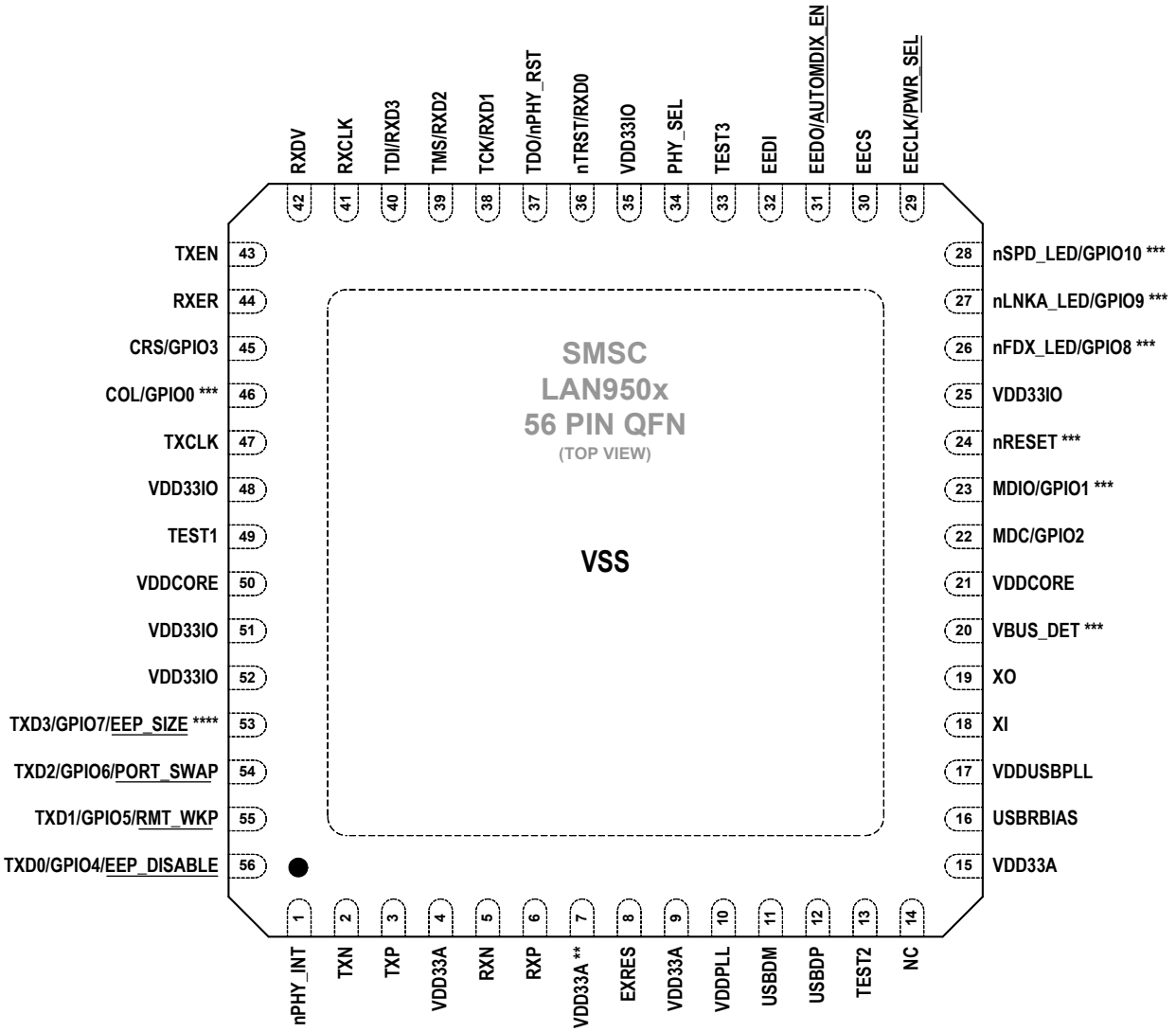


Figure 3.1 Pin Assignments (TOP VIEW)

Note: ** This pin is a no-connect (NC) for LAN9500A/LAN9500Ai, but may be connected to VDD33A for backward compatibility with LAN9500/LAN9500i.

Note: *** For LAN9500A/LAN9500Ai this pin provides additional PME related functionality. Refer to the respective pin descriptions and Chapter 6, "PME Operation," on page 41 for additional information.

Note: **** For LAN9500A/LAN9500Ai GPIO7 may provide additional PHY Link Up related functionality.

Note: When HP Auto-MDIX is activated, the TXN/TXP pins can function as RXN/RXP and vice-versa.

Note: Exposed pad (VSS) on bottom of package must be connected to ground.

Table 3.1 MII Interface Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Receive Error (External PHY Mode)	RXER	IS (PD)	In external PHY mode, the signal on this pin is input from the external PHY and indicates a receive error in the packet. In internal PHY mode, this pin is not used.
1	Transmit Enable (External PHY Mode)	TXEN	O8 (PD)	In external PHY mode, this pin functions as an output to the external PHY and indicates valid data on TXD[3:0]. In internal PHY mode, this pin is not used.
1	Receive Data Valid (External PHY Mode)	RXDV	IS (PD)	In external PHY mode, the signal on this pin is input from the external PHY and indicates valid data on RXD[3:0]. In internal PHY mode, this pin is not used.
1	Receive Clock (External PHY Mode)	RXCLK	IS (PD)	In external PHY mode, this pin is the receiver clock input from the external PHY. In internal PHY mode, this pin is not used.
1	Carrier Sense (External PHY Mode)	CRS	IS (PD)	In external PHY mode, the signal on this pin is input from the external PHY and indicates a network carrier.
	General Purpose I/O 3 (Internal PHY Mode Only)	GPIO3	IS/O8/ OD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input.
1	MII Collision Detect (External PHY Mode)	COL	IS (PD)	In external PHY mode, the signal on this pin is input from the external PHY and indicates a collision event.
	General Purpose I/O 0 (Internal PHY Mode Only)	GPIO0	IS/O8/ OD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input. **Note:** (LAN9500A/LAN9500Ai only) This pin may be used to signal PME when Internal PHY and PME modes of operation are in effect. Refer to Chapter 6, "PME Operation," on page 41 for additional information.

Table 3.1 MII Interface Pins (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Management Data (External PHY Mode)	MDIO	IS/O8 (PD)	In external PHY mode, this pin provides the management data to/from the external PHY.
	General Purpose I/O 1 (Internal PHY Mode Only)	GPIO1	IS/O8/ OD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input. **Note:** (LAN9500A/LAN9500Ai only) This pin may serve as the PME_MODE_SEL input when Internal PHY and PME modes of operation are in effect. Refer to Chapter 6, "PME Operation," on page 41 for additional information.
1	Management Clock (External PHY Mode)	MDC	O8 (PD)	In external PHY mode, this pin outputs the management clock to the external PHY.
	General Purpose I/O 2 (Internal PHY Mode Only)	GPIO2	IS/O8/ OD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input.
1	Transmit Data 3 (External PHY Mode)	TXD3	O8 (PU)	In external PHY mode, this pin functions as the transmit data 3 output to the external PHY.
	General Purpose I/O 7 (Internal PHY Mode Only)	GPIO7	IS/O8/ OD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input. **Note: (LAN9500A/LAN9500Ai ONLY):** GPIO7 may provide additional PHY Link Up related functionality.
1	EEPROM Size Configuration Strap	EEP_SIZE	IS (PU)	The EEP_SIZE strap selects the size of the EEPROM attached to the device. 0 = 128 byte EEPROM is attached and a total of seven address bits are used. 1 = 256/512 byte EEPROM is attached and a total of nine address bits are used. **Note:** A 3-wire style 1K/2K/4K EEPROM that is organized for 128 x 8-bit or 256/512 x 8-bit operation must be used. See Note 3.1 for more information on configuration straps.

Table 3.1 MII Interface Pins (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Transmit Data 2 (External PHY Mode)	TXD2	O8 (PD)	In external PHY mode, this pin functions as the transmit data 2 output to the external PHY.
	General Purpose I/O 6 (Internal PHY Mode Only)	GPIO6	IS/O8/ OD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input.
	USB Port Swap Configuration Strap	PORT_SWAP	IS (PD)	Swaps the mapping of USBDP and USBDM. 0 = USBDP maps to the USB D+ line and USBDM maps to the USB D- line. 1 = USBDP maps to the USB D- line. USBDM maps to the USB D+ line. See Note 3.1 for more information on configuration straps.
1	Transmit Data 1 (External PHY Mode)	TXD1	O8 (PD)	In external PHY mode, this pin functions as the transmit data 1 output to the external PHY.
	General Purpose I/O 5 (Internal PHY Mode Only)	GPIO5	IS/O8/ OD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input.
	Remote Wakeup Configuration Strap	RMT_WKP	IS (PD)	This strap configures the default descriptor values to support remote wakeup. 0 = Remote wakeup is not supported. 1 = Remote wakeup is supported. See Note 3.1 for more information on configuration straps.

Table 3.1 MII Interface Pins (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Transmit Data 0 (External PHY Mode)	TXD0	O8 (PD)	In external PHY mode, this pin functions as the transmit data 0 output to the external PHY.
	General Purpose I/O 4 (Internal PHY Mode Only)	GPIO4	IS/O8/ OD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input.
	EEPROM Disable Configuration Strap	EEP_DISABLE	IS (PD)	This strap disables the autoloading of the EEPROM contents. The assertion of this strap does not prevent register access to the EEPROM. 0 = EEPROM is recognized if present. 1 = EEPROM is not recognized even if it is present. See Note 3.1 for more information on configuration straps.
1	Transmit Clock (External PHY Mode)	TXCLK	IS (PU)	In external PHY mode, this pin is the transmitter clock input from the external PHY. In internal PHY mode, this pin is not used.

Note 3.1 Configuration strap values are latched on power-on reset and system reset. Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load.

Table 3.2 EEPROM Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	EEPROM Data In	EEDI	IS (PD)	This pin is driven by the EEDO output of the external EEPROM.
1	EEPROM Data Out	EEDO	O8 (PU)	This pin drives the EEDI input of the external EEPROM.
	Auto-MDIX Enable Configuration Strap	AUTOMDIX_EN	IS (PU)	Determines the default Auto-MDIX setting. 0 = Auto-MDIX is disabled. 1 = Auto-MDIX is enabled. See Note 3.2 for more information on configuration straps.

Table 3.2 EEPROM Pins (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	EEPROM Chip Select	EECS	O8	This pin drives the chip select output of the external EEPROM. **Note:** The EECS output may tri-state briefly during power-up. Some EEPROM devices may be prone to false selection during this time. When an EEPROM is used, an external pull-down resistor is recommended on this signal to prevent false selection. Refer to your EEPROM manufacturer's datasheet for additional information.
1	EEPROM Clock	EECLK	O8 (PD)	This pin drives the EEPROM clock of the external EEPROM.
1	Power Select Configuration Strap	PWR_SEL	IS (PD)	Determines the default power setting when no EEPROM is present. 0 = The device is bus powered. 1 = The device is self powered. See Note 3.2 for more information on configuration straps.

Note 3.2 Configuration strap values are latched on power-on reset and system reset. Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load.

Table 3.3 JTAG Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	JTAG Test Port Reset (Internal PHY Mode)	nTRST	IS (PU)	In internal PHY mode, this active-low pin functions as the JTAG test port reset input.
	Receive Data 0 (External PHY Mode)	RXD0	IS (PD)	In external PHY mode, this pin functions as the receive data 0 input from the external PHY.
1	JTAG Test Data Out (Internal PHY Mode)	TDO	O8	In internal PHY mode, this pin functions as the JTAG data output.
	PHY Reset (External PHY Mode)	nPHY_RST	O8	In external PHY mode, this active-low pin functions as the PHY reset output.

Table 3.3 JTAG Pins (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	JTAG Test Clock (Internal PHY Mode)	TCK	IS (PU)	In internal PHY mode, this pin functions as the JTAG test clock. The maximum operating frequency of this clock is 25MHz.
	Receive Data 1 (External PHY Mode)	RXD1	IS (PD)	In external PHY mode, this pin functions as the receive data 1 input from the external PHY.
1	JTAG Test Mode Select (Internal PHY Mode)	TMS	IS (PU)	In internal PHY mode, this pin functions as the JTAG test mode select.
	Receive Data 2 (External PHY Mode)	RXD2	IS (PD)	In external PHY mode, this pin functions as the receive data 2 input from the external PHY.
1	JTAG Test Data Input (Internal PHY Mode)	TDI	IS (PU)	In internal PHY mode, this pin functions as the JTAG data input.
	Receive Data 3 (External PHY Mode)	RXD3	IS (PD)	In external PHY mode, this pin functions as the receive data 3 input from the external PHY.

Table 3.4 Miscellaneous Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	PHY Select	PHY_SEL	IS (PD)	Selects whether to use the internal Ethernet PHY or the external PHY connected to the MII port. 0 = Internal PHY is used. 1 = External PHY is used.
1	System Reset	nRESET	IS (PU)	This active-low pin allows external hardware to reset the device. **Note:** (LAN9500A/LAN9500Ai only) This pin may be used to signal PME_CLEAR when PME mode of operation is in effect. Refer to Chapter 6, "PME Operation," on page 41 for additional information.

Table 3.4 Miscellaneous Pins (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Ethernet Full-Duplex Indicator LED	nFDX_LED	OD12 (PU)	This pin is driven low (LED on) when the Ethernet link is operating in full-duplex mode.
	General Purpose I/O 8	GPIO8	IS/O12/ OD12 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input. **Note:** (LAN9500A/LAN9500Ai only) This pin may be used to signal PME when External PHY and PME modes of operation are in effect. Refer to Chapter 6, "PME Operation," on page 41 for additional information. **Note:** By default this pin is configured as a GPIO.
1	Ethernet Link Activity Indicator LED	nLNKA_LED	OD12 (PU)	This pin is driven low (LED on) when a valid link is detected. This pin is pulsed high (LED off) for 80mS whenever transmit or receive activity is detected. This pin is then driven low again for a minimum of 80mS, after which time it will repeat the process if TX or RX activity is detected. Effectively, LED2 is activated solid for a link. When transmit or receive activity is sensed, LED2 will function as an activity indicator.
	General Purpose I/O 9	GPIO9	IS/O12/ OD12 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input. **Note:** (LAN9500A/LAN9500Ai only) This pin may serve as the PME_MODE_SEL input when External PHY and PME modes of operation are in effect. Refer to Chapter 6, "PME Operation," on page 41 for additional information. **Note:** By default this pin is configured as a GPIO.

Table 3.4 Miscellaneous Pins (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Ethernet Speed Indicator LED	nSPD_LED	OD12 (PU)	This pin is driven low (LED on) when the Ethernet operating speed is 100Mbs, or during auto-negotiation. This pin is driven high during 10Mbs operation, or during line isolation.
	General Purpose I/O 10	GPIO10	IS/O12/ OD12 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input. **Note:** (LAN9500A/LAN9500Ai only) This pin may serve as a wakeup pin whose detection mode is selectable when External PHY and PME modes of operation are in effect. Refer to Chapter 6, "PME Operation," on page 41 for additional information. **Note:** By default this pin is configured as a GPIO.
1	Detect Upstream VBUS Power	VBUS_DET	IS_5V (PD)	Detects state of upstream bus power. For bus powered applications, this pin must be tied to VDD33IO. For self powered applications where the device is permanently attached to a host, VBUS_DET should be pulled to VDD33IO. For other self powered applications, refer to the device reference schematic for additional connection information. **Note:** (LAN9500A/LAN9500Ai only) This pin may be used to signal bus power availability when PME mode of operation is in effect. Refer to Chapter 6, "PME Operation," on page 41 for additional information.
1	Test 1	TEST1	-	This pin must always be connected to VDD33IO for proper operation.
1	Test 2	TEST2	-	This pin must always be connected to VSS for proper operation.
1	Test 3	TEST3	-	This pin must always be connected to VSS for proper operation.

Table 3.5 USB Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	USB DMINUS	USBDM	AIO	**Note:** The functionality of this pin may be swapped to USB DPLUS via the PORT_SWAP configuration strap.
1	USB DPLUS	USBDP	AIO	**Note:** The functionality of this pin may be swapped to USB DMINUS via the PORT_SWAP configuration strap.
1	External USB Bias Resistor.	USBRBIAS	AI	Used for setting HS transmit current level and on-chip termination impedance. Connect to an external 12K 1.0% resistor to ground.
1	USB PLL Supply	VDDUSBPLL	P	This pin must be connected to VDDCORE for proper operation. Refer to Chapter 4, "Power Connections," on page 25 and the device reference schematic for additional connection information.
1	Crystal Input	XI	ICLK	External 25 MHz crystal input. **Note:** This pin can also be driven by a single-ended clock oscillator. When this method is used, XO should be left unconnected
1	Crystal Output	XO	OCLK	External 25 MHz crystal output.

Table 3.6 Ethernet PHY Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Ethernet TX Data Out Negative	TXN	AIO	The transmit data outputs may be swapped internally with receive data inputs when Auto-MDIX is enabled.
1	Ethernet TX Data Out Positive	TXP	AIO	The transmit data outputs may be swapped internally with receive data inputs when Auto-MDIX is enabled.
1	Ethernet RX Data In Negative	RXN	AIO	The receive data inputs may be swapped internally with transmit data outputs when Auto-MDIX is enabled.
1	Ethernet RX Data In Positive	RXP	AIO	The receive data inputs may be swapped internally with transmit data outputs when Auto-MDIX is enabled.

Table 3.6 Ethernet PHY Pins (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	PHY Interrupt (Internal PHY Mode)	nPHY_INT	O8	In internal PHY mode, this pin can be configured to output the internal PHY interrupt signal. **Note:** The internal PHY interrupt signal is active-high.
	PHY Interrupt (External PHY Mode)	nPHY_INT	IS (PU)	In external PHY mode, the active-low signal on this pin is input from the external PHY and indicates a PHY interrupt has occurred.
4	+3.3V Analog Power Supply	VDD33A	P	Refer to the device reference schematic for connection information. **Note:** Pin 7 is a no-connect (NC) for LAN9500A/LAN9500Ai, but may be connected to VDD33A for backward compatibility with LAN9500/LAN9500i.
1	External PHY Bias Resistor	EXRES	AI	Used for the internal bias circuits. Connect to an external resistor to ground. For LAN9500A/LAN9500Ai use 12.0K, 1%. For LAN9500/LAN9500i use 12.4K, 1%.
1	Ethernet PLL Power Supply	VDDPLL	P	This pin must be connected to VDDCORE for proper operation. Refer to Chapter 4, "Power Connections," on page 25 and the device reference schematic for additional connection information.

Table 3.7 I/O Power Pins, Core Power Pins, and Ground Pad

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
5	+3.3V I/O Power	VDD33IO	P	Refer to the device reference schematic for connection information.
2	Digital Core Power Supply Output	VDDCORE	P	Refer to Chapter 4, "Power Connections," on page 25 and the device reference schematic for connection information.
Exposed pad on package bottom (Figure 3.1)	Ground	VSS	P	Common Ground

Table 3.8 No-Connect Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	No Connect	NC	-	These pins must be left floating for normal device operation.

3.1 Pin Assignments

Table 3.9 56-QFN Package Pin Assignments

PIN NUM	PIN NAME	PIN NUM	PIN NAME	PIN NUM	PIN NAME	PIN NUM	PIN NAME
1	nPHY_INT	15	VDD33A	29	EECLK/ PWR_SEL	43	TXEN
2	TXN	16	USBRBIAS	30	EECS	44	RXER
3	TXP	17	VDDUSBPLL	31	EEDO/ AUTOMDIX_EN	45	CRS/GPIO3
4	VDD33A	18	XI	32	EEDI	46	COL/GPIO0 Note 3.4
5	RXN	19	XO	33	TEST3	47	TXCLK
6	RXP	20	VBUS_DET Note 3.4	34	PHY_SEL	48	VDD33IO
7	VDD33A Note 3.3	21	VDDCORE	35	VDD33IO	49	TEST1
8	EXRES	22	MDC/GPIO2	36	nTRST/RXD0	50	VDDCORE
9	VDD33A	23	MDIO/GPIO1 Note 3.4	37	TDO/nPHY_RST	51	VDD33IO
10	VDDPLL	24	nRESET Note 3.4	38	TCK/RXD1	52	VDD33IO
11	USBDM	25	VDD33IO	39	TMS/RXD2	53	TXD3/GPIO7/ EEP_SIZE
12	USBDP	26	nFDX_LED/ GPIO8 Note 3.4	40	TDI/RXD3	54	TXD2/GPIO6/ PORT_SWAP
13	TEST2	27	nLNKA_LED/ GPIO9 Note 3.4	41	RXCLK	55	TXD1/GPIO5/ RMT_WKP
14	NC	28	nSPD_LED/ GPIO10 Note 3.4	42	RXDV	56	TXD0/GPIO4/ EEP_DISABLE
EXPOSED PAD MUST BE CONNECTED TO VSS							

Note 3.3 This pin is a no-connect (NC) for LAN9500A/LAN9500Ai, but may be connected to VDD33A for backward compatibility with LAN9500/LAN9500i.

Note 3.4 For LAN9500A/LAN9500Ai this pin provides additional PME related functionality. Refer to the respective pin descriptions and Chapter 6, "PME Operation," on page 41 for additional information.

3.2 Buffer Types

Table 3.10 Buffer Types

BUFFER TYPE	DESCRIPTION
IS	Schmitt-triggered Input
IS_5V	5V Tolerant Schmitt-triggered Input
O8	Output with 8mA sink and 8mA source
OD8	Open-drain output with 8mA sink
O12	Output with 12mA sink and 12mA source
OD12	Open-drain output with 12mA sink
PU	50uA (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. **Note:** Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
PD	50uA (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. **Note:** Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
AI	Analog input
AIO	Analog bi-directional
ICLK	Crystal oscillator input pin
OCLK	Crystal oscillator output pin
P	Power pin

Chapter 4 Power Connections

Figure 4.1 illustrates the power connections for LAN950x.

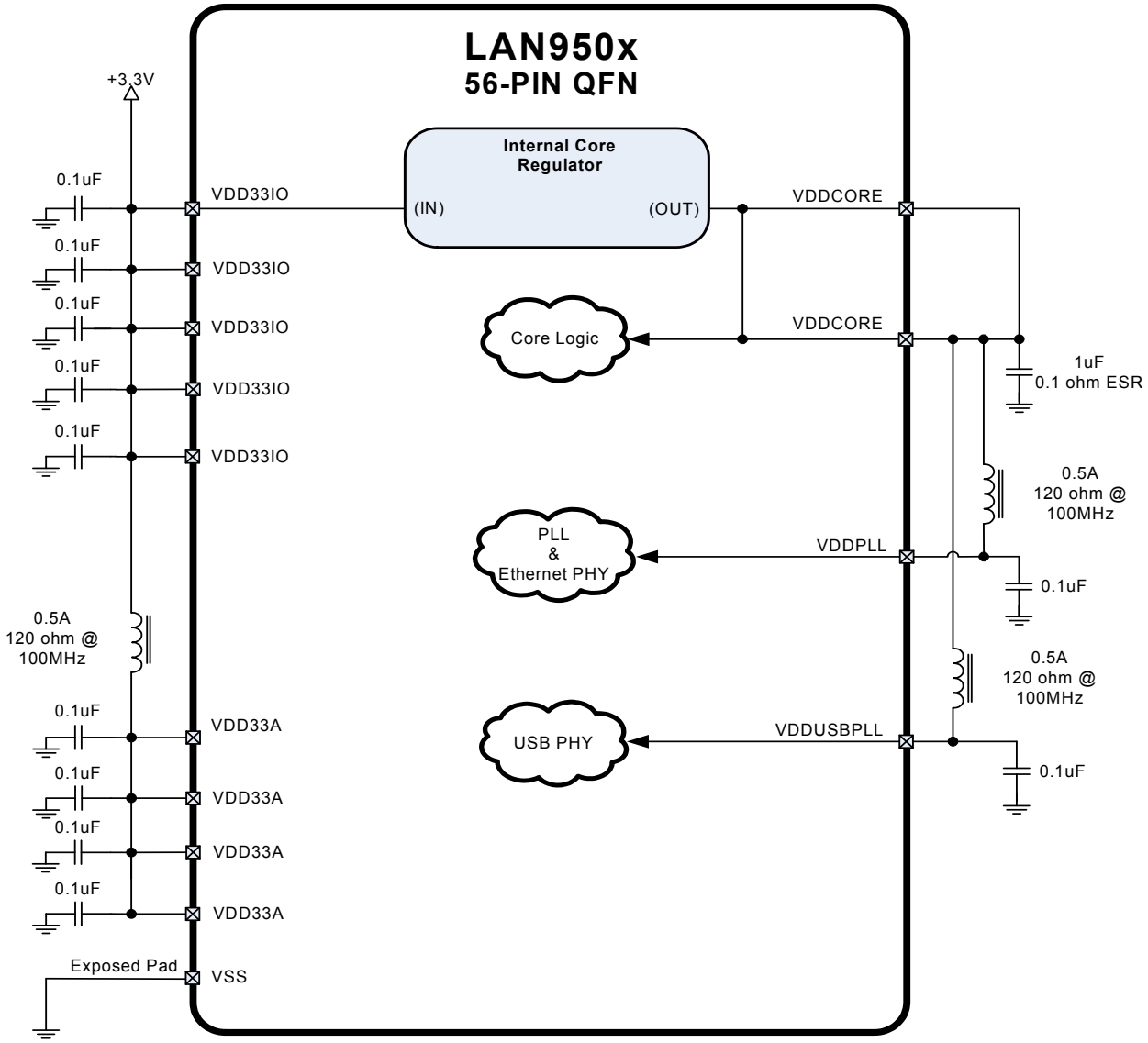


Figure 4.1 Power Connections

Chapter 5 EEPROM Controller (EPC)

LAN950x may use an external EEPROM to store the default values for the USB descriptors and the MAC address. The EEPROM controller supports most “93C46” type EEPROMs. The EEP_SIZE strap selects the size of the EEPROM attached to the device. When this strap is set to “0”, a 128 byte EEPROM is attached and a total of seven address bits are used. When this strap is set to “1” a 256/512 byte EEPROM is attached and a total of nine address bits are used.

Note: A 3-wire style 1K/2K/4K EEPROM that is organized for 128 x 8-bit or 256/512 x 8-bit operation must be used.

The MAC address is used as the default Ethernet MAC address and is loaded into the MAC’s ADDRH and ADDRL registers. If a properly configured EEPROM is not detected, it is the responsibility of the Host LAN Driver to set the IEEE addresses.

After a system-level reset occurs, the device will load the default values from a properly configured EEPROM. The device will not accept USB transactions from the Host until this process is completed.

The device’s EEPROM controller also allows the Host system to read, write and erase the contents of the Serial EEPROM.

5.1 EEPROM Format

Table 5.1 illustrates the format in which data is stored inside of the EEPROM.

Note the EEPROM offsets are given in units of 16-bit word offsets. A length field with a value of zero indicates that the field does not exist in the EEPROM. The device will use the field’s HW default value in this case.

Note: For the device descriptor, the only valid values for the length are 0 and 18.

Note: For the configuration and interface descriptor, the only valid values for the length are 0 and 18.

Note: The EEPROM programmer must ensure that if a string descriptor does not exist in the EEPROM, the referencing descriptor must contain 00h for the respective string index field.

Note: If all string descriptor lengths are zero, then a Language ID will not be supported.

Table 5.1 EEPROM Format

EEPROM ADDRESS	EEPROM CONTENTS
00h	0xA5
01h	MAC Address [7:0]
02h	MAC Address [15:8]
03h	MAC Address [23:16]
04h	MAC Address [31:24]
05h	MAC Address [39:32]
06h	MAC Address [47:40]
07h	Full-Speed Polling Interval for Interrupt Endpoint
08h	Hi-Speed Polling Interval for Interrupt Endpoint

Table 5.1 EEPROM Format (continued)

EEPROM ADDRESS	EEPROM CONTENTS
09h	Configuration Flags
0Ah	Language ID Descriptor [7:0]
0Bh	Language ID Descriptor [15:8]
0Ch	Manufacturer ID String Descriptor Length (bytes)
0Dh	Manufacturer ID String Descriptor EEPROM Word Offset
0Eh	Product Name String Descriptor Length (bytes)
0Fh	Product Name String Descriptor EEPROM Word Offset
10h	Serial Number String Descriptor Length (bytes)
11h	Serial Number String Descriptor EEPROM Word Offset
12h	Configuration String Descriptor Length (bytes)
13h	Configuration String Descriptor Word Offset
14h	Interface String Descriptor Length (bytes)
15h	Interface String Descriptor Word Offset
16h	Hi-Speed Device Descriptor Length (bytes)
17h	Hi-Speed Device Descriptor Word Offset
18h	Hi-Speed Configuration and Interface Descriptor Length (bytes)
19h	Hi-Speed Configuration and Interface Descriptor Word Offset
1Ah	Full-Speed Device Descriptor Length (bytes)
1Bh	Full-Speed Device Descriptor Word Offset
1Ch	Full-Speed Configuration and Interface Descriptor Length (bytes)
1Dh	Full-Speed Configuration and Interface Descriptor Word Offset
1Eh	**(LAN9500A/LAN9500Ai Only)** GPIO7:0 Wakeup Enables Bit x = 0 -> GPIOx Pin Disabled for Wakeup Use. Bit x = 1 -> GPIOx Pin Enabled for Wakeup Use.
1Fh	**(LAN9500A/LAN9500Ai Only)** GPI010:8 Wakeup Enables Bit x = 0 -> GPIO(x+8) Pin Disabled for Wakeup Use. Bit x = 1 -> GPIO(x+8) Pin Enabled for Wakeup Use. **Note:** Bits 7:3 Unused.
20h	**(LAN9500A/LAN9500Ai Only)** GPIO PME Flags

Note: EEPROM byte addresses past the indicated address can be used to store data for any purpose:
LAN9500/LAN9500i - 1Dh
LAN9500A/LAN9500Ai - 20h

Table 5.2 describes the Configuration Flags.

Table 5.2 Configuration Flags

<table>
<tr><th>BITS</th><th>DESCRIPTION</th></tr>
<tr><td>7:6</td><td>RESERVED</td></tr>
<tr><td>5:4</td><td>(LAN9500A/LAN9500Ai Only, Otherwise RESERVED)

PHY Boost
This field provides the ability to boost the electrical drive strength of the HS output current to the upstream port.

00 = Normal electrical drive strength.
01 = Elevated electrical drive strength (+4% boost).
10 = Elevated electrical drive strength (+8% boost).
11 = Elevated electrical drive strength (+12% boost).</td></tr>
<tr><td>3</td><td>RESERVED</td></tr>
<tr><td>2</td><td>Remote Wakeup Support
0 = The device does not support remote wakeup.
1 = The device supports remote wakeup.</td></tr>
<tr><td>1</td><td>(LAN9500A/LAN9500Ai Only, Otherwise RESERVED)

LED Select
This bit determines the functionality of external LED pins.

<table>
<tr><th>BIT VALUE</th><th>PIN NAME</th><th>FUNCTION</th></tr>
<tr><td rowspan="3">0</td><td>nSPD_LED</td><td>Speed Indicator</td></tr>
<tr><td>nLNKA_LED</td><td>Link and Activity Indicator</td></tr>
<tr><td>nFDX_LED</td><td>Full Duplex Link Indicator</td></tr>
<tr><td rowspan="3">1</td><td>nSPD_LED</td><td>Speed Indicator</td></tr>
<tr><td>nLNKA_LED</td><td>Link Indicator</td></tr>
<tr><td>nFDX_LED</td><td>Activity Indicator</td></tr>
</table>
</td></tr>
<tr><td>0</td><td>Power Method
0 = The device is bus powered.
1 = The device is self powered.</td></tr>
</table>

Table 5.3 describes the GPIO PME flags **(LAN9500A/LAN9500Ai Only)**.

Table 5.3 GPIO PME Flags

BITS	DESCRIPTION
7	**GPIO PME Enable** Setting this bit enables the assertion of the GPIO0 or GPIO8 pin, as a result of a Wakeup (GPIO) pin, Magic Packet, or PHY Link Up. The host processor may use the GPIO0/GPIO8 pin to asynchronously wake up, in a manner analogous to a PCI PME pin. GPIO0 signals the event when operating in Internal PHY mode, while GPIO8 signals the event when operating in External PHY mode. Internal or External PHY mode of operation is dictated by the PHY_SEL pin. 0 = The device does not support GPIO PME signaling. 1 = The device supports GPIO PME signaling. **Note:** When this bit is 0, the remaining GPIO PME parameters in this flag byte are ignored.
6	**GPIO PME Configuration** This bit selects whether the GPIO PME is signaled on the GPIO pin as a level or a pulse. If pulse is selected, the duration of the pulse is determined by the setting of the GPIO PME Length bit of this flag byte. The level of the signal or the polarity of the pulse is determined by the GPIO PME Polarity bit of this flag byte. 0 = GPIO PME is signaled via a level. 1 = GPIO PME is signaled via a pulse. **Note:** If GPIO PME Enable is 0, this bit is ignored.
5	**GPIO PME Length** When the GPIO PME Configuration bit of this flag byte indicates that the GPIO PME is signaled by a pulse on the GPIO pin, this bit determines the duration of the pulse. 0 = GPIO PME pulse length is 1.5 mS. 1 = GPIO PME pulse length is 150 mS. **Note:** If GPIO PME Enable is 0, this bit is ignored.
4	**GPIO PME Polarity** Specifies the level of the signal or the polarity of the pulse used for GPIO PME signaling. 0 = GPIO PME signaling polarity is low. 1 = GPIO PME signaling polarity is high. **Note:** If GPIO PME Enable is 0, this bit is ignored.
3	**GPIO PME Buffer Type** This bit selects the output buffer type for GPIO0/GPIO8. 0 = Open drain driver / open source 1 = Push-Pull driver **Note:** Buffer Type = 0, Polarity = 0 implies Open Drain Buffer Type = 0, Polarity = 1 implies Open Source **Note:** If GPIO PME Enable is 0, this bit is ignored.
2	**GPIO PME WOL Select** Three types of wakeup events are supported; Magic Packet, PHY Link Up, and Wakeup Pin(s) assertion. Wakeup Pin(s) are selected via the GPIO Wakeup Enables specified in bytes 1Eh and 1Fh of the EEPROM. This bit selects whether Magic packet or Link Up wakeup events are supported. 0 = Magic packet wakeup supported. 1 = PHY linkup wakeup supported. (not supported in External PHY mode) **Note:** If GPIO PME Enable is 0, this bit is ignored.

Table 5.3 GPIO PME Flags (continued)

BITS	DESCRIPTION
1	**GPIO10 Detection Select** This bit selects the detection mode for GPIO10 when operating in PME mode. In PME mode, GPIO10 is usable in both Internal and External PHY mode as a wakeup pin. This parameter defines whether the wakeup should occur on an active high or active low signal. 0 = Active-low detection for GPIO10. 1 = Active-high detection for GPIO10. **Note:** If GPIO PME Enable is 0, this bit is ignored.
0	**RESERVED**

5.2 EEPROM Defaults

The signature value of 0xA5 is stored at address 0. A different signature value indicates to the EEPROM controller that no EEPROM or an un-programmed EEPROM is attached to the device. In this case, the hardware default values are used, as shown in Table 5.4.

Table 5.4 EEPROM Defaults

FIELD	DEFAULT VALUE
MAC Address	FFFFFFFFFFFFh
Full-Speed Polling Interval (mS)	01h
Hi-Speed Polling Interval (mS)	04h
Configuration Flags	04h
Maximum Power (mA)	FAh
Vendor ID	0424h
Product ID	DEVICE / PRODUCT ID LAN9500/LAN9500i — 9500h LAN9500A/LAN9500Ai — 9E00h

Note: The Configuration Flags are affected by the PWR_SEL and RMT_WKP straps.

5.3 EEPROM Auto-Load

Certain system level resets (USB reset, POR, nRESET, and SRST) cause the EEPROM contents to be loaded into the device. After a reset, the EEPROM controller attempts to read the first byte of data from the EEPROM. If the value 0xA5 is read from the first address, then the EEPROM controller will assume that an external Serial EEPROM is present.

Note: The USB reset only loads the MAC address.

5.4 Examples of EEPROM Format Interpretation

5.4.1 LAN9500/LAN9500i

Table 5.5 and Table 5.6 provide an example of how the contents of a EEPROM are formatted in the case of LAN9500/LAN9500i. Table 5.5 is a dump of the EEPROM memory (256-byte EEPROM), while Table 5.6 illustrates, byte by byte, how the EEPROM is formatted.

Table 5.5 Dump of EEPROM Memory - LAN9500/LAN9500i

OFFSET BYTE	VALUE
0000h	A5 12 34 56 78 9A BC 01
0008h	04 04 09 04 0A 0F 10 14
0010h	10 1C 00 00 00 00 12 24
0018h	12 2D 12 36 12 3F 0A 03
0020h	53 00 4D 00 53 00 43 00
0028h	10 03 4C 00 41 00 4E 00
0030h	39 00 35 00 30 00 30 00
0038h	10 03 30 00 30 00 30 00
0040h	35 00 31 00 32 00 33 00
0048h	12 01 00 02 FF 00 01 40
0050h	24 04 00 95 00 01 01 02
0058h	03 01 09 02 27 00 01 01
0060h	00 A0 FA 09 04 00 00 03
0068h	FF 00 FF 00 12 01 00 02
0070h	FF 00 01 40 24 04 00 95
0078h	00 01 01 02 03 01 09 02
0080h	27 00 01 01 00 A0 FA 09
0088h	04 00 00 03 FF 00 FF 00
0090h - 00FFh	.....

Table 5.6 EEPROM Example - 256 Byte EEPROM - LAN9500/LAN9500i

EEPROM ADDRESS	EEPROM CONTENTS (HEX)	DESCRIPTION
00h	A5	EEPROM Programmed Indicator
01h - 06h	12 34 56 78 9A BC	MAC Address 12 34 56 78 9A BC
07h	01	Full-Speed Polling Interval for Interrupt Endpoint (1ms)
08h	04	Hi-Speed Polling Interval for Interrupt Endpoint (4ms)
09h	04	Configuration Flags - The device is bus powered and supports remote wakeup.
0Ah - 0Bh	09 04	Language ID Descriptor 0409h, English
0Ch	0A	Manufacturer ID String Descriptor Length (10 bytes)
0Dh	0F	Manufacturer ID String Descriptor EEPROM Word Offset (0Fh) Corresponds to EEPROM Byte Offset 1Eh
0Eh	10	Product Name String Descriptor Length (16 bytes)
0Fh	14	Product Name String Descriptor EEPROM Word Offset (14h) Corresponds to EEPROM Byte Offset 28h
10h	10	Serial Number String Descriptor Length (16 bytes)
11h	1C	Serial Number String Descriptor EEPROM Word Offset (1Ch) Corresponds to EEPROM Byte Offset 38h
12h	00	Configuration String Descriptor Length (0 bytes - NA)
13h	00	Configuration String Descriptor Word Offset (Don’t Care)
14h	00	Interface String Descriptor Length (0 bytes - NA)
15h	00	Interface String Descriptor Word Offset (Don’t Care)
16h	12	Hi-Speed Device Descriptor Length (18 bytes)
17h	24	Hi-Speed Device Descriptor Word Offset (24h) Corresponds to EEPROM Byte Offset 48h
18h	12	Hi-Speed Configuration and Interface Descriptor Length (18 bytes)
19h	2D	Hi-Speed Configuration and Interface Descriptor Word Offset (2Dh) Corresponds to EEPROM Byte Offset 5Ah
1Ah	12	Full-Speed Device Descriptor Length (18 bytes)
1Bh	36	Full-Speed Device Descriptor Word Offset (36h) Corresponds to EEPROM Byte Offset 6Ch
1Ch	12	Full-Speed Configuration and Interface Descriptor Length (18bytes)
1Dh	3F	Full-Speed Configuration and Interface Descriptor Word Offset (3Fh) Corresponds to EEPROM Byte Offset 7Eh
1Eh	0A	Size of Manufacturer ID String Descriptor (10 bytes)

Table 5.6 EEPROM Example - 256 Byte EEPROM - LAN9500/LAN9500i (continued)

EEPROM ADDRESS	EEPROM CONTENTS (HEX)	DESCRIPTION
1Fh	03	Descriptor Type (String Descriptor - 03h)
20h-27h	53 00 4D 00 53 00 43 00	Manufacturer ID String (“SMSC” in UNICODE)
28h	10	Size of Product Name String Descriptor (16 bytes)
29h	03	Descriptor Type (String Descriptor - 03h)
2Ah-37h	4C 00 41 00 4E 00 39 00 35 00 30 00 30 00	Product Name String (“LAN9500” in UNICODE)
38h	10	Size of Serial Number String Descriptor (16 bytes)
39h	03	Descriptor Type (String Descriptor - 03h)
3Ah-47h	30 00 30 00 30 00 35 00 31 00 32 00 33 00	Serial Number String (“0005123” in UNICODE)
48h	12	Size of Hi-Speed Device Descriptor in Bytes (18 bytes)
49h	01	Descriptor Type (Device Descriptor - 01h)
4Ah-4Bh	00 02	USB Specification Number that the device complies with (0200h)
4Ch	FF	Class Code
4Dh	00	Subclass Code
4Eh	01	Protocol Code
4Fh	40	Maximum Packet Size for Endpoint 0
50h-51h	24 04	Vendor ID (0424h)
52h-53h	00 95	Product ID (9500h)
54h-55h	00 01	Device Release Number (0100h)
56h	01	Index of Manufacturer String Descriptor
57h	02	Index of Product String Descriptor
58h	03	Index of Serial Number String Descriptor
59h	01	Number of Possible Configurations
5Ah	09	Size of Hi-Speed Configuration Descriptor in bytes (9 bytes)
5Bh	02	Descriptor Type (Configuration Descriptor - 02h)
5Ch-5Dh	27 00	Total length in bytes of data returned (0027h = 39 bytes)
5Eh	01	Number of Interfaces
5Fh	01	Value to use as an argument to select this configuration
60h	00	Index of String Descriptor describing this configuration
61h	A0	Bus powered and remote wakeup enabled

Table 5.6 EEPROM Example - 256 Byte EEPROM - LAN9500/LAN9500i (continued)

EEPROM ADDRESS	EEPROM CONTENTS (HEX)	DESCRIPTION
62h	FA	Maximum Power Consumption is 500 mA
63h	09	Size of Descriptor in Bytes (9 Bytes)
64h	04	Descriptor Type (Interface Descriptor - 04h)
65h	00	Number identifying this Interface
66h	00	Value used to select alternative setting
67h	03	Number of Endpoints used for this interface (Less endpoint 0)
68h	FF	Class Code
69h	00	Subclass Code
6Ah	FF	Protocol Code
6Bh	00	Index of String Descriptor Describing this interface
6Ch	12	Size of Full-Speed Device Descriptor in Bytes (18 Bytes)
6Dh	01	Descriptor Type (Device Descriptor - 01h)
6Eh-6Fh	00 02	USB Specification Number that the device complies with (0200h)
70h	FF	Class Code
71h	00	Subclass Code
72h	01	Protocol Code
73h	40	Maximum Packet Size for Endpoint 0
74h-75h	24 04	Vendor ID (0424h)
76h-77h	00 95	Product ID (9500h)
78h-79h	00 01	Device Release Number (0100h)
7Ah	01	Index of Manufacturer String Descriptor
7Bh	02	Index of Product String Descriptor
7Ch	03	Index of Serial Number String Descriptor
7Dh	01	Number of Possible Configurations
7Eh	09	Size of Full-Speed Configuration Descriptor in bytes (9 bytes)
7Fh	02	Descriptor Type (Configuration Descriptor - 02h)
80h-81h	27 00	Total length in bytes of data returned (0027h = 39 bytes)
82h	01	Number of Interfaces
83h	01	Value to use as an argument to select this configuration
84h	00	Index of String Descriptor describing this configuration

Table 5.6 EEPROM Example - 256 Byte EEPROM - LAN9500/LAN9500i (continued)

EEPROM ADDRESS	EEPROM CONTENTS (HEX)	DESCRIPTION
85h	A0	Bus powered and remote wakeup enabled
86h	FA	Maximum Power Consumption is 500 mA
87h	09	Size of Full-Speed Interface Descriptor in Bytes (9 Bytes)
88h	04	Descriptor Type (Interface Descriptor - 04h)
89h	00	Number identifying this Interface
8Ah	00	Value used to select alternative setting
8Bh	03	Number of Endpoints used for this interface (Less endpoint 0)
8Ch	FF	Class Code
8Dh	00	Subclass Code
8Eh	FF	Protocol Code
8Fh	00	Index of String Descriptor Describing this interface
90h- FFh	-	Data storage for use by Host as desired

5.4.2 LAN9500A/LAN9500Ai

Table 5.7 and Table 5.8 provide an example of how the contents of a EEPROM are formatted in the case of LAN9500A/LAN9500Ai. Table 5.7 is a dump of the EEPROM memory (256-byte EEPROM), while Table 5.8 illustrates, byte by byte, how the EEPROM is formatted.

Table 5.7 Dump of EEPROM Memory - LAN9500A/LAN9500Ai

OFFSET BYTE	VALUE
0000h	A5 12 34 56 78 9A BC 01
0008h	04 04 09 04 0A 11 12 16
0010h	10 1F 00 00 00 00 12 27
0018h	12 30 12 39 12 42 00 04
0020h	8A 00 0A 03 53 00 4D 00
0028h	53 00 43 00 12 03 4C 00
0030h	41 00 4E 00 39 00 35 00
0038h	30 00 30 00 41 00 10 03
0040h	30 00 30 00 30 00 35 00
0048h	31 00 32 00 33 00 12 01

Table 5.7 Dump of EEPROM Memory - LAN9500A/LAN9500Ai (continued)

OFFSET BYTE	VALUE
0050h	00 02 FF 00 FF 40 24 04
0058h	00 9E 00 01 01 02 03 01
0060h	09 02 27 00 01 01 00 A0
0068h	FA 09 04 00 00 03 FF 00
0070h	FF 00 12 01 00 02 FF 00
0078h	FF 40 24 04 00 9E 00 01
0080h	01 02 03 01 09 02 27 00
0088h	01 01 00 A0 FA 09 04 00
0090h - 00FFh	00 03 FF 00 FF 00 .....

Table 5.8 EEPROM Example - 256 Byte EEPROM - LAN9500A/LAN9500Ai

EEPROM ADDRESS	EEPROM CONTENTS (HEX)	DESCRIPTION
00h	A5	EEPROM Programmed Indicator
01h - 06h	12 34 56 78 9A BC	MAC Address 12 34 56 78 9A BC
07h	01	Full-Speed Polling Interval for Interrupt Endpoint (1ms)
08h	04	Hi-Speed Polling Interval for Interrupt Endpoint (4ms)
09h	04	Configuration Flags - No PHY Boost, the device is bus powered and supports remote wakeup, nSPD_LED = Speed Indicator, nLNKA_LED = Link and Activity Indicator, nFDX_LED = Full Duplex Link Indicator.
0Ah - 0Bh	09 04	Language ID Descriptor 0409h, English
0Ch	0A	Manufacturer ID String Descriptor Length (10 bytes)
0Dh	11	Manufacturer ID String Descriptor EEPROM Word Offset (11h) Corresponds to EEPROM Byte Offset 22h
0Eh	12	Product Name String Descriptor Length (18 bytes)
0Fh	16	Product Name String Descriptor EEPROM Word Offset (16h) Corresponds to EEPROM Byte Offset 2Ch
10h	10	Serial Number String Descriptor Length (16 bytes)
11h	1F	Serial Number String Descriptor EEPROM Word Offset (1Fh) Corresponds to EEPROM Byte Offset 3Eh
12h	00	Configuration String Descriptor Length (0 bytes - NA)
13h	00	Configuration String Descriptor Word Offset (Don’t Care)

Table 5.8 EEPROM Example - 256 Byte EEPROM - LAN9500A/LAN9500Ai (continued)

EEPROM ADDRESS	EEPROM CONTENTS (HEX)	DESCRIPTION
14h	00	Interface String Descriptor Length (0 bytes - NA)
15h	00	Interface String Descriptor Word Offset (Don't Care)
16h	12	Hi-Speed Device Descriptor Length (18 bytes)
17h	27	Hi-Speed Device Descriptor Word Offset (27h) Corresponds to EEPROM Byte Offset 4Eh
18h	12	Hi-Speed Configuration and Interface Descriptor Length (18 bytes)
19h	30	Hi-Speed Configuration and Interface Descriptor Word Offset (30h) Corresponds to EEPROM Byte Offset 60h
1Ah	12	Full-Speed Device Descriptor Length (18 bytes)
1Bh	39	Full-Speed Device Descriptor Word Offset (39h) Corresponds to EEPROM Byte Offset 72h
1Ch	12	Full-Speed Configuration and Interface Descriptor Length (18bytes)
1Dh	42	Full-Speed Configuration and Interface Descriptor Word Offset (42h) Corresponds to EEPROM Byte Offset 84h
1Eh	00	GPIO7:0 Wake Enables - GPIO7:0 Not Used For Wakeup Signaling
1Fh	04	GPIO10:8 Wake Enables - GPIO10 Used For Wakeup Signaling
20h	8A	GPIO PME Flags - PME Signaling Enabled via Low Level, Push-Pull Driver, GPIO10 Active High Detection.
21h	00	PAD BYTE - Used To Align Following Descriptor on WORD Boundary
22h	0A	Size of Manufacturer ID String Descriptor (10 bytes)
23h	03	Descriptor Type (String Descriptor - 03h)
24h - 2Bh	53 00 4D 00 53 00 43 00	Manufacturer ID String ("SMSC" in UNICODE)
2Ch	12	Size of Product Name String Descriptor (18 bytes)
2Dh	03	Descriptor Type (String Descriptor - 03h)
2Eh - 3Dh	4C 00 41 00 4E 00 39 00 35 00 30 00 30 00 41 00	Product Name String ("LAN9500A" in UNICODE)
3Eh	10	Size of Serial Number String Descriptor (16 bytes)
3Fh	03	Descriptor Type (String Descriptor - 03h)
40h - 4Dh	30 00 30 00 30 00 35 00 31 00 32 00 33 00	Serial Number String ("0005123" in UNICODE)
4Eh	12	Size of Hi-Speed Device Descriptor in Bytes (18 bytes)
4Fh	01	Descriptor Type (Device Descriptor - 01h)
50h - 51h	00 02	USB Specification Number that the device complies with (0200h)
52h	FF	Class Code

Table 5.8 EEPROM Example - 256 Byte EEPROM - LAN9500A/LAN9500Ai (continued)

EEPROM ADDRESS	EEPROM CONTENTS (HEX)	DESCRIPTION
53h	00	Subclass Code
54h	FF	Protocol Code
55h	40	Maximum Packet Size for Endpoint 0
56h - 57h	24 04	Vendor ID (0424h)
58h - 59h	00 9E	Product ID (9E00h)
5Ah - 5Bh	00 01	Device Release Number (0100h)
5Ch	01	Index of Manufacturer String Descriptor
5Dh	02	Index of Product String Descriptor
5Eh	03	Index of Serial Number String Descriptor
5Fh	01	Number of Possible Configurations
60h	09	Size of Hi-Speed Configuration Descriptor in bytes (9 bytes)
61h	02	Descriptor Type (Configuration Descriptor - 02h)
62h - 63h	27 00	Total length in bytes of data returned (0027h = 39 bytes)
64h	01	Number of Interfaces
65h	01	Value to use as an argument to select this configuration
66h	00	Index of String Descriptor describing this configuration
67h	A0	Bus powered and remote wakeup enabled
68h	FA	Maximum Power Consumption is 500 mA
69h	09	Size of Descriptor in Bytes (9 Bytes)
6Ah	04	Descriptor Type (Interface Descriptor - 04h)
6Bh	00	Number identifying this Interface
6Ch	00	Value used to select alternative setting
6Dh	03	Number of Endpoints used for this interface (Less endpoint 0)
6Eh	FF	Class Code
6Fh	00	Subclass Code
70h	FF	Protocol Code
71h	00	Index of String Descriptor Describing this interface
72h	12	Size of Full-Speed Device Descriptor in Bytes (18 Bytes)
73h	01	Descriptor Type (Device Descriptor - 01h)
74h - 75h	00 02	USB Specification Number that the device complies with (0200h)

Table 5.8 EEPROM Example - 256 Byte EEPROM - LAN9500A/LAN9500Ai (continued)

EEPROM ADDRESS	EEPROM CONTENTS (HEX)	DESCRIPTION
76h	FF	Class Code
77h	00	Subclass Code
78h	FF	Protocol Code
79h	40	Maximum Packet Size for Endpoint 0
7Ah - 7Bh	24 04	Vendor ID (0424h)
7Ch - 7Dh	00 9E	Product ID (9E00h)
7Eh - 7Fh	00 01	Device Release Number (0100h)
80h	01	Index of Manufacturer String Descriptor
81h	02	Index of Product String Descriptor
82h	03	Index of Serial Number String Descriptor
83h	01	Number of Possible Configurations
84h	09	Size of Full-Speed Configuration Descriptor in bytes (9 bytes)
85h	02	Descriptor Type (Configuration Descriptor - 02h)
86h - 87h	27 00	Total length in bytes of data returned (0027h = 39 bytes)
88h	01	Number of Interfaces
89h	01	Value to use as an argument to select this configuration
8Ah	00	Index of String Descriptor describing this configuration
8Bh	A0	Bus powered and remote wakeup enabled
8Ch	FA	Maximum Power Consumption is 500 mA
8Dh	09	Size of Full-Speed Interface Descriptor in Bytes (9 Bytes)
8Eh	04	Descriptor Type (Interface Descriptor - 04h)
8Fh	00	Number identifying this Interface
90h	00	Value used to select alternative setting
91h	03	Number of Endpoints used for this interface (Less endpoint 0)
92h	FF	Class Code
93h	00	Subclass Code
94h	FF	Protocol Code
95h	00	Index of String Descriptor Describing this interface
96h - FFh	-	Data storage for use by Host as desired

5.5 Customized Operation Without EEPROM

Customized operation without EEPROM is supported only by LAN9500A/LAN9500Ai.

The device provides the capability to customize operation without the use of an EEPROM. Descriptor information and initialization quantities normally fetched from EEPROM and used to initialize descriptors and elements of the System Control and Status Registers may be specified via an alternate mechanism. This alternate mechanism involves the use of the Descriptor RAM in conjunction with the Attribute Registers and select elements of the System Control and Status Registers. The software device driver orchestrates the process by performing the following actions in the order indicated:

- Initialization of System Control and Status Register Elements in Lieu of EEPROM Load
- Attribute Register Initialization
- Descriptor RAM Initialization
- Enable Descriptor RAM and Flag Attribute Registers as Source
- Inhibit Reset of Select System Control and Status Register Elements

Chapter 6 PME Operation

PME Operation is supported only by LAN9500A/LAN9500Ai.

The device provides a mechanism for waking up a host system via PME mode of operation. PME signaling is only available while the device is operating in the self powered mode. Figure 6.1 illustrates a typical application using LAN9500A/LAN9500Ai.

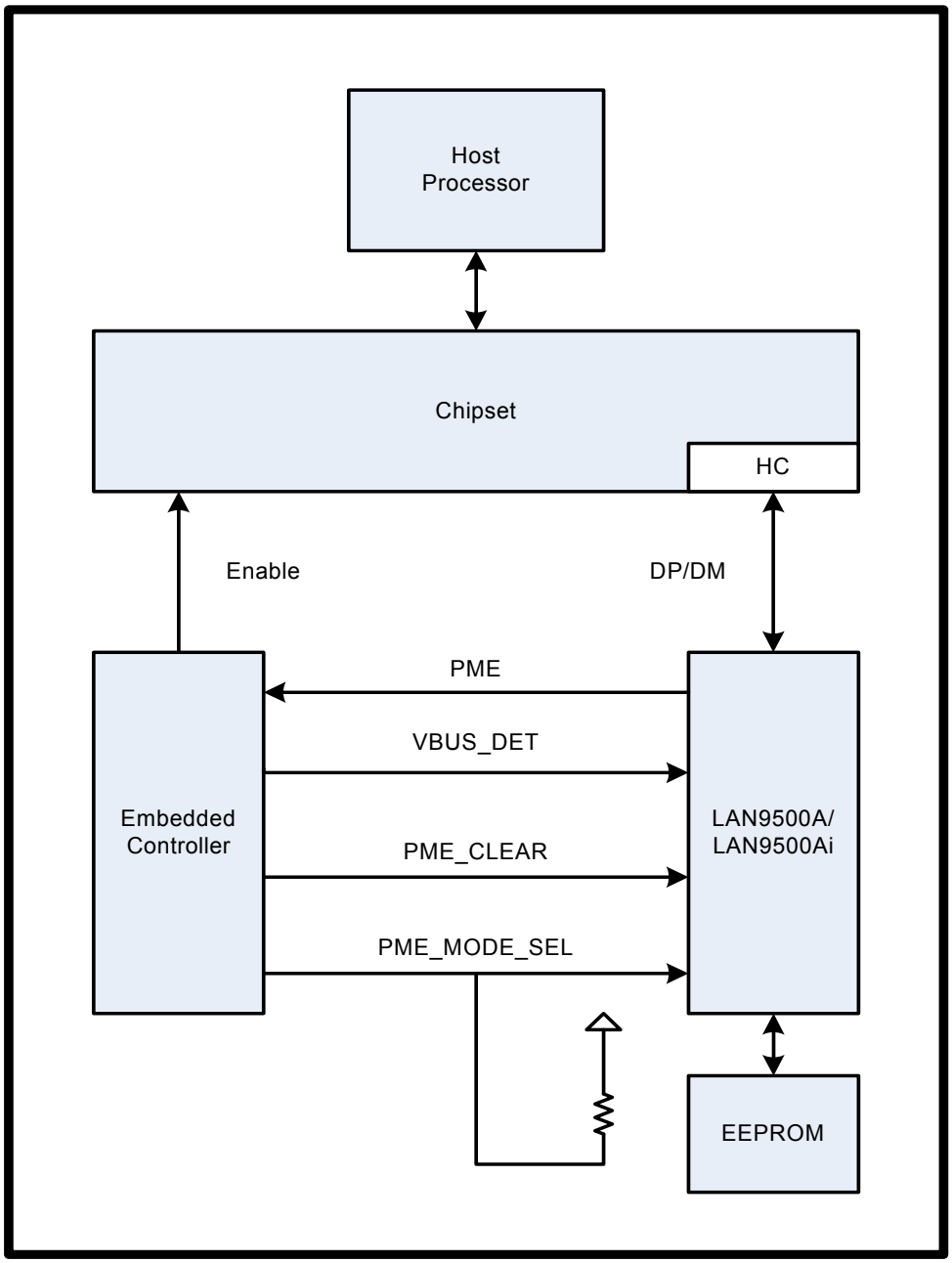


Figure 6.1 Typical Application

The Host Processor is connected to a Chipset containing the Host USB Controller (HC). The USB Host Controller interfaces to the device via the DP/DM USB signals. An Embedded Controller (EC) signals the Chipset and the Host processor to power up via an Enable signal. The EC interfaces to the device via four signals. The PME signal is an input to the EC from the device that indicates the occurrence of a wakeup event. The VBUS_DET output of the EC is used to indicate bus power availability. The PME_CLEAR (nRESET) signal is used to clear the PME. The PME_MODE_SEL signal is sampled by the device when PME_CLEAR (nRESET) is asserted and is used by the device to determine whether it should remain in PME mode or resume normal operation.

GPIO pins are used for PME handling. The pins used depend on the value of the PHY_SEL pin, which determines PHY mode of operation. In Internal PHY mode of operation, GPIO0 is reserved for use as an output to signal the PME. GPIO1 is reserved for use as the PME_MODE_SEL input. GPIO8 and GPIO9 are reserved for analogous use, respectively, in External PHY mode of operation.

The application scenario in Figure 6.1 assumes that the Host Processor and the Chipset are powered off, the EC is operational, and the device is in PME mode, waiting for a wake event to occur. A wake event will result in the device signaling a PME event to the EC, which will then wake up the Host Processor and Chipset via the Enable signal. The EC asserts VBUS_DET after the USB bus is powered, sets PME_MODE_SEL to determine whether the device is to begin normal operation or continue in PME mode, and asserts PME_CLEAR (nRESET) to clear the PME.

The following wake events are supported:

- Wakeup Pin(s)

  The GPIO pins not reserved for PME handling have the capability to wake up the device when operating in PME mode. In order for a GPIO to generate a wake event, it's enable bit must be set in the GPI010:8 Wakeup Enables or GPIO7:0 Wakeup Enables bytes of the EEPROM, as appropriate. During PME mode of operation, the GPIOs used for signaling (GPIOs 0 and 1 or GPIOs 8 and 9) are not affected by the values set in the corresponding bits of GPI010:8 Wakeup Enables or GPIO7:0 Wakeup Enables.

  GPIO10 is available as a wakeup pin in External PHY mode, while GPIOs 2 - 10 are available in Internal PHY Mode. The GPIO10 Detection Select bit in the GPIO PME Flags byte of the EEPROM sets the detection mode for GPIO10 in both External and Internal PHY mode (if set in GPI010:8 Wakeup Enables), while GPIOs 2 - 9 are fixed as active low when operating in Internal PHY mode.

- Magic Packet

  Reception of a Magic Packet when in PME mode will result in a PME being asserted.

- PHY Link Up

  Detection of a PHY link partner when in PME mode will result in a PME being asserted.

In order to facilitate PME mode of operation, the GPIO PME Enable bit in the GPIO PME Flags field, must be set and all remaining GPIO PME Flags field bits must be appropriately configured for pulse or level signaling, buffer type, and GPIO PME WOL selection. The PME event is signaled on GPIO0 (External PHY mode) or GPIO8, depending on the PHY Mode of operation.

The PME_MODE_SEL pin (GPIO1 in Internal Mode of operation, GPIO9 in External Mode of operation) must be driven to the value that determines whether or not the device remains in PME mode of operation (1) or resumes normal operation (0) when the PME is recognized and cleared by the EC via PME_CLEAR (nRESET) assertion.

Note: When in PME mode, nRESET or POR will always cause the contents of the EEPROM to be reloaded.

Note: GPIO10 may be used in PME and External PHY mode to connect to an external PHY's Link LED, in order to generate a PHY Link Up wake event.

Figure 6.2 flowcharts PME operation while in Internal PHY mode. The following conditions hold:

EEPROM Configuration:

- GPIO PME Enable = 1 (enabled)
- GPIO PME Configuration = 0 (PME signaled via level on GPIO pin)
- GPIO PME Length = 0 (NA)
- GPIO PME Polarity = 1 (high level signals event)
- GPIO PME Buffer Type = 1 (Push-Pull)
- GPIO PME WOL Select = 0 (Magic Packet wakeup)
- GPIO10 Detection Select = 0 (Active-low detection)
- Power Method = 1 (self powered)
- MAC address for Magic Packet

PME signaling configuration (as determined by PHY Mode)

- GPIO0 signals PME
- GPIO1 is PME_MODE_SEL

Note: A POR occurring when PME_MODE_SEL = 1 and an EEPROM present with the GPIO PME Enable set results in the device entering PME Mode.

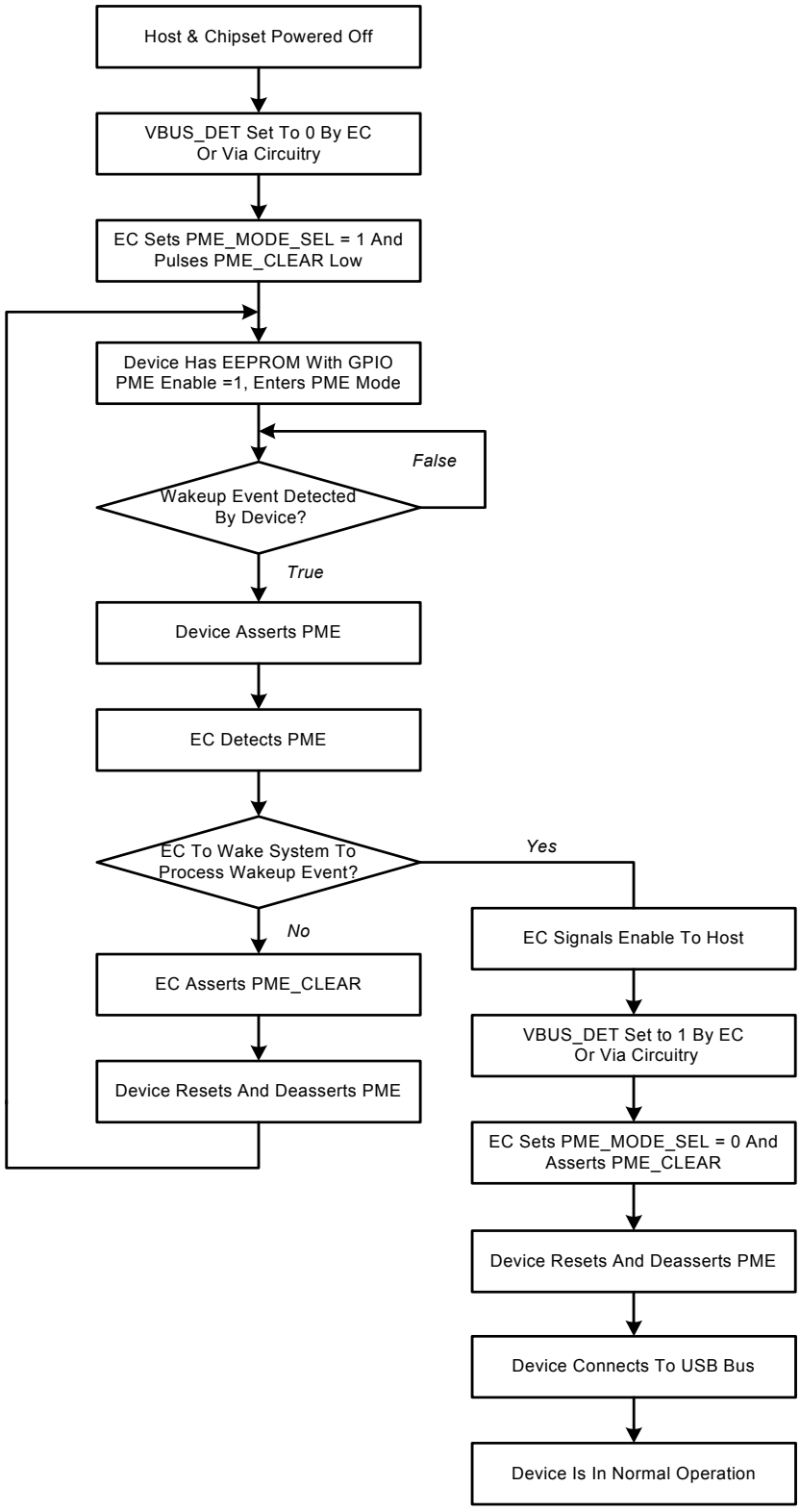


Figure 6.2 PME Operation

Chapter 7 NetDetach Operation

NetDetach operation is supported only by LAN9500A/LAN9500Ai.

NetDetach is a mode of operation where the device detaches from the USB bus after the Ethernet cable is disconnected. This is advantageous for mobile devices, as an attached USB device may prevent the Host CPU from entering the APCI C3 state. Allowing the CPU to enter the C3 state maximizes battery life, as the C3 state is the lowest of the four APCI power states.

When detached, the device is in a low power state. After the Ethernet cable is reconnected, or a programmed GPIO pin asserts, the device automatically attaches to the USB bus. GPIO pin assertion is supported so that this feature can be used with external PHY mode. In this case, the external PHY's link LED would be connected to a GPIO.

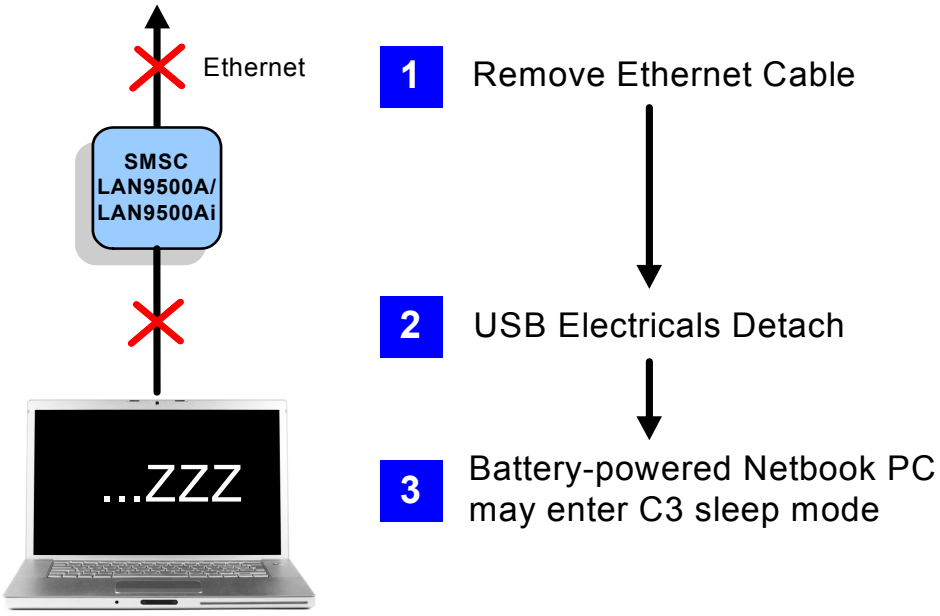


Figure 7.1 Device Detach

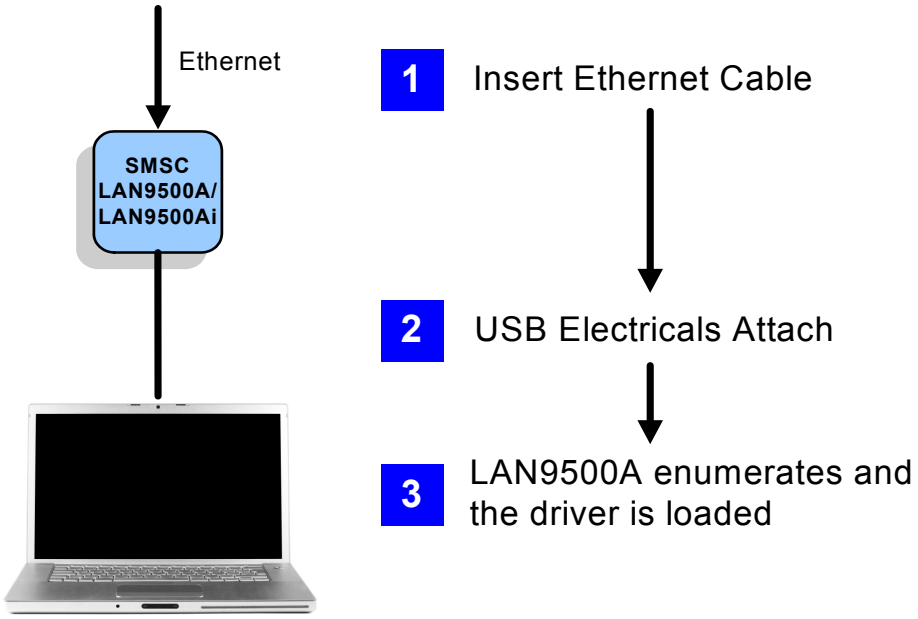


Figure 7.2 Device Attach

Chapter 8 Operational Characteristics

8.1 Absolute Maximum Ratings*

Supply Voltage (VDD33IO, VDD33A) (Note 8.1) . . . . . 0V to +3.6V

Positive voltage on signal pins, with respect to ground (Note 8.2) . . . . . +6V

Negative voltage on signal pins, with respect to ground (Note 8.3) . . . . . -0.5V

Positive voltage on XI, with respect to ground. . . . . +4.6V

Positive voltage on XO, with respect to ground. . . . . +2.5V

Ambient Operating Temperature in Still Air (T_A). . . . . Note 8.4

Storage Temperature. . . . . -55^{o}C to +150^{o}C

Lead Temperature Range . . . . . Refer to JEDEC Spec. J-STD-020

HBM ESD Performance . . . . . Note 8.5

IEC61000-4-2 Contact Discharge ESD Performance (Note 8.6) . . . . . +/-8kV

IEC61000-4-2 Air-Gap Discharge ESD Performance (Note 8.6) . . . . . +/-15kV

Note 8.1 When powering this device from laboratory or system power supplies, it is important that the absolute maximum ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

Note 8.2 This rating does not apply to the following pins: XI, XO, EXRES, USBRBIAS.

Note 8.3 This rating does not apply to the following pins: EXRES, USBRBIAS.

Note 8.4 0^{o}C to +70^{o}C for commercial version, -40^{o}C to +85^{o}C for industrial version.

Note 8.5 +/-8kV for LAN9500/LAN9500i, +/-5kV for LAN9500A/LAN9500Ai

Note 8.6 Performed by independent 3rd party test facility.

*Stresses exceeding those listed in this section could cause permanent damage to the device. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at any condition exceeding those indicated in Section 8.2, "Operating Conditions**", Section 8.4, "DC Specifications", or any other applicable section of this specification is not implied. Note, device signals are *NOT* 5 volt tolerant unless specified otherwise.

8.2 Operating Conditions**

Supply Voltage (VDD33A, VDD33BIAS, VDD33IO). . . . . +3.3V +/- 300mV

Ambient Operating Temperature in Still Air (T_A). . . . . Note 8.4

**Proper operation of the device is guaranteed only within the ranges specified in this section.

8.3 Power Consumption

This section details the power consumption of the device as measured during various modes of operation. Power consumption values are provided for both the device-only, and for the device plus Ethernet components. Power dissipation is determined by temperature, supply voltage, and external source/sink requirements.

Note: All current consumption and power dissipation values were measured at VDD33IO and VDD33A equal to 3.3V.

8.3.1 SUSPEND0

Table 8.1 Power Consumption/Dissipation - SUSPEND0 (LAN9500/LAN9500i)

PARAMETER	MIN	TYPICAL	MAX	UNIT
Supply current (VDD33IO, VDD33A) (Device Only)		78		mA
Power Dissipation (Device Only)		257		mW
Power Dissipation (Device and Ethernet components)		395		mW

Table 8.2 Power Consumption/Dissipation - SUSPEND0 (LAN9500A/LAN9500Ai)

PARAMETER	MIN	TYPICAL	MAX	UNIT
Supply current (VDD33IO, VDD33A) (Device Only)		46		mA
Power Dissipation (Device Only)		152		mW
Power Dissipation (Device and Ethernet components)		291		mW

8.3.2 SUSPEND1

Table 8.3 Power Consumption/Dissipation - SUSPEND1 (LAN9500/LAN9500i)

PARAMETER	MIN	TYPICAL	MAX	UNIT
Supply current (VDD33IO, VDD33A) (Device Only)		20		mA
Power Dissipation (Device Only)		66		mW
Power Dissipation (Device and Ethernet components)		66		mW

Table 8.4 Power Consumption/Dissipation - SUSPEND1 (LAN9500A/LAN9500Ai)

PARAMETER	MIN	TYPICAL	MAX	UNIT
Supply current (VDD33IO, VDD33A) (Device Only)		7.0		mA
Power Dissipation (Device Only)		23.5		mW
Power Dissipation (Device and Ethernet components)		27.5		mW

8.3.3 SUSPEND2

Table 8.5 Power Consumption/Dissipation - SUSPEND2 (LAN9500/LAN9500i)

PARAMETER	MIN	TYPICAL	MAX	UNIT
Supply current (VDD33IO, VDD33A) (Device Only)		0.624		mA
Power Dissipation (Device Only)		2.1		mW
Power Dissipation (Device and Ethernet components)		2.1		mW

Table 8.6 Power Consumption/Dissipation - SUSPEND2 (LAN9500A/LAN9500Ai)

PARAMETER	MIN	TYPICAL	MAX	UNIT
Supply current (VDD33IO, VDD33A) (Device Only)		1.6		mA
Power Dissipation (Device Only)		5.3		mW
Power Dissipation (Device and Ethernet components)		5.3		mW

Note: SUSPEND2 power consumption/dissipation values were measured in bus-powered mode.

8.3.4 SUSPEND3

Note: SUSPEND3 not supported by LAN9500/LAN9500i.

Table 8.7 Power Consumption/Dissipation - SUSPEND3 (LAN9500A/LAN9500Ai)

PARAMETER	MIN	TYPICAL	MAX	UNIT
Supply current (VDD33IO, VDD33A) (Device Only)		24.5		mA
Power Dissipation (Device Only)		81.2		mW
Power Dissipation (Device and Ethernet components)		85.1		mW

8.3.5 Operational

Table 8.8 Operational Power Consumption/Dissipation (LAN9500/LAN9500i)

PARAMETER	MIN	TYPICAL	MAX	UNIT
100BASE-TX Full Duplex (USB High-Speed)				
Supply current (VDD33IO, VDD33A) (Device Only)		143		mA
Power Dissipation (Device Only)		474		mW
Power Dissipation (Device and Ethernet components)		618		mW
10BASE-T Full Duplex (USB High-Speed)				
Supply current (VDD33IO, VDD33A) (Device Only)		103		mA
Power Dissipation (Device Only)		342		mW
Power Dissipation (Device and Ethernet components)		692		mW
100BASE-TX Full Duplex (USB Full-Speed)				
Supply current (VDD33IO, VDD33A) (Device Only)		139		mA
Power Dissipation (Device Only)		460		mW
Power Dissipation (Device and Ethernet components)		605		mW
10BASE-T Full Duplex (USB Full-Speed)				
Supply current (VDD33IO, VDD33A) (Device Only)		98		mA
Power Dissipation (Device Only)		324		mW
Power Dissipation (Device and Ethernet components)		673		mW

Table 8.9 Operational Power Consumption/Dissipation (LAN9500A/LAN9500Ai)

PARAMETER	MIN	TYPICAL	MAX	UNIT
100BASE-TX Full Duplex (USB High-Speed)				
Supply current (VDD33IO, VDD33A) (Device Only)		69		mA
Power Dissipation (Device Only)		228		mW
Power Dissipation (Device and Ethernet components)		367		mW
10BASE-T Full Duplex (USB High-Speed)				
Supply current (VDD33IO, VDD33A) (Device Only)		45		mA
Power Dissipation (Device Only)		149		mW
Power Dissipation (Device and Ethernet components)		489		mW
100BASE-TX Full Duplex (USB Full-Speed)				
Supply current (VDD33IO, VDD33A) (Device Only)		66		mA
Power Dissipation (Device Only)		218		mW
Power Dissipation (Device and Ethernet components)		356		mW
10BASE-T Full Duplex (USB Full-Speed)				
Supply current (VDD33IO, VDD33A) (Device Only)		43		mA
Power Dissipation (Device Only)		142		mW
Power Dissipation (Device and Ethernet components)		483		mW

8.3.6 Customer Evaluation Board Operational Current Consumption***

Table 8.10 CEB Operational Current Consumption (LAN9500/LAN9500i)

PARAMETER	MIN	TYPICAL	MAX	UNIT
100BASE-TX Full Duplex (USB High-Speed)				
Total SMSC Customer Evaluation Board Current Consumption			208	mA

Table 8.11 CEB Operational Current Consumption (LAN9500A/LAN9500Ai)

PARAMETER	MIN	TYPICAL	MAX	UNIT
100BASE-TX Full Duplex (USB High-Speed)				
Total SMSC Customer Evaluation Board Current Consumption			150	mA

***Total system current consumption as measured on the 5V USB VBUS input to a bus-powered Customer Evaluation Board, where VBUS = 5.0V and VDD33IO = VDD33A = 3.3V.

8.4 DC Specifications

Table 8.12 I/O Buffer Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
IS Type Input Buffer						
Low Input Level	V_{ILI}	-0.3			V	
High Input Level	V_{IHI}			3.6	V	
Negative-Going Threshold	V_{ILT}	1.01	1.19	1.39	V	Schmitt trigger
Positive-Going Threshold	V_{IHT}	1.39	1.59	1.8	V	Schmitt trigger
SchmittTrigger Hysteresis (V_{IHT} - V_{ILT})	V_{HYS}	336	399	485	mV	
Input Leakage (V_{IN} = VSS or VDD33IO)	I_{IH}	-10		10	uA	Note 8.7
Input Capacitance	C_{IN}			3	pF	
IS_5V Type Input Buffer						
Low Input Level	V_{ILI}	-0.3			V	
High Input Level	V_{IHI}			5.5	V	
Negative-Going Threshold	V_{ILT}	1.01	1.19	1.39	V	Schmitt trigger
Positive-Going Threshold	V_{IHT}	1.39	1.59	1.8	V	Schmitt trigger
SchmittTrigger Hysteresis (V_{IHT} - V_{ILT})	V_{HYS}	336	399	485	mV	
Input Leakage (V_{IN} = VSS or VDD33IO)	I_{IH}	-10		10	uA	Note 8.7
Input Leakage (V_{IN} = 5.5V)	I_{IH}			79	uA	Note 8.7, Note 8.8
Input Capacitance	C_{IN}			4	pF	
O8 Type Buffers						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8mA
High Output Level	V_{OH}	VDD33IO - 0.4			V	I_{OH} = -8mA
OD8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8mA
O12 Type Buffers						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
High Output Level	V_{OH}	VDD33IO - 0.4			V	I_{OH} = -12mA
OD12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
ICLK Type Buffer (XI Input)						Note 8.9
Low Input Level	V_{ILI}	-0.3		0.5	V	
High Input Level	V_{IHI}	1.4		3.6	V	

Note 8.7 This specification applies to all inputs and tri-stated bi-directional pins. Internal pull-down and pull-up resistors add +/- 50uA per-pin (typical).

Note 8.8 This is the total 5.5V input leakage for the entire device.

Note 8.9 XI can optionally be driven from a 25MHz single-ended clock oscillator.

Table 8.13 100BASE-TX Transceiver Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Peak Differential Output Voltage High	V_{PPH}	950	-	1050	mVpk	Note 8.10
Peak Differential Output Voltage Low	V_{PPL}	-950	-	-1050	mVpk	Note 8.10
Signal Amplitude Symmetry	V_{SS}	98	-	102	%	Note 8.10
Signal Rise and Fall Time	T_{RF}	3.0	-	5.0	nS	Note 8.10
Rise and Fall Symmetry	T_{RFS}	-	-	0.5	nS	Note 8.10
Duty Cycle Distortion	D_{CD}	35	50	65	%	Note 8.11
Overshoot and Undershoot	V_{OS}	-	-	5	%	
Jitter				1.4	nS	Note 8.12

Note 8.10 Measured at line side of transformer, line replaced by 100Ω (+/- 1%) resistor.

Note 8.11 Offset from 16nS pulse width at 50% of pulse peak.

Note 8.12 Measured differentially.

Table 8.14 10BASE-T Transceiver Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Transmitter Peak Differential Output Voltage	V_{OUT}	2.2	2.5	2.8	V	Note 8.13
Receiver Differential Squelch Threshold	V_{DS}	300	420	585	mV	

Note 8.13 Min/max voltages guaranteed as measured with 100Ω resistive load.

8.5 AC Specifications

This section details the various AC timing specifications of the device.

Note: The MII timing adheres to the IEEE 802.3 specification. Refer to the IEEE 802.3 specification for additional MII timing information.

Note: The USBDP and USBDM pin timing adheres to the USB 2.0 specification. Refer to the Universal Serial Bus Revision 2.0 specification for detailed USB timing information.

8.5.1 Equivalent Test Load

Output timing specifications assume the 25pF equivalent test load illustrated in Figure 8.1 below, unless otherwise specified.

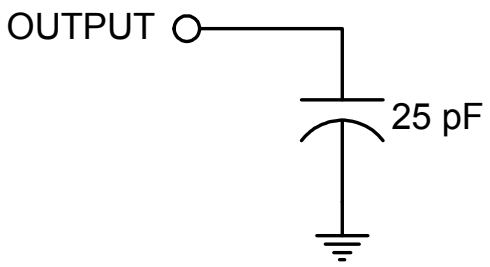


Figure 8.1 Output Equivalent Test Load

8.5.2 Power-On Configuration Strap Valid Timing

Figure 8.2 illustrates the configuration strap valid timing requirement in relation to power-on. In order for valid configuration strap values to be read at power-on, the following timing requirements must be met.

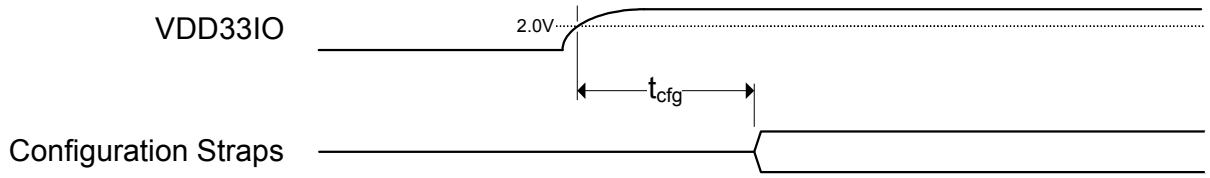


Figure 8.2 Power-On Configuration Strap Valid Timing

Table 8.15 Power-On Configuration Strap Valid Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{cfg}	Configuration strap valid time			15	mS

8.5.3 Reset and Configuration Strap Timing

Figure 8.3 illustrates the nRESET pin timing requirements and its relation to the configuration strap pins and output drive. Assertion of nRESET is not a requirement. However, if used, it must be asserted for the minimum period specified.

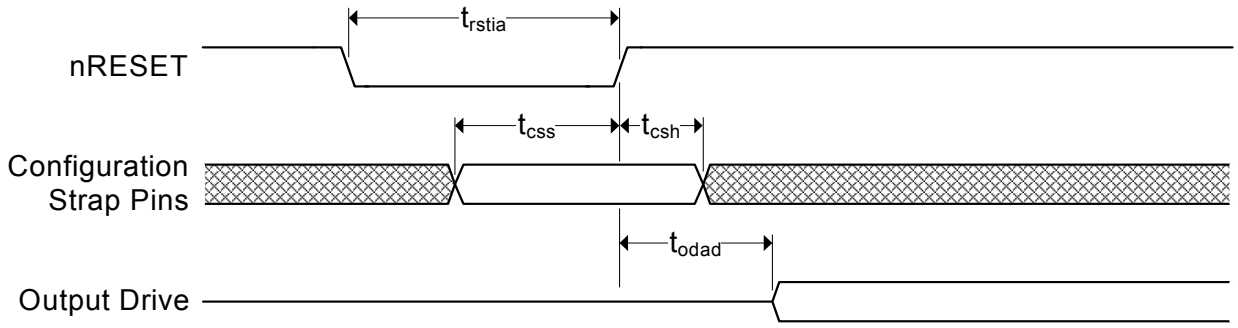


Figure 8.3 nRESET Reset Pin Timing

Table 8.16 nRESET Reset Pin Timing Values

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{rstia}	nRESET input assertion time	1			uS
t_{css}	Configuration strap pins setup to nRESET deassertion	200			nS
t_{csh}	Configuration strap pins hold after nRESET deassertion	10			nS
t_{odad}	Output drive after deassertion	30			nS

8.5.4 EEPROM Timing

The following specifies the EEPROM timing requirements for the device:

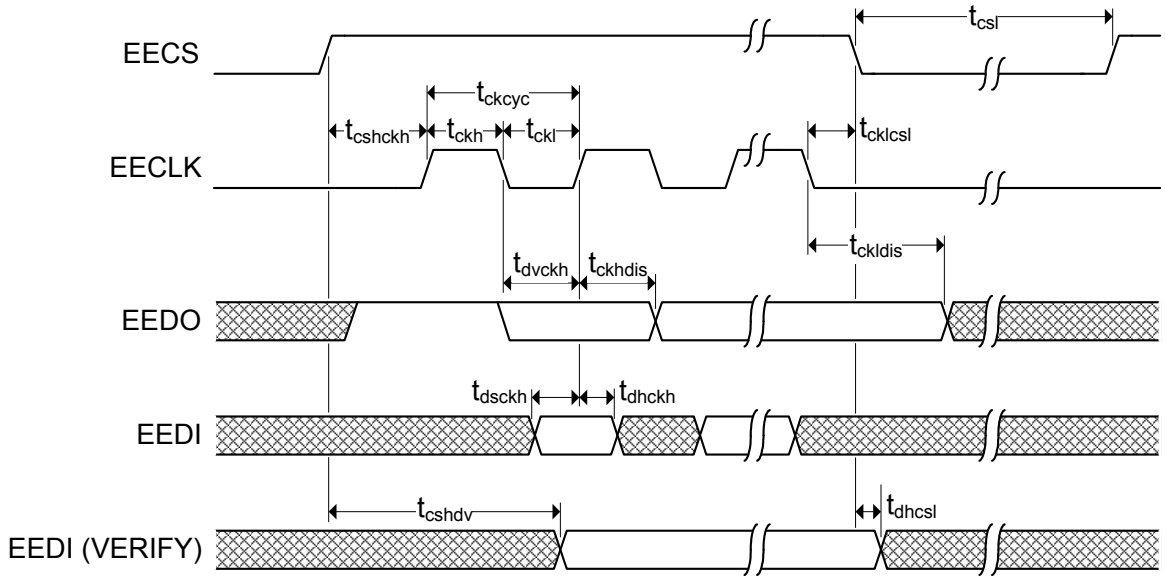


Figure 8.4 EEPROM Timing

Table 8.17 EEPROM Timing Values

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{ckcyc}	EECLK Cycle time	1110		1130	ns
t_{ckh}	EECLK High time	550		570	ns
t_{ckl}	EECLK Low time	550		570	ns
t_{cshckh}	EECS high before rising edge of EECLK	1070			ns
t_{cklcsl}	EECLK falling edge to EECS low	30			ns
t_{dvckh}	EEDO valid before rising edge of EECLK	550			ns
t_{ckhdis}	EEDO disable after rising edge EECLK	550			ns
t_{dsckh}	EEDI setup to rising edge of EECLK	90			ns
t_{dhckh}	EEDI hold after rising edge of EECLK	0			ns
t_{ckldis}	EECLK low to data disable (OUTPUT)	580			ns
t_{cshdv}	EEDIO valid after EECS high (VERIFY)			600	ns
t_{dhcsl}	EEDIO hold after EECS low (VERIFY)	0			ns
t_{csl}	EECS low	1070			ns

8.5.5 MII Interface Timing

This section specifies the MII interface transmit and receive timing.

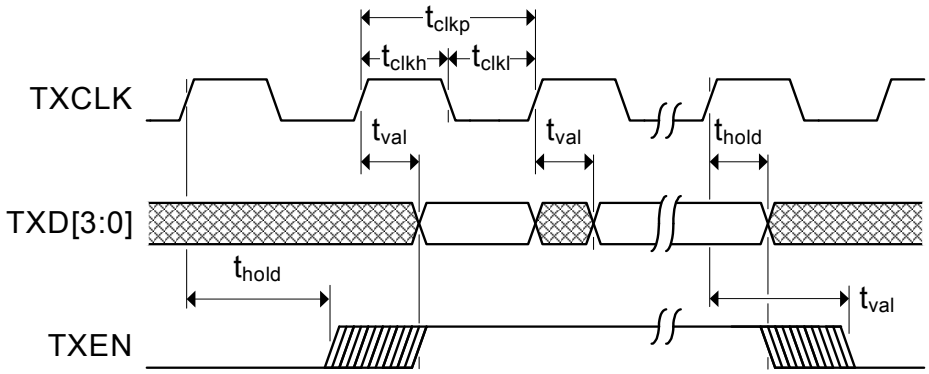


Figure 8.5 MII Transmit Timing

Table 8.18 MII Transmit Timing Values

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTES
t_{clkp}	TXCLK period	40		ns	
t_{clkh}	TXCLK high time	t_{clkp}*0.4	t_{clkp}*0.6	ns	
t_{clkl}	TXCLK low time	t_{clkp}*0.4	t_{clkp}*0.6	ns	
t_{val}	TXD[3:0], TXEN output valid from rising edge of TXCLK		22.0	ns	Note 8.14
t_{hold}	TXD[3:0], TXEN output hold from rising edge of TXCLK	0		ns	Note 8.14

Note 8.14 Timing was designed for system load between 10 pf and 25 pf.

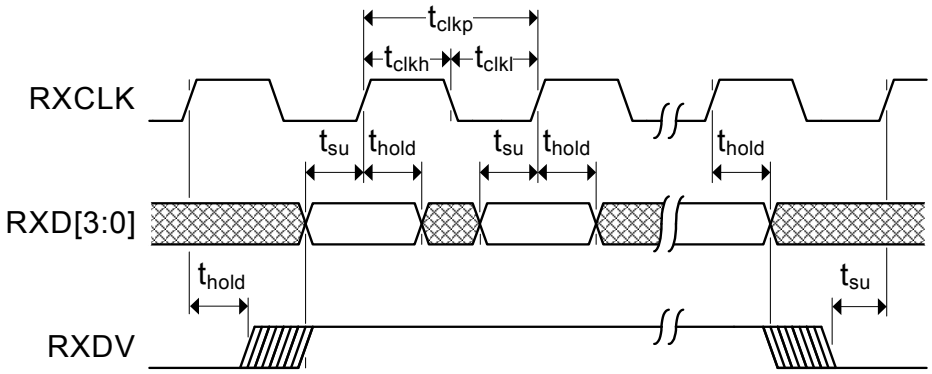


Figure 8.6 MII Receive Timing

Table 8.19 MII Receive Timing Values

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTES
t_{clkp}	RXCLK period	40		ns	
t_{clkh}	RXCLK high time	t_{clkp}*0.4	t_{clkp}*0.6	ns	
t_{clkl}	RXCLK low time	t_{clkp}*0.4	t_{clkp}*0.6	ns	
t_{su}	RXD[3:0], RXDV setup time to rising edge of RXCLK	8.0		ns	Note 8.15
t_{hold}	RXD[3:0], RXDV hold time after rising edge of RXCLK	9.0		ns	Note 8.15

Note 8.15 Timing was designed for system load between 10 pf and 25 pf.

8.5.6 Turbo MII Interface Timing

This section specifies the Turbo MII interface transmit and receive timing.

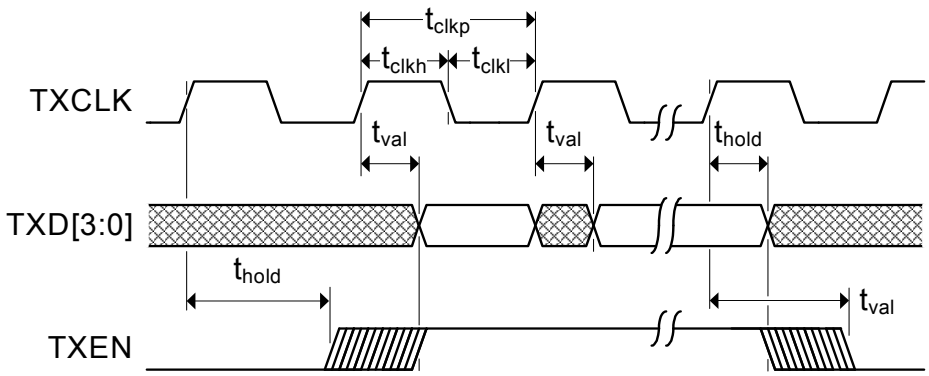


Figure 8.7 Turbo MII Transmit Timing

Table 8.20 Turbo MII Transmit Timing Values

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTES
t_{clkp}	TXCLK period	20		ns	
t_{clkh}	TXCLK high time	t_{clkp}*0.4	t_{clkp}*0.6	ns	
t_{clkl}	TXCLK low time	t_{clkp}*0.4	t_{clkp}*0.6	ns	
t_{val}	TXD[3:0], TXEN output valid from rising edge of TXCLK		12.5	ns	Note 8.16
t_{hold}	TXD[3:0], TXEN output hold from rising edge of TXCLK	1.5		ns	Note 8.16

Note 8.16 Timing was designed for system load between 10 pf and 15 pf.

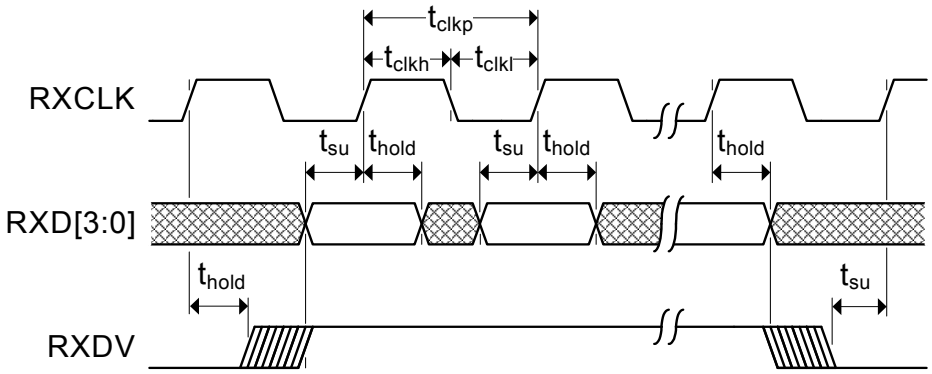


Figure 8.8 Turbo MII Receive Timing

Table 8.21 Turbo MII Receive Timing Values

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTES
t_{clkp}	RXCLK period	20		ns	
t_{clkh}	RXCLK high time	t_{clkp}*0.4	t_{clkp}*0.6	ns	
t_{clkl}	RXCLK low time	t_{clkp}*0.4	t_{clkp}*0.6	ns	
t_{su}	RXD[3:0], RXDV setup time to rising edge of RXCLK	5.5		ns	Note 8.17
t_{hold}	RXD[3:0], RXDV hold time after rising edge of RXCLK	0		ns	Note 8.17

Note 8.17 Timing was designed for system load between 10 pf and 15 pf.

8.5.7 JTAG Timing

This section specifies the JTAG timing of the device.

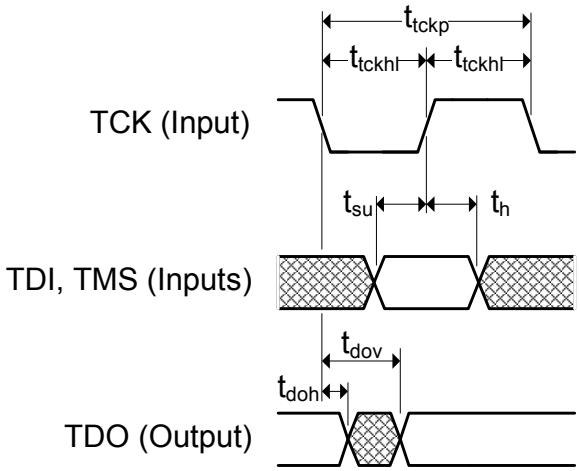


Figure 8.9 JTAG Timing

Table 8.22 JTAG Timing Values

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTES
t_{tckp}	TCK clock period	66.67		ns	
t_{tckhl}	TCK clock high/low time	t_{tckp}*0.4	t_{tckp}*0.6	ns	
t_{su}	TDI, TMS setup to TCK rising edge	10		ns	
t_h	TDI, TMS hold from TCK rising edge	10		ns	
t_{dov}	TDO output valid from TCK falling edge		16	ns	
$t_{doinvld}$	TDO output invalid from TCK falling edge	0		ns	

8.6 Clock Circuit

The device can accept either a 25MHz crystal (preferred) or a 25MHz single-ended clock oscillator (+/-50ppm) input. If the single-ended clock oscillator method is implemented, XO should be left unconnected and XI should be driven with a nominal 0-3.3V clock signal. The input clock duty cycle is 40% minimum, 50% typical and 60% maximum.

It is recommended that a crystal utilizing matching parallel load capacitors be used for the crystal input/output signals (XI/XO). See Table 8.23 for the recommended crystal specifications.

Table 8.23 Crystal Specifications

PARAMETER	SYMBOL	MIN	NOM	MAX	UNITS	NOTES
Crystal Cut	AT, typ					
Crystal Oscillation Mode	Fundamental Mode					
Crystal Calibration Mode	Parallel Resonant Mode					
Frequency	F_{fund}	-	25.000	-	MHz	
Frequency Tolerance @ 25°C	F_{tol}	-	-	+/-50	PPM	Note 8.18
Frequency Stability Over Temp	F_{temp}	-	-	+/-50	PPM	Note 8.18
Frequency Deviation Over Time	F_{age}	-	+/-3 to 5	-	PPM	Note 8.19
Total Allowable PPM Budget		-	-	+/-50	PPM	Note 8.20
Shunt Capacitance	C_O	-	7 typ	-	pF	
Load Capacitance	C_L	-	20 typ	-	pF	
Drive Level	P_W	300	-	-	uW	
Equivalent Series Resistance	R_1	-	-	50	Ohm	
Operating Temperature Range		Note 8.21	-	Note 8.22	°C	
XI Pin Capacitance		-	3 typ	-	pF	Note 8.23
XO Pin Capacitance		-	3 typ	-	pF	Note 8.23

Note 8.18 The maximum allowable values for Frequency Tolerance and Frequency Stability are application dependant. Since any particular application must meet the IEEE +/-50 PPM Total PPM Budget, the combination of these two values must be approximately +/-45 PPM (allowing for aging).

Note 8.19 Frequency Deviation Over Time is also referred to as Aging.

Note 8.20 The total deviation for the Transmitter Clock Frequency is specified by IEEE 802.3u as +/- 50 PPM.

Note 8.21 0°C for commercial version, -40°C for industrial version.

Note 8.22 +70°C for commercial version, +85°C for industrial version.

Note 8.23 This number includes the pad, the bond wire and the lead frame. PCB capacitance is not included in this value. The XO/XI pin and PCB capacitance values are required to accurately calculate the value of the two external load capacitors. These two external load capacitors determine the accuracy of the 25.000 MHz frequency.

Chapter 9 Package Outline

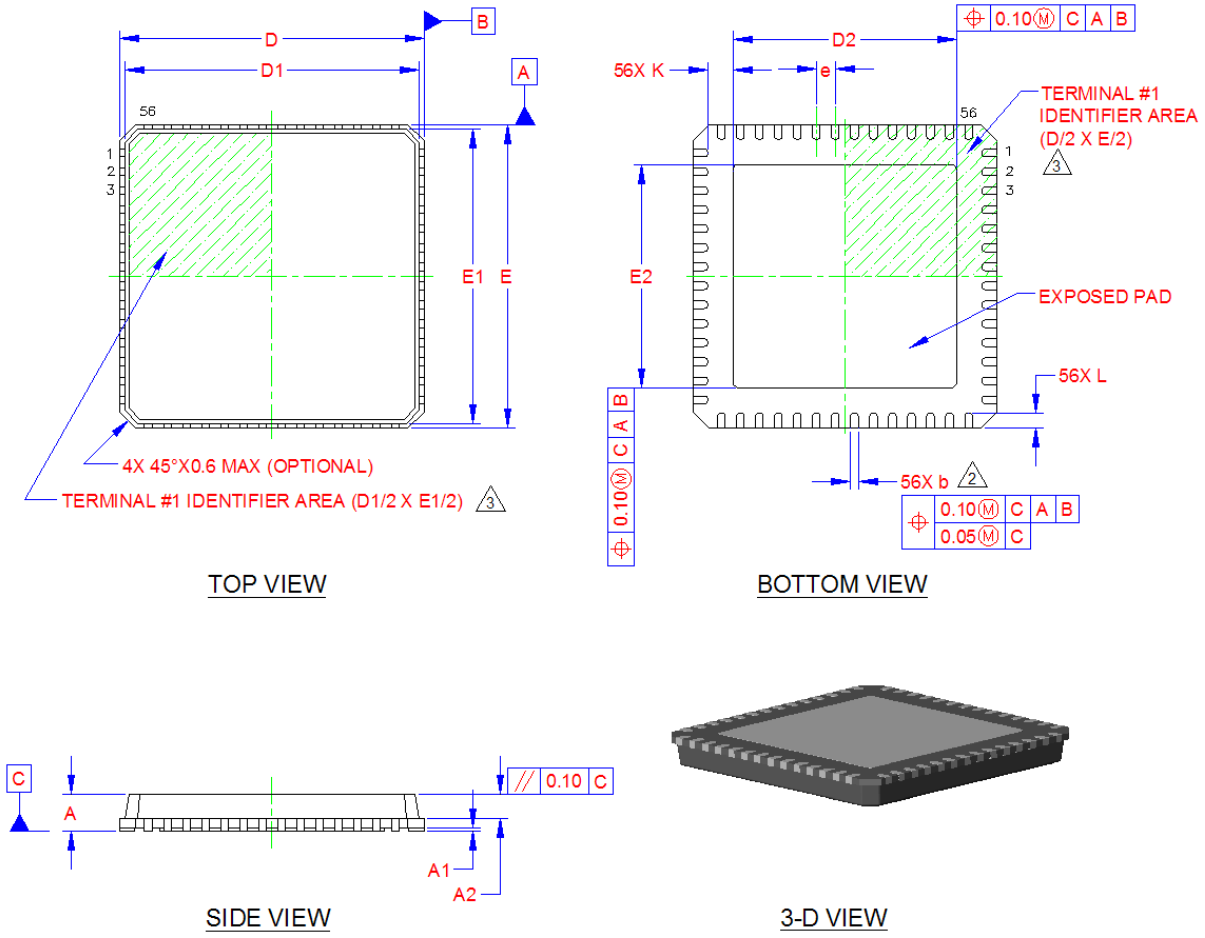


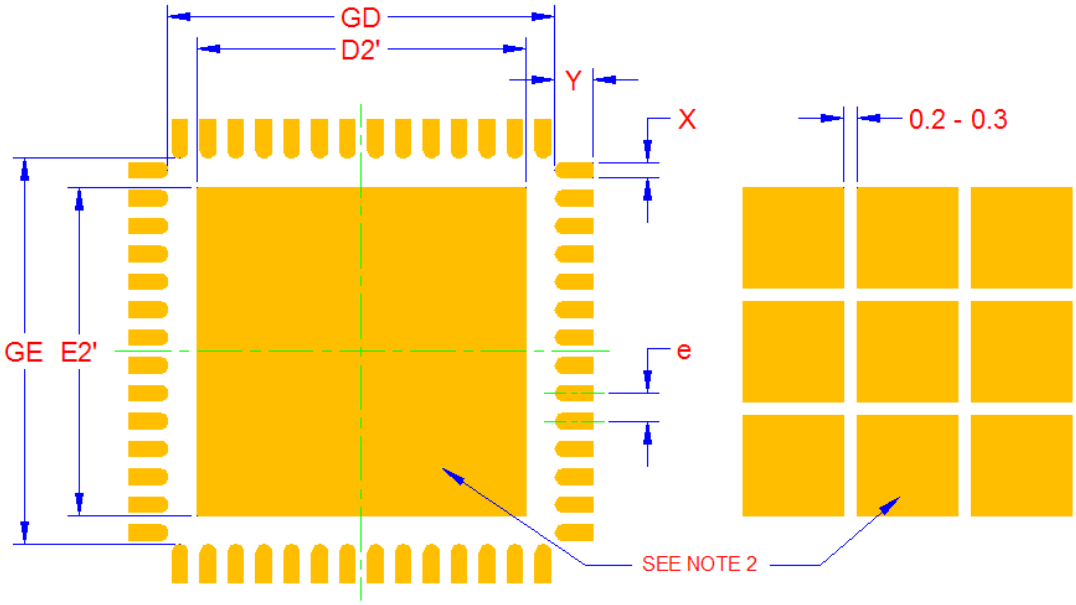
Figure 9.1 LAN950x 56-QFN Package

Table 9.1 LAN950x 56-QFN Dimensions

	MIN	NOMINAL	MAX	REMARKS
A	0.70	0.85	1.00	Overall Package Height
A1	0.00	0.02	0.05	Standoff
A2	-	-	0.90	Mold Cap Thickness
D/E	7.85	8.00	8.15	X/Y Body Size
D1/E1	7.55	7.75	7.95	X/Y Mold Cap Size
D2/E2	5.80	5.90	6.00	X/Y Exposed Pad Size
L	0.30	0.40	0.50	Terminal Length
b	0.18	0.25	0.30	Terminal Width
K	0.55	-	-	Center Pad to Pin Clearance
e	0.50 BSC			Terminal Pitch

Notes:

1. All dimensions are in millimeters unless otherwise noted.
2. Position tolerance of each terminal and exposed pad is +/- 0.05 mm at maximum material condition. Dimension “b” applies to plated terminals and is measured between 0.15 and 0.30 mm from the terminal tip.
3. The pin 1 identifier may vary, but is always located within the zone indicated.



LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
GD/GE	6.93	-	7.05
D2'/E2'	-	5.90	5.90
X	-	0.28	0.28
Y	-	0.69	0.69
e		0.50	

NOTES:
1. THE USER MAY MODIFY THE PCB LAND PATTERN DESIGN AND DIMENSIONS BASED ON THEIR EXPERIENCE AND/OR PROCESS CAPABILITY
2. EXPOSED SOLDERABLE COPPER AREA OF THE CENTER PAD CAN BE EITHER SOLID OR SEGMENTED
3. MAXIMUM THERMAL AND ELECTRICAL PACKAGE PERFORMANCE IS ACHIEVED WHEN AN ARRAY OF SOLID VIAS IS INCORPORATED IN THE CENTER LAND PATTERN

PCB LAND PATTERN

Figure 9.2 LAN950x 56-QFN Recommended PCB Land Pattern

Chapter 10 Datasheet Revision History

Table 10.1 Customer Revision History

REVISION LEVEL AND DATE	SECTION/FIGURE/ENTRY	CORRECTION
Rev. 1.1 (04-18-13)	Microchip logo added to cover, legal disclaimer modified. Added to ordering information: “Please contact your SMSC sales representative for additional documentation related to this product such as application notes, anomaly sheets, and design guidelines.”	
Rev. 1.1 (07-15-11)	Ordering Information	Added tape and reel options.
Rev. 1.1 (07-12-11)	Figure 4.1 Power Connections on page 25	Substitued “u” and “ohm” for Greek symbols mu and omega that were not properly displayed because of font issues.
	Section 8.5.7, "JTAG Timing," on page 62	Added this section.
Rev. 1.0 (05-17-10)	Initial Release	