

# DATA SHEET

**80C562/83C562**

Single-chip 8-bit microcontroller

Product specification

1992 Jan 08

IC20 Data Handbook

# Single-chip 8-bit microcontroller

# 80C562/83C562

Single-chip 8-bit microcontroller with 8-bit A/D, capture/compare timer, high-speed outputs, PWM

## DESCRIPTION

The 80C562/83C562 (hereafter generically referred to as 8XC562) Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 83C562/83C562 has the same instruction set as the 80C51.

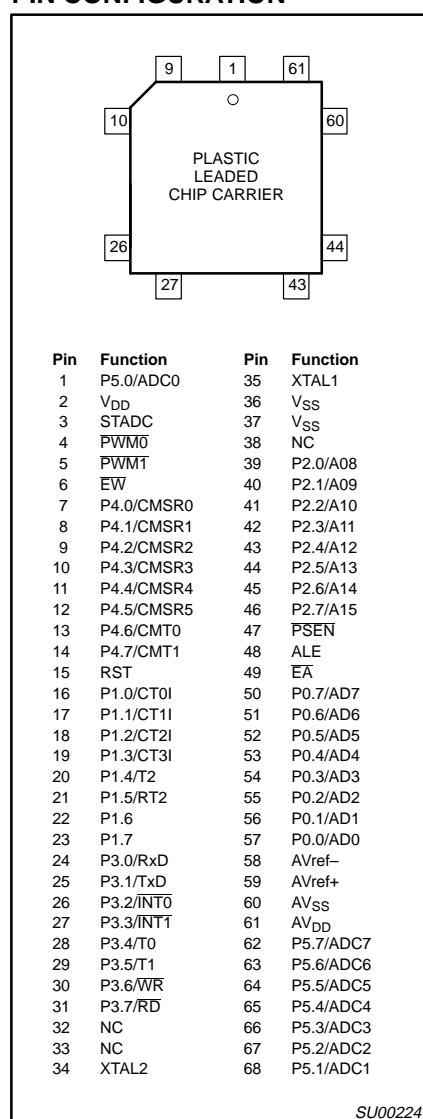
The 8XC562 contains a non-volatile  $256 \times 8$  read-only program memory, a volatile  $256 \times 8$  read/write data memory (83C562) (the 80C562 is ROMless), a volatile  $256 \times 8$  read/write data memory, six 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), an additional 16-bit timer coupled to capture and compare latches, a 15-source, two-priority-level, nested interrupt structure, an 8-input ADC, two pulse width modulated outputs, standard 80C51 UART, a "watchdog" timer and on-chip oscillator and timing circuits. For systems that require extra capability, the 83C562 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 12MHz crystal, 58% of the instructions are executed in  $1\mu\text{s}$  and 40% in  $2\mu\text{s}$ . Multiply and divide instructions require  $4\mu\text{s}$ .

## FEATURES

- 80C51 instruction set
- $8k \times 8$  ROM expandable externally to 64k bytes
- $256 \times 8$  RAM, expandable externally to 64k bytes
- Two standard 16-bit timer/counters
- An additional 16-bit timer/counter coupled to four capture registers and three compare registers
- Capable of producing eight synchronized, timed outputs
- An 8-bit ADC with eight multiplexed analog inputs
- Two 8-bit resolution, pulse width modulated outputs
- Five 8-bit I/O ports plus one 8-bit input port shared with analog inputs
- Full-duplex UART compatible with the standard 80C51
- On-chip watchdog timer
- Three temperature ranges
  - 0 to  $+70^\circ\text{C}$
  - $-40$  to  $+85^\circ\text{C}$
  - $-40$  to  $+125^\circ\text{C}$

## PIN CONFIGURATION



SU00224

## Single-chip 8-bit microcontroller

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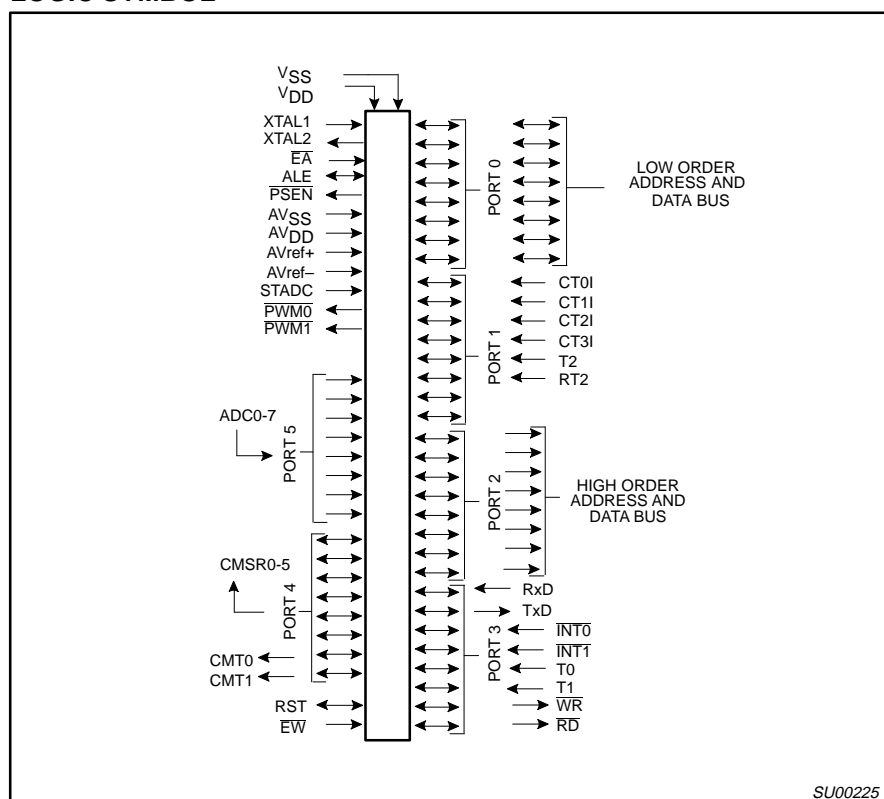
## ORDERING INFORMATION

PHILIPS PART ORDER NUMBER PART MARKING		PHILIPS NORTH AMERICA PART ORDER NUMBER		Drawing Number	EPROM	Drawing Number	TEMPERATURE RANGE °C AND PACKAGE	FREQ MHz
ROMless	ROM	ROMless	ROM					
PCB80C562-16WP	PCB83C562-16WP/xxx	S80C562-4A68	S83C562-4A68	SOT188	S87C552-4A68 <sup>2</sup>	SOT188-3	0 to +70, Plastic Leaded Chip Carrier	16
					S87C552-4K68 <sup>2</sup>	1473A	0 to +70, Plastic Leaded Chip Carrier w/Window	16
PCF80C562-12WP	PCF83C562-12WP/xxx	S80C562-2A68	S83C562-2A68	SOT188	S87C552-5A68 <sup>2</sup>	SOT188-3	−40 to +85, Plastic Leaded Chip Carrier	12
					S87C552-5K68 <sup>2</sup>	1473A	−40 to +85, Plastic Leaded Chip Carrier w/Window	12
PCA80C562-12WP	PCA83C562-12WP/xxx	S80C562-6A68	S83C562-6A68	SOT188			−40 to +125, Plastic Leaded Chip Carrier	12

## NOTES:

- 80C562 and 83C562 frequency range is 1.2MHz–12MHz or 1.2MHz–16MHz.
- 87C552 frequency range is 3.5MHz–16MHz. For full specification, see the 87C552 data sheets.
- xxx denotes the ROM code number.

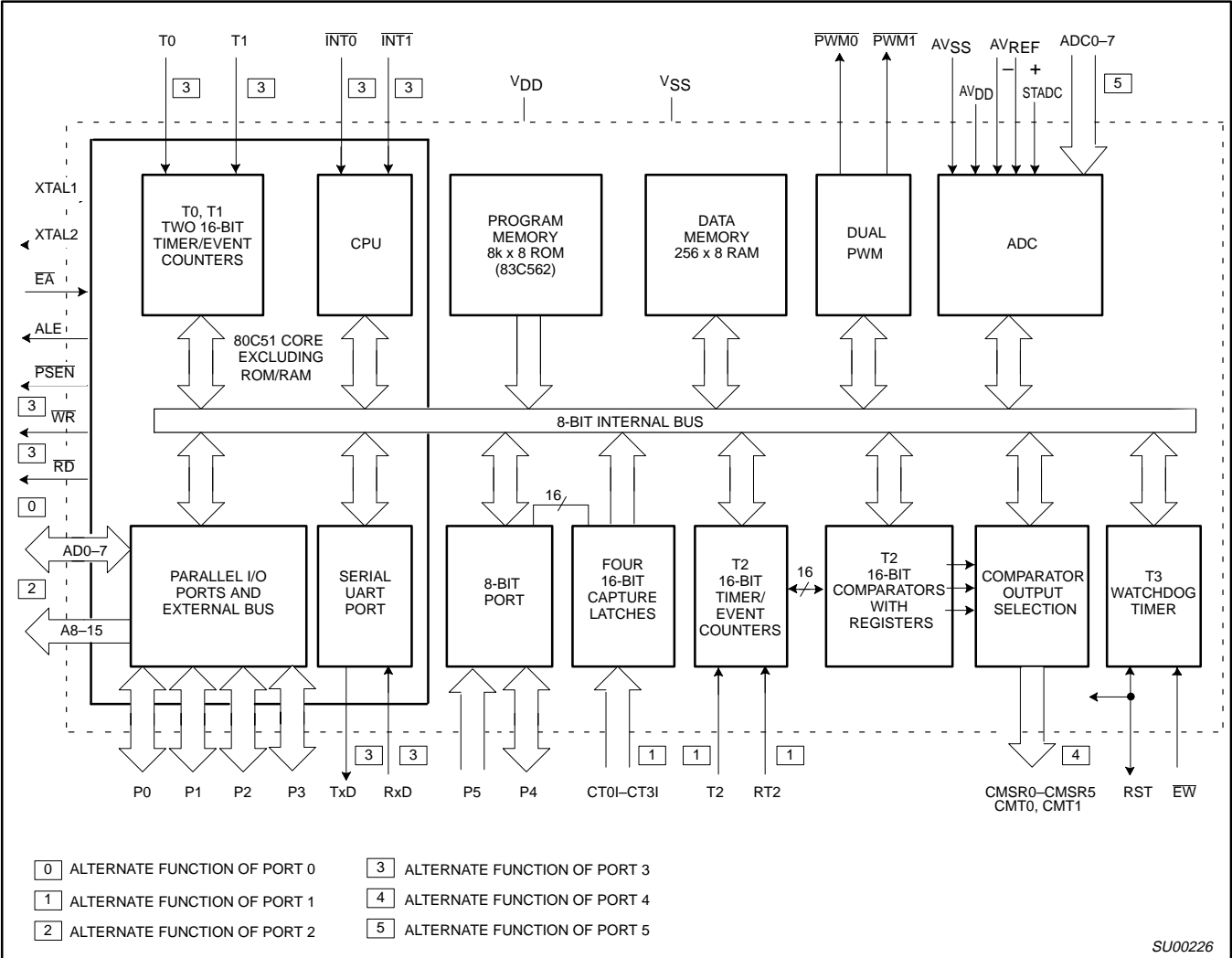
## LOGIC SYMBOL



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BLOCK DIAGRAM



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## PIN DESCRIPTION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
V <sub>DD</sub>	2	I	<b>Digital Power Supply:</b> +5V power supply pin during normal operation, idle and power-down mode.
STADC	3	I	<b>Start ADC Operation:</b> Input starting analog to digital conversion (ADC operation can also be started by software).
PWM0	4	O	<b>Pulse Width Modulation:</b> Output 0.
PWM1	5	O	<b>Pulse Width Modulation:</b> Output 1.
EW	6	I	<b>Enable Watchdog Timer:</b> Enable for T3 watchdog timer and disable power-down mode.
P0.0–P0.7	57–50	I/O	<b>Port 0:</b> Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application it uses strong internal pull-ups when emitting 1s.
P1.0–P1.7	16–23	I/O	<b>Port 1:</b> 8-bit I/O port. Alternate functions include: <b>(P1.0–P1.7):</b> Quasi-bidirectional port pins. <b>CT0I–CT3I (P1.0–P1.3):</b> Capture timer input signals for timer T2. <b>T2 (P1.4):</b> T2 event input <b>RT2 (P1.5):</b> T2 timer reset signal. Rising edge triggered.
	16–23	I/O	
	16–19	I/O	
	20	I	
	21	I	
P2.0–P2.7	39–46	I/O	<b>Port 2:</b> 8-bit quasi-bidirectional I/O port. Alternate function: High-order address byte for external memory (A08–A15).
P3.0–P3.7	24–31	I/O	<b>Port 3:</b> 8-bit quasi-bidirectional I/O port. Alternate functions include: <b>RxD(P3.0):</b> Serial input port. <b>TxD (P3.1):</b> Serial output port. <b>INT0 (P3.2):</b> External interrupt. <b>INT1 (P3.3):</b> External interrupt. <b>T0 (P3.4):</b> Timer 0 external input. <b>T1 (P3.5):</b> Timer 1 external input. <b>WR (P3.6):</b> External data memory write strobe. <b>RD (P3.7):</b> External data memory read strobe.
	24		
	25		
	26		
	27		
	28		
	29		
	30		
	31		
P4.0–P4.7	7–14	I/O	<b>Port 4:</b> 8-bit quasi-bidirectional I/O port. Alternate functions include: <b>CMSR0–CMSR5 (P4.0–P4.5):</b> Timer T2 compare and set/reset outputs on a match with timer T2. <b>CMT0, CMT1 (P4.6, P4.7):</b> Timer T2 compare and toggle outputs on a match with timer T2.
	7–12	O	
	13, 14	O	
P5.0–P5.7	68–62, 1	I	<b>Port 5:</b> 8-bit input port. <b>ADC0–ADC7 (P5.0–P5.7):</b> Alternate function: Eight input channels to ADC.
RST	15	I/O	<b>Reset:</b> Input to reset the 87C552. It also provides a reset pulse as output when timer T3 overflows.
XTAL1	35	I	<b>Crystal Input 1:</b> Input to the inverting amplifier that forms the oscillator, and input to the internal clock generator. Receives the external clock signal when an external oscillator is used.
XTAL2	34	O	<b>Crystal Input 2:</b> Output of the inverting amplifier that forms the oscillator. Left open–circuit when an external clock is used.
V <sub>SS</sub>	36, 37	I	<b>Digital ground.</b>
PSEN	47	O	<b>Program Store Enable:</b> Active-low read strobe to external program memory.
ALE	48	O	<b>Address Latch Enable:</b> Latches the low byte of the address during accesses to external memory. It is activated every six oscillator periods. During an external data memory access, one ALE pulse is skipped. ALE can drive up to eight LS TTL inputs and handles CMOS inputs without an external pull-up.
EA	49	I	<b>External Access:</b> When EA is held at TTL level high, the CPU executes out of the internal program ROM provided the program counter is less than 8192. When EA is held at TTL low level, the CPU executes out of external program memory. EA is not allowed to float.
AV <sub>REF–</sub>	58	I	<b>Analog to Digital Conversion Reference Resistor:</b> Low-end.
AV <sub>REF+</sub>	59	I	<b>Analog to Digital Conversion Reference Resistor:</b> High-end.
AV <sub>SS</sub>	60	I	<b>Analog Ground</b>
AV <sub>DD</sub>	61	I	<b>Analog Power Supply</b>

## NOTE:

1. To avoid “latch-up” effect at power-on, the voltage on any pin at any time must not be higher or lower than V<sub>DD</sub> +0.5V or V<sub>SS</sub> – 0.5V, respectively.

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**OSCILLATOR CHARACTERISTICS**

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator, as shown in the logic symbol.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

**RESET**

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), while the oscillator is running. To ensure a good power-on reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles. At power-on, the voltage on  $V_{DD}$  and RST must come up at the same time for a proper start-up.

**IDLE MODE**

In the idle mode, the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers

remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

**POWER-DOWN MODE**

In the power-down mode, the oscillator is stopped and the instruction to invoke power-down is the last instruction executed. Only the contents of the on-chip RAM are preserved. A hardware reset is the only way to terminate the power-down mode. The control bits for the reduced power modes are in the special function register PCON. Table 1 shows the state of the I/O ports during low current operating modes.

**Table 1. External Pin Status During Idle and Power-Down Modes**

MODE	PROGRAM MEMORY	ALE	PSEN	PORT 0	PORT 1	PORT 2	PORT 3	PORT 4	PWM0/PWM1
Idle	Internal	1	1	Data	Data	Data	Data	Data	High
Idle	External	1	1	Float	Data	Address	Data	Data	High
Power-down	Internal	0	0	Data	Data	Data	Data	Data	High
Power-down	External	0	0	Float	Data	Data	Data	Data	High

**ABSOLUTE MAXIMUM RATINGS<sup>1, 2, 3</sup>**

PARAMETER	RATING	UNIT
Voltage on any other pin to $V_{SS}$	-0.5 to +6.5	V
Input, output DC current on any single I/O pin	5.0	mA
Power dissipation (based on package heat transfer limitations, not device power consumption)	1.0	W
Storage temperature range	-65 to +150	°C

**NOTES:**

- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
- This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
- Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to  $V_{SS}$  unless otherwise noted.

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**DC ELECTRICAL CHARACTERISTICS** $V_{SS}, AV_{SS} = 0V$ 

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
$V_{DD}$	Supply voltage PCB8XC562 PCF8XC562 PCA8XC562		4.0 4.0 4.5	6.0 6.0 5.5	V V V
$I_{DD}$	Supply current operating: PCB8XC562 PCF8XC562 PCA8XC562	See notes 1 and 2 $f_{OSC} = 16MHz$ $f_{OSC} = 12MHz$ $f_{OSC} = 12MHz$		45 34 30	mA mA mA
$I_{ID}$	Idle mode: PCB8XC562 PCF8XC562 PCA8XC562	See notes 1 and 3 $f_{OSC} = 16MHz$ $f_{OSC} = 12MHz$ $f_{OSC} = 12MHz$		10 8 7	mA mA mA
$I_{PD}$	Power-down current:  PCB8XC562 PCF8XC562 PCA8XC562	See notes 1 and 4; $2V < V_{PD} < V_{DD} \text{ max}$		50 50 100	$\mu A$ $\mu A$ $\mu A$
<b>Inputs</b>					
$V_{IL}$	Input low voltage, except $\overline{EA}$		-0.5	$0.2V_{DD}-0.1$	V
$V_{IL1}$	Input low voltage to $\overline{EA}$		-0.5	$0.2V_{DD}-0.3$	V
$V_{IH}$	Input high voltage, except XTAL1, RST		$0.2V_{DD}+0.9$	$V_{DD}+0.5$	V
$V_{IH1}$	Input high voltage, XTAL1, RST		$0.7V_{DD}$	$V_{DD}+0.5$	V
$I_{IL}$	Logical 0 input current, ports 1, 2, 3, 4	$V_{IN} = 0.45V$		-50	$\mu A$
$I_{TL}$	Logical 1-to-0 transition current, ports 1, 2, 3, 4	See note 5		-650	$\mu A$
$\pm I_{IL1}$	Input leakage current, port 0, $\overline{EA}$ , STADC, $\overline{EW}$	$0.45V < V_I < V_{DD}$		10	$\mu A$
<b>Outputs</b>					
$V_{OL}$	Output low voltage, ports 1, 2, 3, 4	$I_{OL} = 1.6mA^6$		0.45	V
$V_{OL1}$	Output low voltage, port 0, ALE, $\overline{PSEN}$ , $\overline{PWM0}$ , $\overline{PWM1}$	$I_{OL} = 3.2mA^6$		0.45	V
$V_{OH}$	Output high voltage, ports 1, 2, 3, 4	$V_{DD} + 5V \pm 10\%$ $-I_{OH} = 60\mu A$ $-I_{OH} = 25\mu A$ $-I_{OH} = 10\mu A$	2.4 $0.75V_{DD}$ $0.9V_{DD}$		V V V
$V_{OH1}$	Output high voltage (port 0 in external bus mode, ALE, $\overline{PSEN}$ , $\overline{PWM0}$ , $\overline{PWM1}$ ) <sup>7</sup>	$V_{DD} + 5V \pm 10\%$ $-I_{OH} = 400\mu A$ $-I_{OH} = 150\mu A$ $-I_{OH} = 40\mu A$	2.4 $0.75V_{DD}$ $0.9V_{DD}$		V V V
$V_{OH2}$	Output high voltage (RST)	$-I_{OH} = 400\mu A$ $-I_{OH} = 120\mu A$	2.4 $0.8V_{DD}$		V V
$R_{RST}$	Internal reset pull-down resistor		50	150	k $\Omega$
$C_{IO}$	Pin capacitance	Test freq = 1MHz, $T_{amb} = 25^\circ C$		10	pF

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## DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
Analog Inputs					
AV <sub>DD</sub>	Analog supply voltage: PCB8XC562 PCF8XC562 PCA8XC562	AV <sub>DD</sub> = V <sub>DD</sub> ±0.2V AV <sub>DD</sub> = V <sub>DD</sub> ±0.2V AV <sub>DD</sub> = V <sub>DD</sub> ±0.2V	4.0 4.0 4.5	6.0 6.0 5.5	V V V
AI <sub>DD</sub>	Analog supply current: operating:	Port 5 = 0 to AV <sub>DD</sub>		1.2	mA
AI <sub>ID</sub>	Idle mode: PCB8XC562 PCF8XC562 PCA8XC562			50 50 100	μA μA μA
AI <sub>PD</sub>	Power-down mode: PCB8XC562 PCF8XC562 PCA8XC562	2V < AV <sub>PD</sub> < AV <sub>DD</sub> max		50 50 100	μA μA μA
AV <sub>IN</sub>	Analog input voltage		AV <sub>SS</sub> -0.2	AV <sub>DD</sub> +0.2	V
AV <sub>REF</sub>	Reference voltage: AV <sub>REF-</sub> AV <sub>REF+</sub>		AV <sub>SS</sub> -0.2	AV <sub>DD</sub> +0.2	V V
R <sub>REF</sub>	Resistance between AV <sub>REF+</sub> and AV <sub>REF-</sub>		5	25	kΩ
C <sub>IA</sub>	Analog input capacitance			15	pF
t <sub>ADS</sub>	Sampling time			6t <sub>CY</sub>	μs
t <sub>ADC</sub>	Conversion time (including sampling time)			24t <sub>CY</sub>	μs
DL <sub>e</sub>	Differential non-linearity <sup>8, 9, 10</sup>			±1	LSB
IL <sub>e</sub>	Integral non-linearity <sup>8, 11</sup>			±1	LSB
OS <sub>e</sub>	Offset error <sup>8, 12</sup>			±1	LSB
G <sub>e</sub>	Gain error <sup>8, 13</sup>			0.4	%
M <sub>CTC</sub>	Channel to channel matching			±1	LSB
C <sub>t</sub>	Crosstalk between inputs of port 5 <sup>14</sup>	0–100kHz		-60	dB

## NOTES:

- See Figures 8 through 12 for I<sub>DD</sub> test conditions.
- The operating supply current is measured with all output pins disconnected; XTAL1 driven with t<sub>r</sub> = t<sub>f</sub> = 10ns; V<sub>IL</sub> = V<sub>SS</sub> + 0.5V; V<sub>IH</sub> = V<sub>DD</sub> - 0.5V; XTAL2 not connected; EA = RST = Port 0 = EW = V<sub>DD</sub>; STADC = V<sub>SS</sub>.
- The idle mode supply current is measured with all output pins disconnected; XTAL1 driven with t<sub>r</sub> = t<sub>f</sub> = 10ns; V<sub>IL</sub> = V<sub>SS</sub> + 0.5V; V<sub>IH</sub> = V<sub>DD</sub> - 0.5V; XTAL2 not connected; Port 0 = EW = V<sub>DD</sub>; EA = RST = STADC = V<sub>SS</sub>.
- The power-down current is measured with all output pins disconnected; XTAL2 not connected; Port 0 = EW = V<sub>DD</sub>; EA = RST = STADC = XTAL1 = V<sub>SS</sub>.
- Pins of ports 1, 2, 3, and 4 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V<sub>IN</sub> is approximately 2V.
- Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V<sub>OL</sub>s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I<sub>OL</sub> can exceed these conditions provided that no single output sinks more than 5mA and no more than two outputs exceed the test conditions.
- Capacitive loading on ports 0 and 2 may cause the V<sub>OH</sub> on ALE and PSEN to momentarily fall below the 0.9V<sub>DD</sub> specification when the address bits are stabilizing.
- Conditions: AV<sub>REF-</sub> = 0V; AV<sub>DD</sub> = 5.0V; AV<sub>REF+</sub> = 5.12V. ADC is monotonic with no missing codes.
- The differential non-linearity (DL<sub>e</sub>) is the difference between the actual step width and the ideal step width. (See Figure 1.)
- The ADC is monotonic; there are no missing codes.
- The integral non-linearity (IL<sub>e</sub>) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset error. (See Figure 1.)
- The offset error (OS<sub>e</sub>) is the absolute difference between the straight line which fits the actual transfer curve (after removing gain error), and a straight line which fits the ideal transfer curve. (See Figure 1.)
- The gain error (G<sub>e</sub>) is the relative difference in percent between the straight line fitting the actual transfer curve (after removing offset error), and the straight line which fits the ideal transfer curve. Gain error is constant at every point on the transfer curve. (See Figure 1.)
- This should be considered when both analog and digital signals are simultaneously input to port 5.



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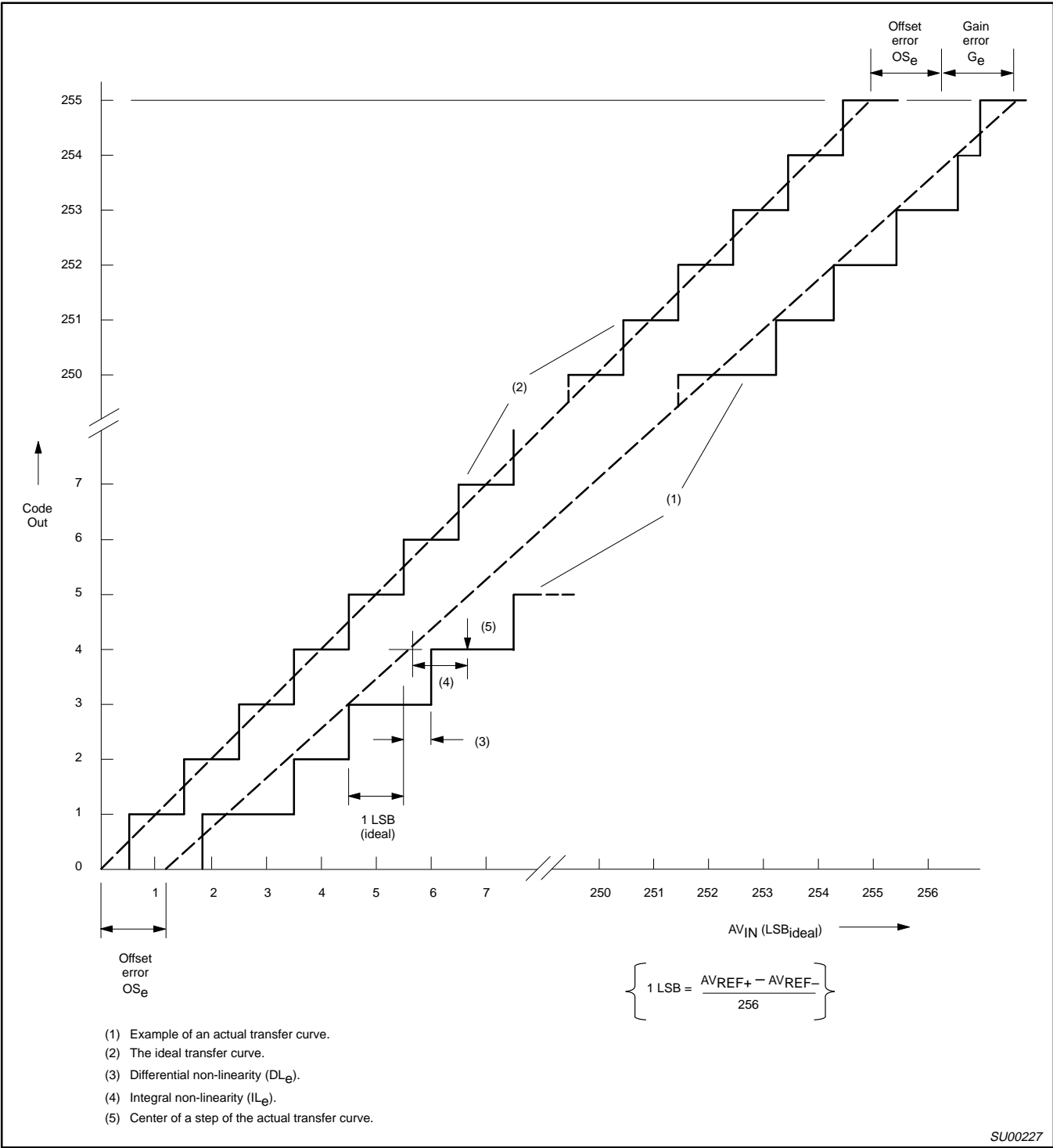


Figure 1. ADC Conversion Characteristic

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AC ELECTRICAL CHARACTERISTICS<sup>1, 2</sup>

SYMBOL	FIGURE	PARAMETER	12MHz CLOCK		VARIABLE CLOCK		UNIT
			MIN	MAX	MIN	MAX	
1/t <sub>CLCL</sub>	2	Oscillator frequency			1.2	16	MHz
t <sub>LHLL</sub>	2	ALE pulse width	127		2t <sub>CLCL</sub> -40		ns
t <sub>AVLL</sub>	2	Address valid to ALE low	28		t <sub>CLCL</sub> -55		ns
t <sub>LLAX</sub>	2	Address hold after ALE low	48		t <sub>CLCL</sub> -35		ns
t <sub>LLIV</sub>	2	ALE low to valid instruction in		234		4t <sub>CLCL</sub> -100	ns
t <sub>LLPL</sub>	2	ALE low to PSEN low	43		t <sub>CLCL</sub> -40		ns
t <sub>PLPH</sub>	2	PSEN pulse width	205		3t <sub>CLCL</sub> -45		ns
t <sub>PLIV</sub>	2	PSEN low to valid instruction in		145		3t <sub>CLCL</sub> -105	ns
t <sub>PXIX</sub>	2	Input instruction hold after PSEN	0		0		ns
t <sub>PXIZ</sub>	2	Input instruction float after PSEN		59		t <sub>CLCL</sub> -25	ns
t <sub>AVIV</sub>	2	Address to valid instruction in		312		5t <sub>CLCL</sub> -105	ns
t <sub>PLAZ</sub>	2	PSEN low to address float		10		10	ns
<b>Data Memory</b>							
t <sub>AVLL</sub>	3, 4	Address valid to ALE low	43		t <sub>CLCL</sub> -35		ns
t <sub>RLRH</sub>	3	RD pulse width	400		6t <sub>CLCL</sub> -100		ns
t <sub>WLWH</sub>	4	WR pulse width	400		6t <sub>CLCL</sub> -100		ns
t <sub>RLDV</sub>	3	RD low to valid data in		252		5t <sub>CLCL</sub> -165	ns
t <sub>RHDX</sub>	3	Data hold after RD	0		0		ns
t <sub>RHDZ</sub>	3	Data float after RD		97		2t <sub>CLCL</sub> -70	ns
t <sub>LLDV</sub>	3	ALE low to valid data in		517		8t <sub>CLCL</sub> -150	ns
t <sub>AVDV</sub>	3	Address to valid data in		585		9t <sub>CLCL</sub> -165	ns
t <sub>LLWL</sub>	3, 4	ALE low to RD or WR low	200	300	3t <sub>CLCL</sub> -50	3t <sub>CLCL</sub> +50	ns
t <sub>AVWL</sub>	3, 4	Address valid to WR low or RD low	203		4t <sub>CLCL</sub> -130		ns
t <sub>QVWX</sub>	4	Data valid to WR transition	23		t <sub>CLCL</sub> -60		ns
t <sub>DW</sub>	4	Data before WR	433		7t <sub>CLCL</sub> -150		ns
t <sub>WHQX</sub>	4	Data hold after WR	33		t <sub>CLCL</sub> -50		ns
t <sub>RLAZ</sub>	3	RD low to address float		0		0	ns
t <sub>WHLH</sub>	3, 4	RD or WR high to ALE high	43	123	t <sub>CLCL</sub> -40	t <sub>CLCL</sub> +40	ns
<b>External Clock</b>							
t <sub>CHCX</sub>	5	High time <sup>3</sup>	20		20		ns
t <sub>CLCX</sub>	5	Low time <sup>3</sup>	20		20		ns
t <sub>CLCH</sub>	5	Rise time <sup>3</sup>		20		20	ns
t <sub>CHCL</sub>	5	Fall time <sup>3</sup>		20		20	ns

## NOTES:

- Parameters are valid over operating temperature range unless otherwise specified.
- Load capacitance for port 0, ALE, and PSEN = 100pF, load capacitance for all other outputs = 80pF.
- These values are characterized but not 100% production tested.

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## EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

A – Address

C – Clock

D – Input data

H – Logic level high

I – Instruction (program memory contents)

L – Logic level low, or ALE

P –  $\overline{\text{PSEN}}$

Q – Output data

R –  $\overline{\text{RD}}$  signal

t – Time

V – Valid

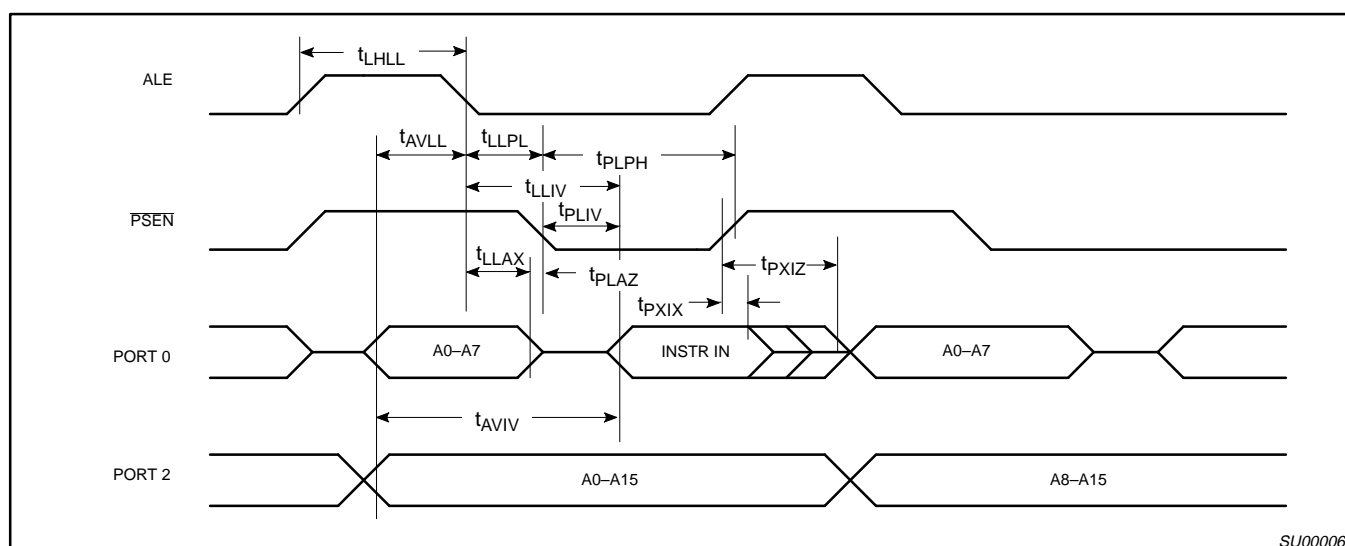
W –  $\overline{\text{WR}}$  signal

X – No longer a valid logic level

Z – Float

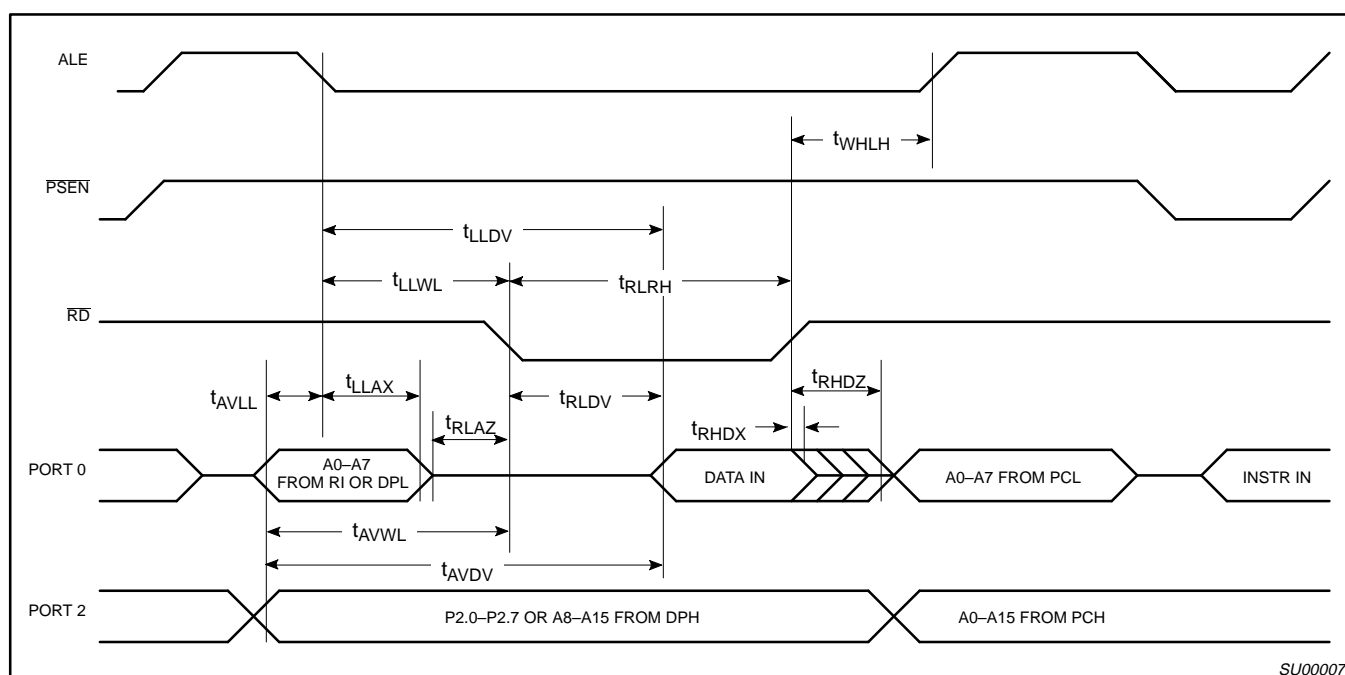
**Examples:**  $t_{\text{AVLL}}$  = Time for address valid to ALE low.

$t_{\text{LLPL}}$  = Time for ALE low to  $\overline{\text{PSEN}}$  low.



SU00006

Figure 2. External Program Memory Read Cycle



SU00007

Figure 3. External Data Memory Read Cycle

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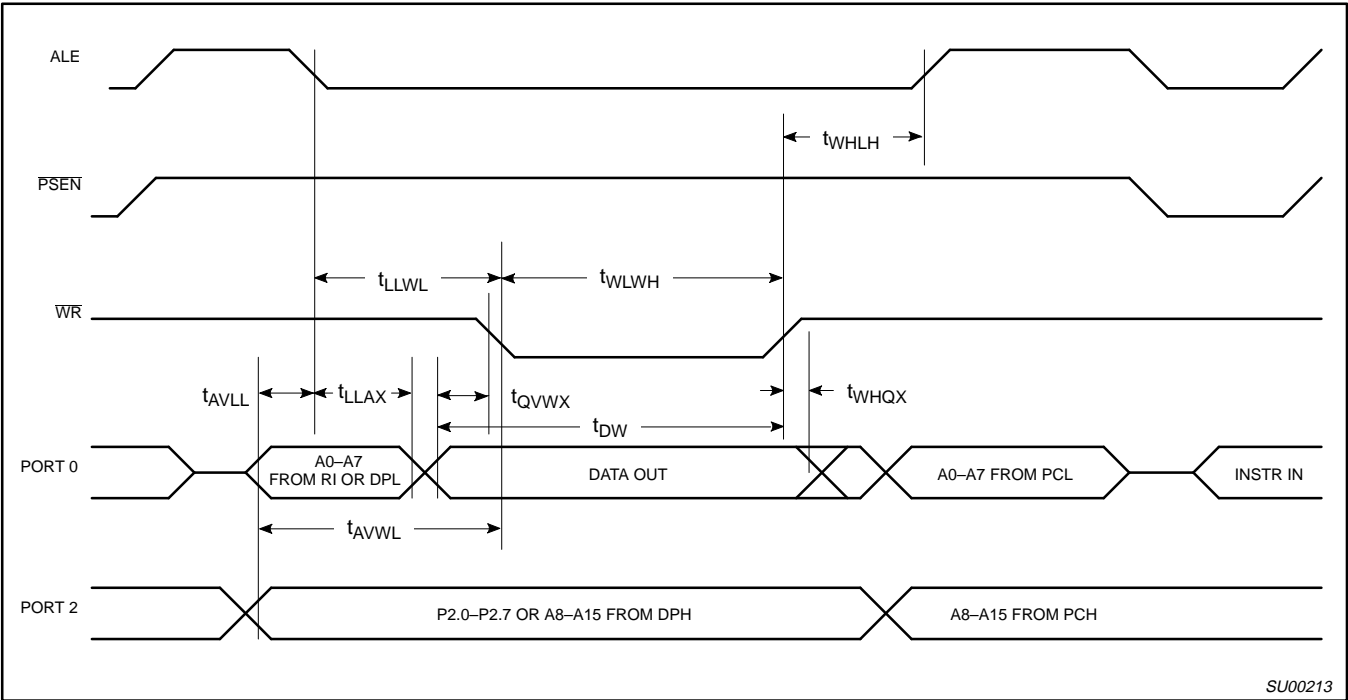


Figure 4. External Data Memory Write Cycle

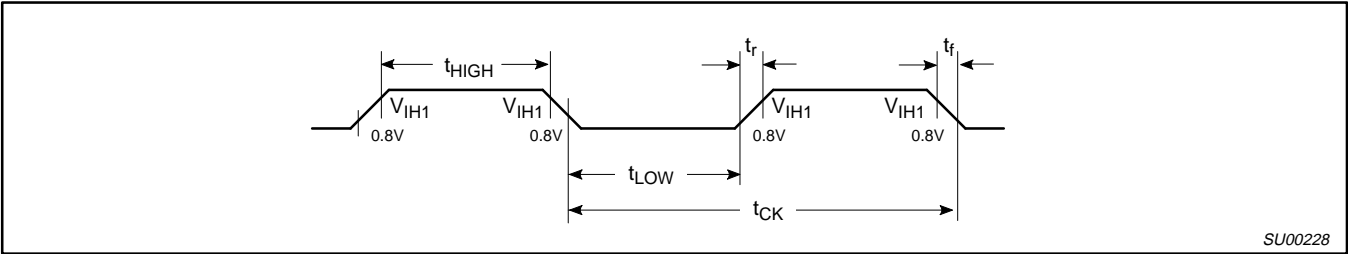


Figure 5. External Clock Drive XTAL1

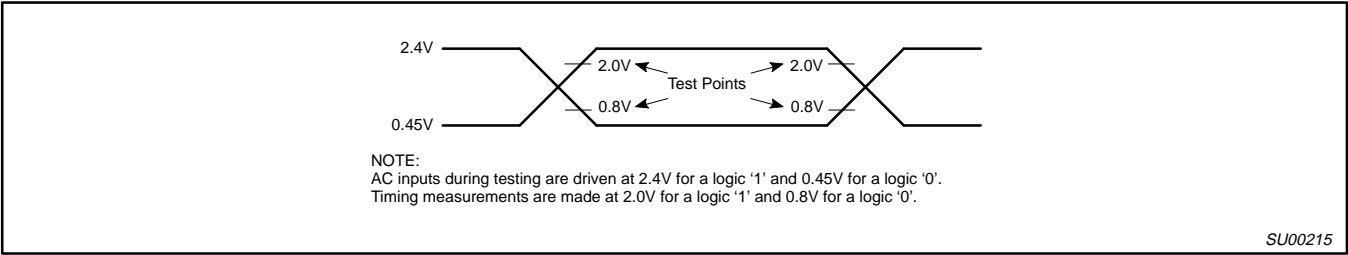


Figure 6. AC Testing Input/Output

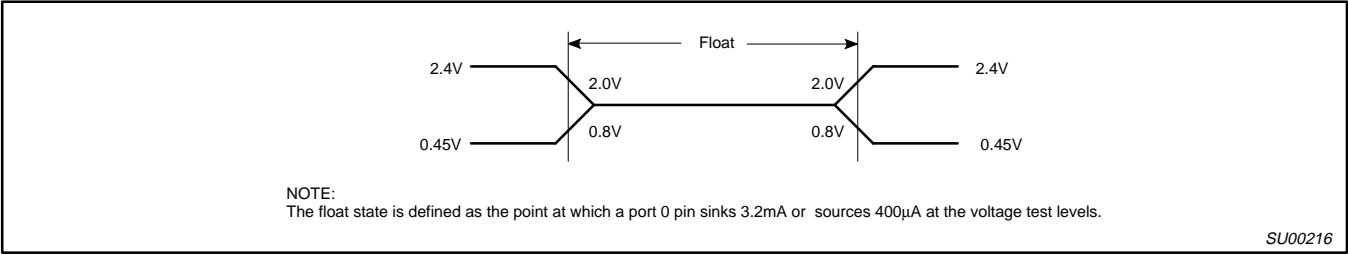


Figure 7. AC Testing Input, Float Waveform

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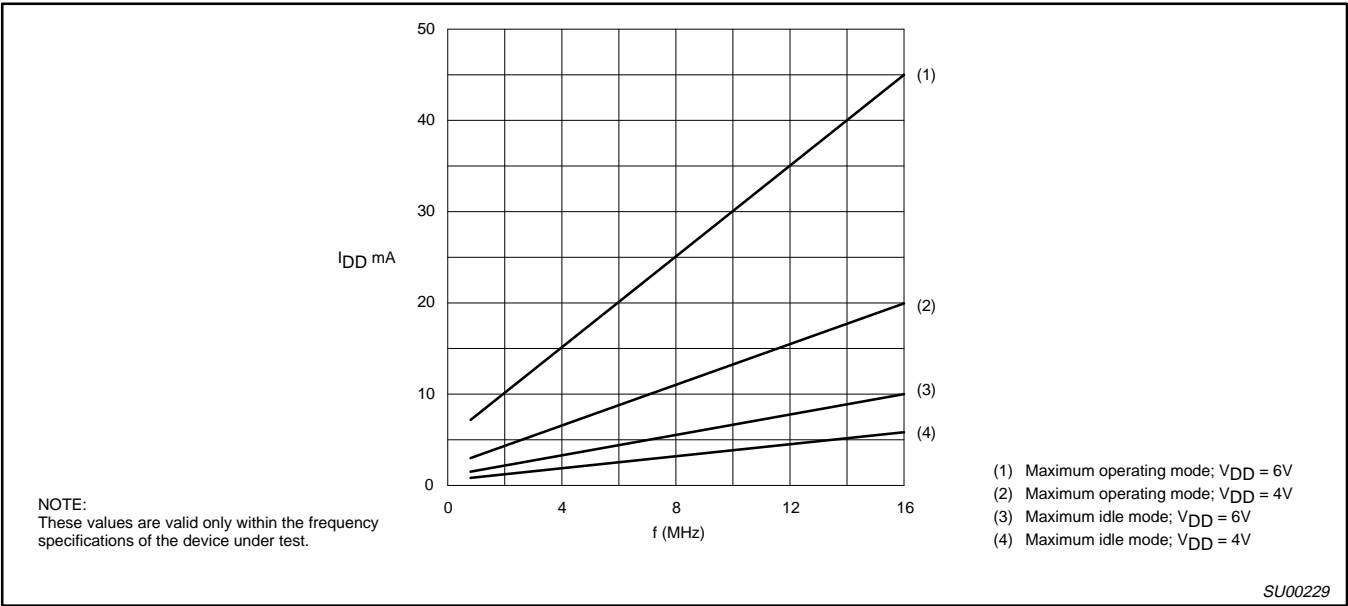


Figure 8. Supply Current ( $I_{DD}$ ) as a Function of Frequency at XTAL1 ( $f_{osc}$ )

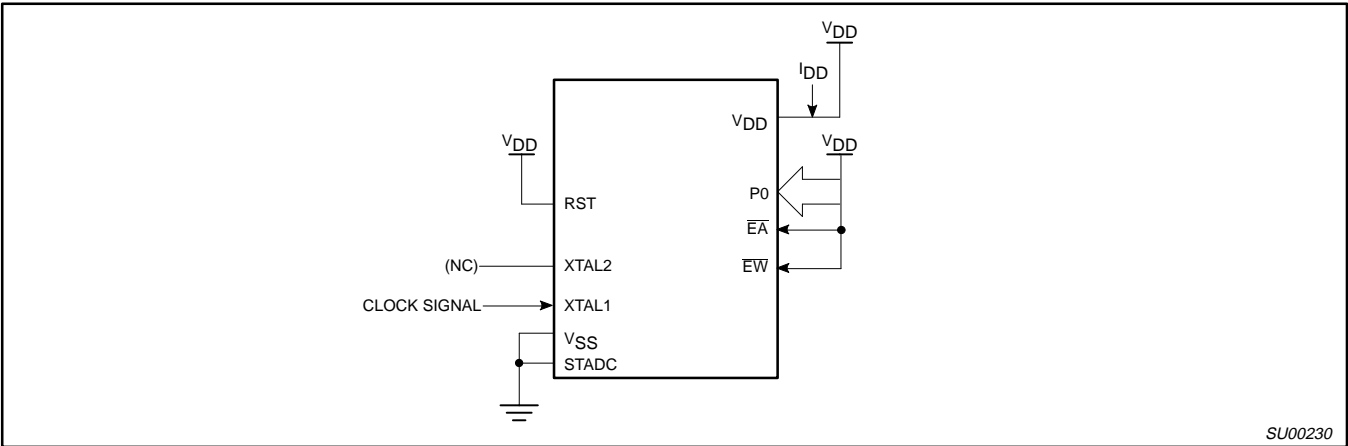


Figure 9.  $I_{DD}$  Test Condition, Active Mode  
All other pins are disconnected

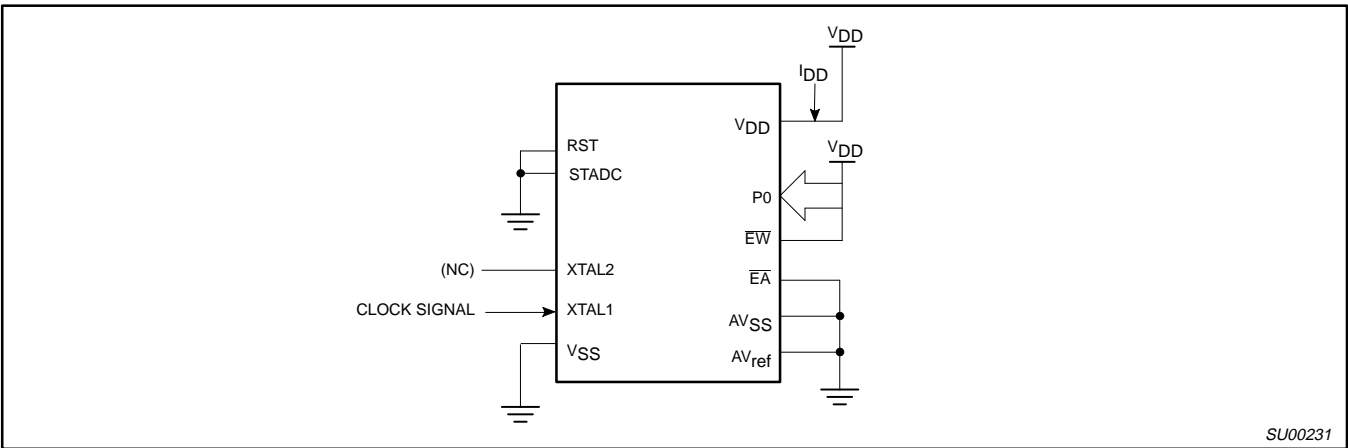


Figure 10.  $I_{DD}$  Test Condition, Idle Mode  
All other pins are disconnected

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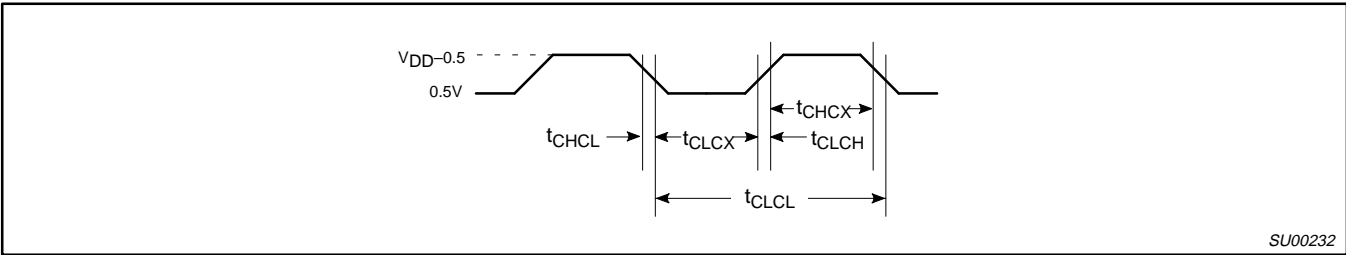


Figure 11. Clock Signal Waveform for  $I_{DD}$   
Tests in Active and Idle Modes  
 $t_{CLCH} = t_{CHCL} = 10\text{ns}$

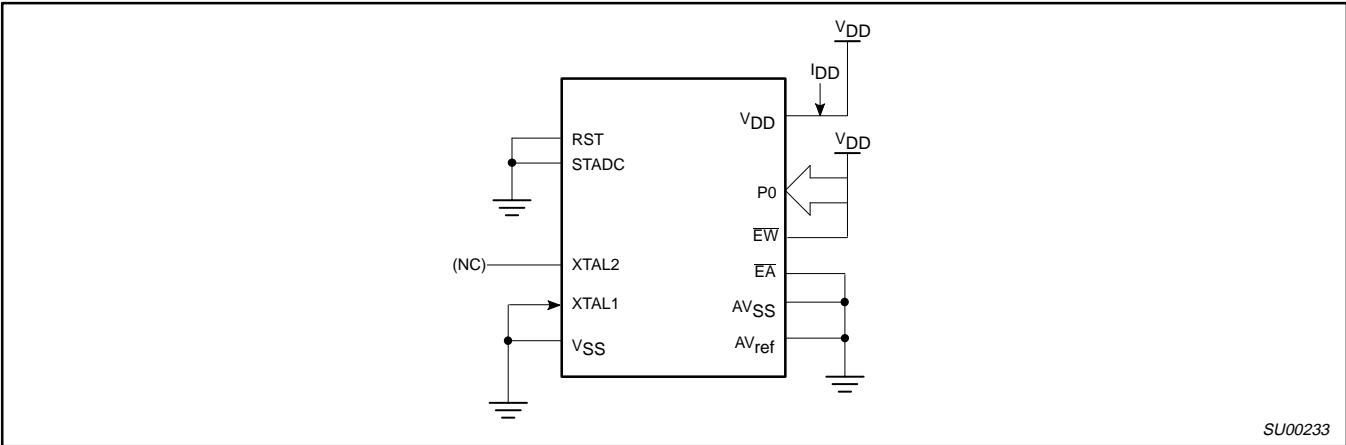


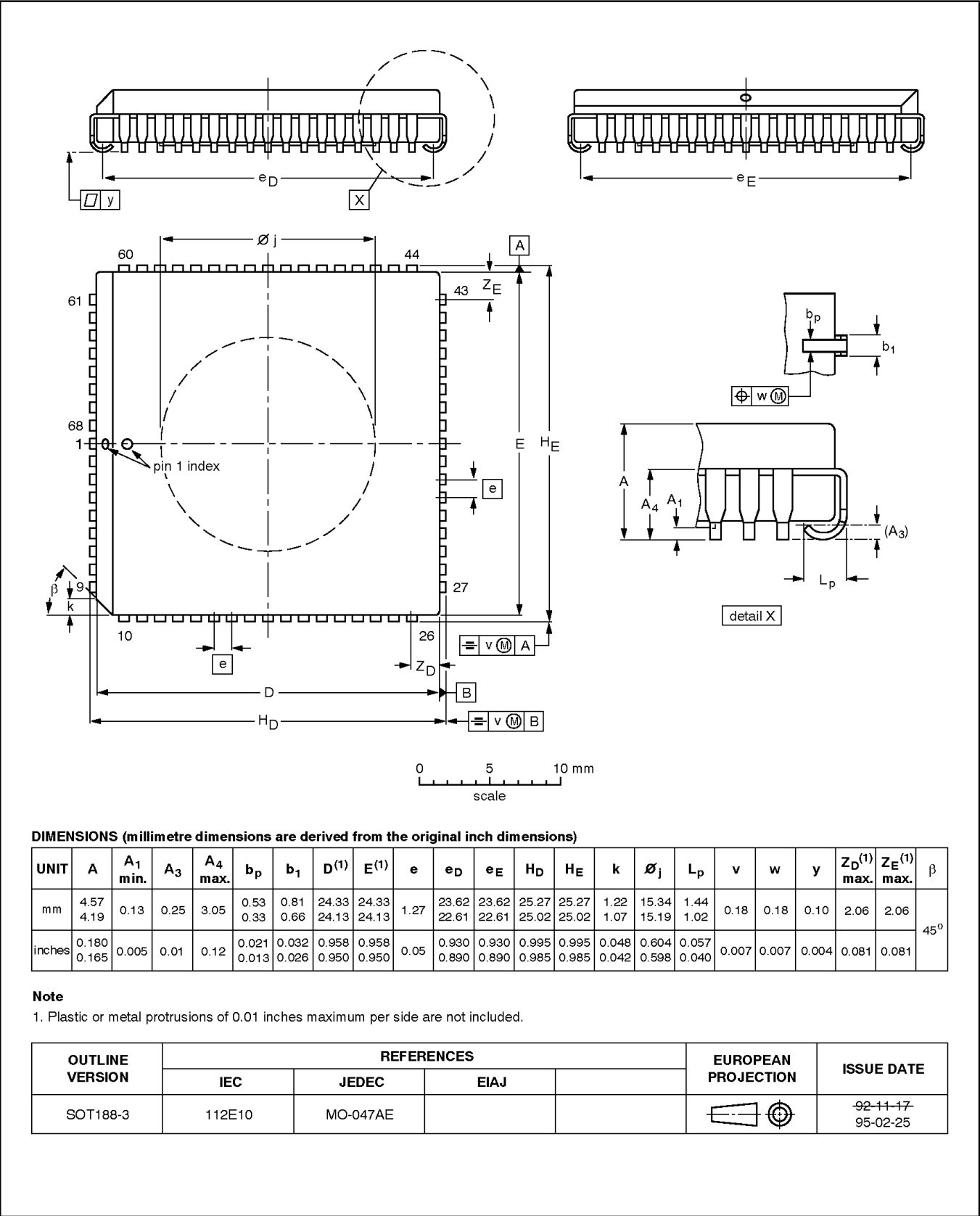
Figure 12.  $I_{DD}$  Test Condition, Power Down Mode  
All other pins are disconnected.  $V_{DD} = 2\text{V to } 5.5\text{V}$

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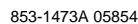
PLCC68: plastic leaded chip carrier; 68 leads; pedestal

SOT188-3



## 80C562/83C562

## 1473A 68-PIN CERQUAD J-BEND (K) PACKAGE





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**NOTES**

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DEFINITIONS		
Data Sheet Identification	Product Status	Definition
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