ICs for Communications

Broadband Multichannel Subscriber Line-Interface Circuits for Splitterless G.Lite Applications
B-MuSLIC

PEB 4550
PEB 3554
PEB 55504
PEB 35508

Preliminary Product Overview 05.99

B-MuSLIC Revision History:		Current Version: 05.99
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Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)

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SC,
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Preface

This document summarizes the Broadband Multichannel Subscriber Line-Interface Circuits for Splitterless G.Lite Applications (B-MuSLIC). The B-MuSLIC is a highly integrated chipset integrating ADSL-Lite functionality with the proven MuSLIC PCM codec filter for analog telephony applications. This product provides all ADSL-Lite functionality required by ITU-T G.992.2, and provides software-programmable BORSCHT functionality to meet worldwide voice telephony standards. The B-MuSLIC provides up to 8 ADSL Lite and analog voice channels, is totally programmable, and integrates many previously external functions on-chip.

This document contains general information about the B-MuSLIC and describes in brief the main features, functional blocks, interfaces, and typical applications of the chipset. Please refer to Related Documentation for technical specifications.

Related Documentation

Product Overview MuCaDo (MultiChannel Asymmetrical DSL System for G.Lite)

Conventions Used in This Document

Abbreviations and acronyms are shown at the end of the document.

1 Overview

The B-MuSLIC chipset (Figure 1-1) is used in ADSL-Lite DSLAMs for Central Offices (COs) and Digital-Loop Carrier systems (DLCs).

The **B-MuSLIC** (Broadband Multichannel Subscriber Line-Interface Circuits for Splitterless G.Lite Applications) chipset comprises:

- **B-SLIC** (PEB 4550 Broadband Ringing SLIC)
  - Single-channel Broadband Subscriber Line Circuit
- **B-QAP** (PEB 3554) ADSL.lite Analog Frontend
  - 4-channel AD/DA converter with integrated filters
- **ALiDD** (PEB 55504)
  - 4-channel ADSL-Lite Data Pump compatible with G.Lite standard
- **B-MuPP** (PEB 35508 Broadband Multichannel Processor for POTS)
  - 8-channel voice processing DSP with µC and PCM/IOM2 interface

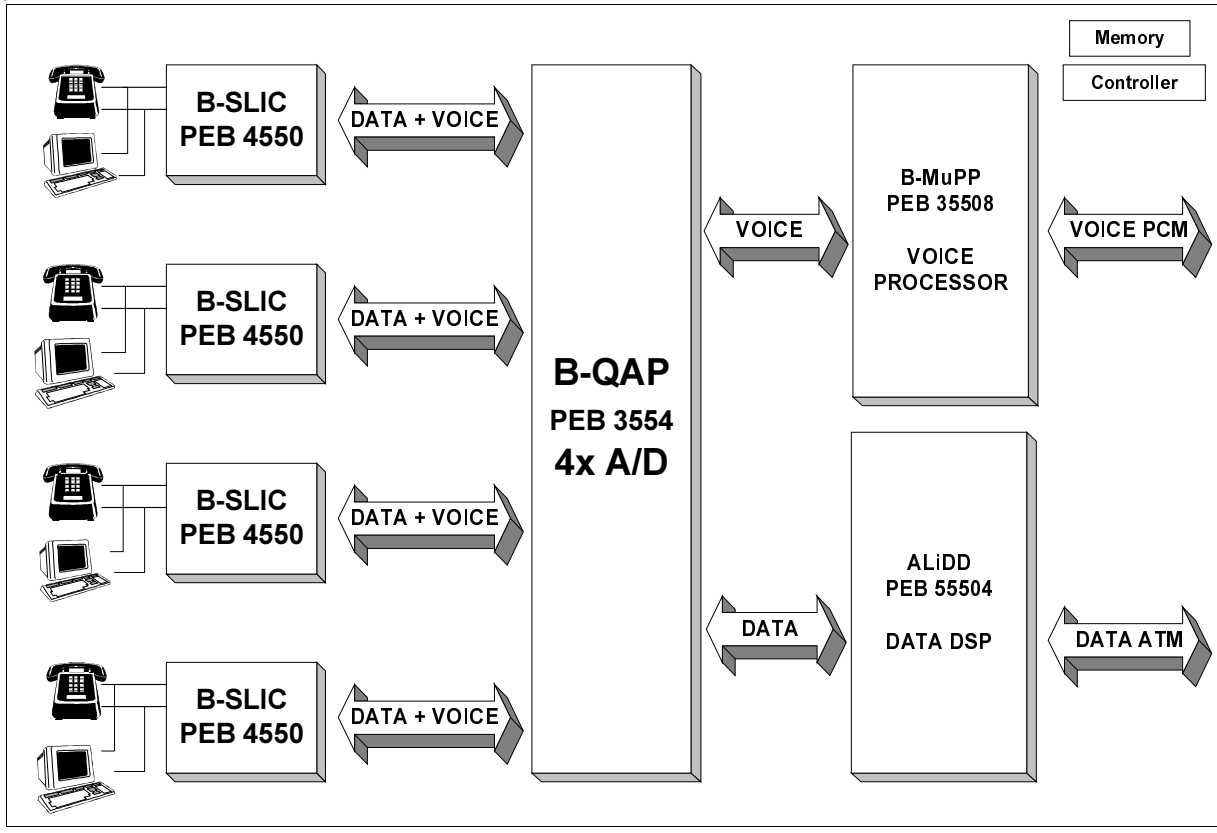


Figure 1-1 Architecture of B-MuSLIC Chipset on an ADSL-Lite Linecard

ADSL-Lite Linecard Architecture

The B-MuSLIC chipset supports data transmission at rates of 1536 kbps downstream and 512 kbps upstream simultaneously with voice transmission. Eight-bit data is sent to the ALiDD using a Utopia-2 ATM interface, while voice is sent to the B-MuPP using either a PCM highway or the IOM-2 interface (Figure 1-3). Programming, control, and signalling information from the ALiDD and the B-MuPP is sent to the local processor via a flexible 8-bit parallel µP interface.

ADSL-Lite utilizes the existing copper pair that traditionally has been used only for POTS service. ADSL-Lite offers subscribers the advantage of concurrent splitterless data and voice transmission. The data and voice services are separated within the B-MuSLIC chipset; thus, no external splitter is required (Figure 1-1). For each channel, the linecard provides a line driver, an A/D and D/A converter, and an ADSL-Lite data pump.

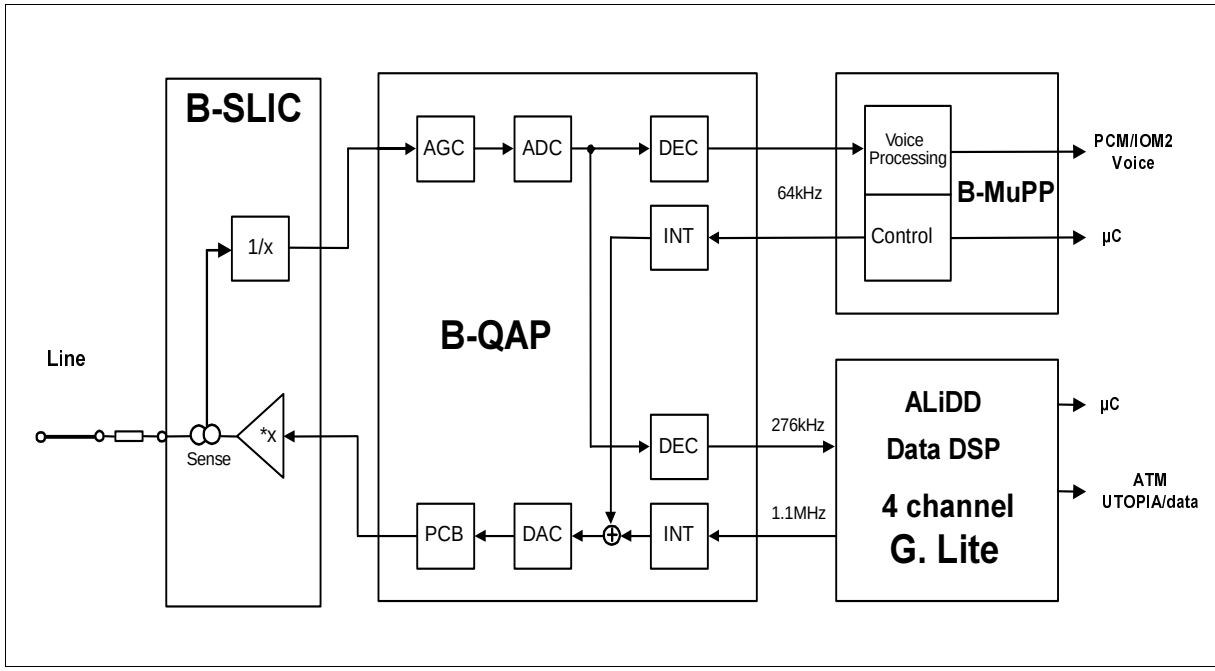


Figure 1-2 General Architecture of the ADSL-Lite Linecard

The B-MuSLIC is an optimized and integrated solution for linecards, providing 4 channels of ADSL-Lite data transmission at 1536 kbps downstream and up to 512 kbps upstream in one chipset.

Eight-bit data is sent to the ALiDD using an Utopia-2 ATM interface. Programming and control information for ALiDD and B-MuPP is exchanged with a local processor via a flexible 8- or 16-bit parallel µP interface.

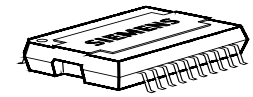
1.1 Features

- Application for COs, Access Networks (ANs), DLCs, PBXs
- Highly integrated
- 8-channel G.992.2 (ADSL-lite) compliant
- Data pump fully software upgradeable
- Integrated data/voice separation, no additional POTS Splitter required
- No separate ADSL Linecard required, no DSLAM required
- µC/PCM and IOM-2 Interfaces for voice
- Data interface switchable between Utopia-2 or µC interface
- Integrated programmable balanced ringing (85 Vrms) with support for external unbalanced ringing
- Voice telephony in accordance with relevant ITU-T Q.552 Z interface, LSSGR, Bellcore, and DTAG recommendations
- Channel-independent programmable filters for country-specific requirements:
  - Impedance matching
  - Transhybrid balancing
  - Frequency response
  - Receive/transmit levels
  - DC-feeding
- Line supervision
- Integrated Test and Diagnostic Functionality (ITDF)
  - Line test, circuit test, board test
- Utopia-2 compliant data interface
- µC Interface for chipset control
- High-performance 13-bit A/D and D/A conversion
- GPIO pins
- Data-only mode uses tones #1-5 for upstream direction (optional)
- Chipset family offers
  - Migration path to full-rate ADSL
  - Higher integration (fewer external parts, more channels)
  - Solution for DSLAMs (ADSL-Lite data only); refer to separate product overview
- Power Down Mode with Off-Hook (Voice) and Remote Active Request (Data) detection; each channel can be powered down individually

1.2 Typical Applications

Many applications benefit from the highly integrated, versatile B-MuSLIC architecture. Product reliability and manufacturability are enhanced by the high level of integration and by fabrication in low-power mixed-signal CMOS technology. The inherent flexibility and scalability reduces time-to-market, inventory costs, and support administration. The following list and figures show some of the typical applications for which the B-MuSLIC was designed.

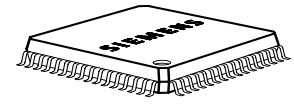
- Highly integrated ADSL-Lite linecards for linecards with 4, 8, or more channels in:
  - COs (Figure 1-3)
  - PBXs
  - ANs
  - DLCs



P-DSO-20-5

P-MQFP-100-2

P-TQFP-144-1



P-MQFP-64-1

Type	Package
PEB 4550	P-DSO-20-5
PEB 3554	P-MQFP-100-2
PEB 55504	P-TQFP-144-1
PEB 35508	P-MQFP-64-1

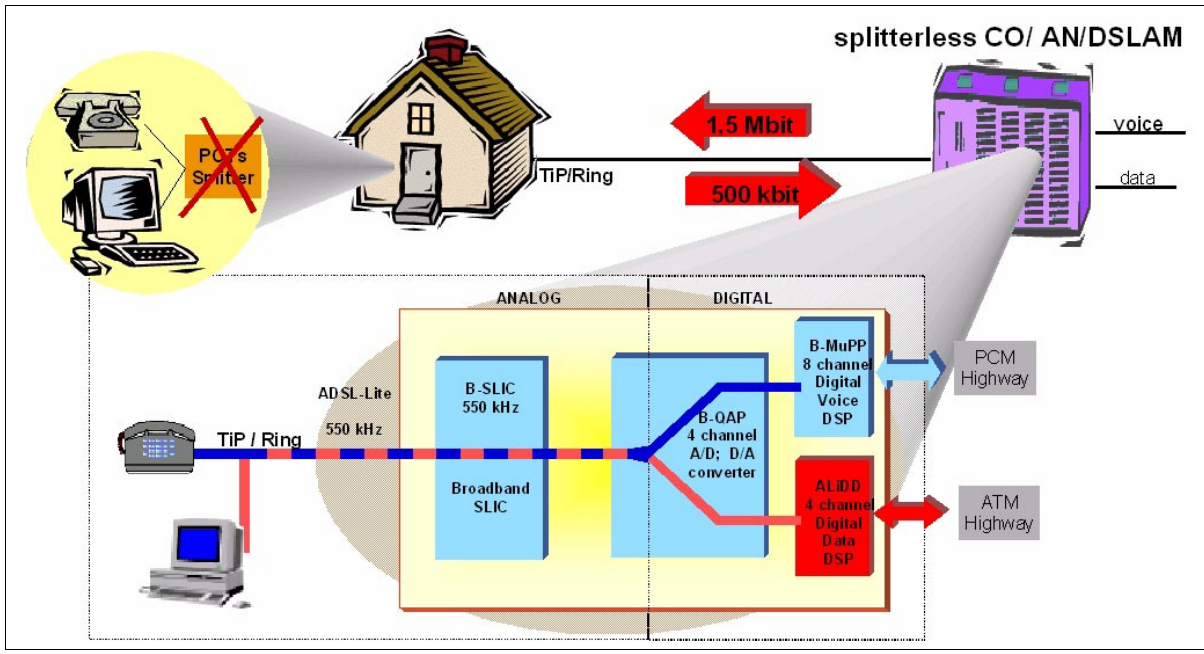


Figure 1-3 ADSL-Lite Linecard in a Central Office

An 8-channel ADSL-Lite linecard in a Central Office is depicted in Figure 1-4. The B-MuSLIC chipset or a 8-channel data/voice linecard consists of:

– 8 x B-SLIC
– 2 x B-QAP
– 2 x ALiDD
– 1 x B-MuPP

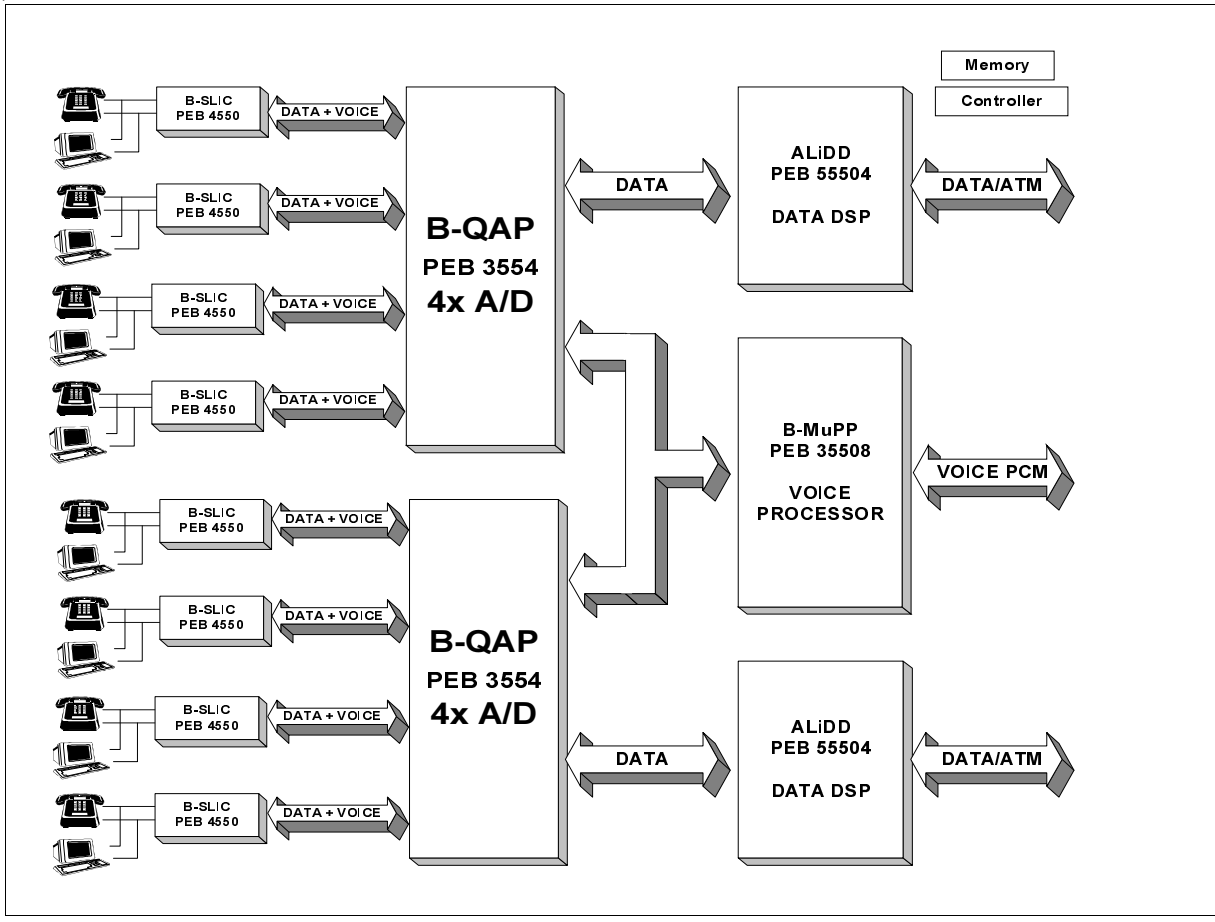


Figure 1-4 8-Channel ADSL-Lite Linecard in a Central Office

1.3 Product Family Overview

This document describes the B-MuSLIC and its features. The roadmap for the B-MuSLIC includes higher integration, and the B-MuSLIC-F, which will support full-rate ADSL according to G.992.1.

For data-only G.Lite DSLAM applications, refer to the MuCADO L/F documentation.

In contrast to the B-MuSLIC architecture described above, the MuCADO L is a highly integrated chipset solution for ADSL-Lite data-only service without voice-transmission. It is targeted at DSLAM applications that support ADSL-Lite.

2 Functional Description

This section describes the functional blocks of the B-MuSLIC chipset (Figure 2-1). Functions are described in detail in the following sections:

- 2.3 ALiDD ADSL-Lite Data Pump Functions
- 2.2 B-QAP ADSL-Lite Analog Frontend
- 2.4 B-MuPP
- 2.1 B-SLIC
- 2.5 Interfaces
- 2.6 Programmable Voice-path Parameter
- 2.7 Power Dissipation
- 2.8 Programmable Parameters

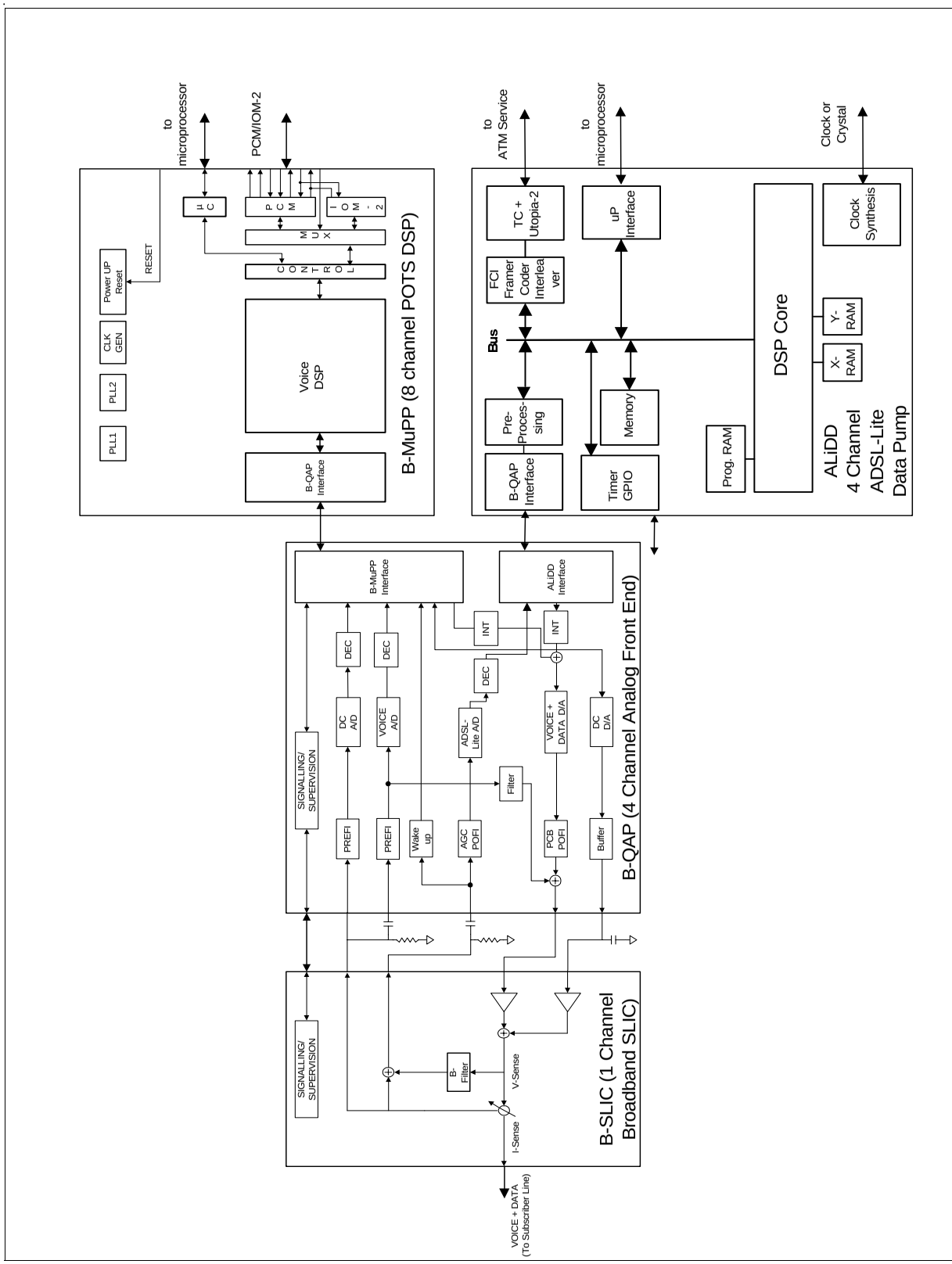


Figure 2-1 B-MuSLIC chipset block diagram

The B-MuSLIC chipset is a cost-effective, high-performance solution for Integrated Voice and Data (IVD) ADSL-Lite linecards according to the ITU-T recommendation G.992.2. It offers splitterless operation (no splitter in CO and no splitter at CPE needed) and a fully-featured solution for voice telephony.

The detailed functional block (Figure 2-5) shows how all G.992.2 functions and voice functions are implemented using 4 integrated circuits. The ALiDD is a DSP optimized for ADSL-Lite; it offers an Utopia-2 interface for data, and a synchronous parallel µC interface for programming and control. The mixed-signal B-QAP provides 4 channels of A/D and D/A conversion and filtering. The B-MuPP is a digital signal processor for analog voice telephony, controls the B-QAP and generates required clocks. Its parallel interface connects to a µC. The B-SLIC provides all necessary line feeding functionality and has very low harmonic distortion.

2.1 B-SLIC

The B-SLIC (Broadband Subscriber Line Interface Circuit) is used as the interface between the telephone line and the B-QAP/B-MuPP/ALIDD within integrated voice and data linecards. It offers high-voltage functionality.

Features:

- High-voltage line feeding
- Very linear data transmission
  - THD = -70dB at 550 kHz (downstream)
  - GBW = 20 MHz (downstream)
- Power Spectral Density -40dBm/Hz
- Internal ring signal injection up to 85 Vrms (balanced)
- Sensing of transversal and longitudinal line current
- Reliable170 V SMART technology
- Boosted battery mode for long telephone lines
- Thermal shutdown
- Small P-DSO-20 power package

2.2 B-QAP ADSL-Lite Analog Frontend

The B-QAP contains all analog frontend functions for 4 independent voice and G-Lite channels with separate interfaces to 4 B-SLICs. In the downstream direction, the serial data bitstream received from the ALiDD and the serial voice bitstream received from the B-MuPP is combined into on datastream and then converted to analog with a D/A converter. The signal passes a programmable gain stage before it reaches the external B-SLIC. In the upstream direction, the received signal is converted to a digital data stream and then separated into the data bitstream for ALiDD and the voice bitstream for

B-MuPP. After passing hardware filters the bitstream is transferred to the ALiDD and B-MuPP.

Also common to all 4 channels are the serial, digital interfaces to ALiDD and to B-MuPP.

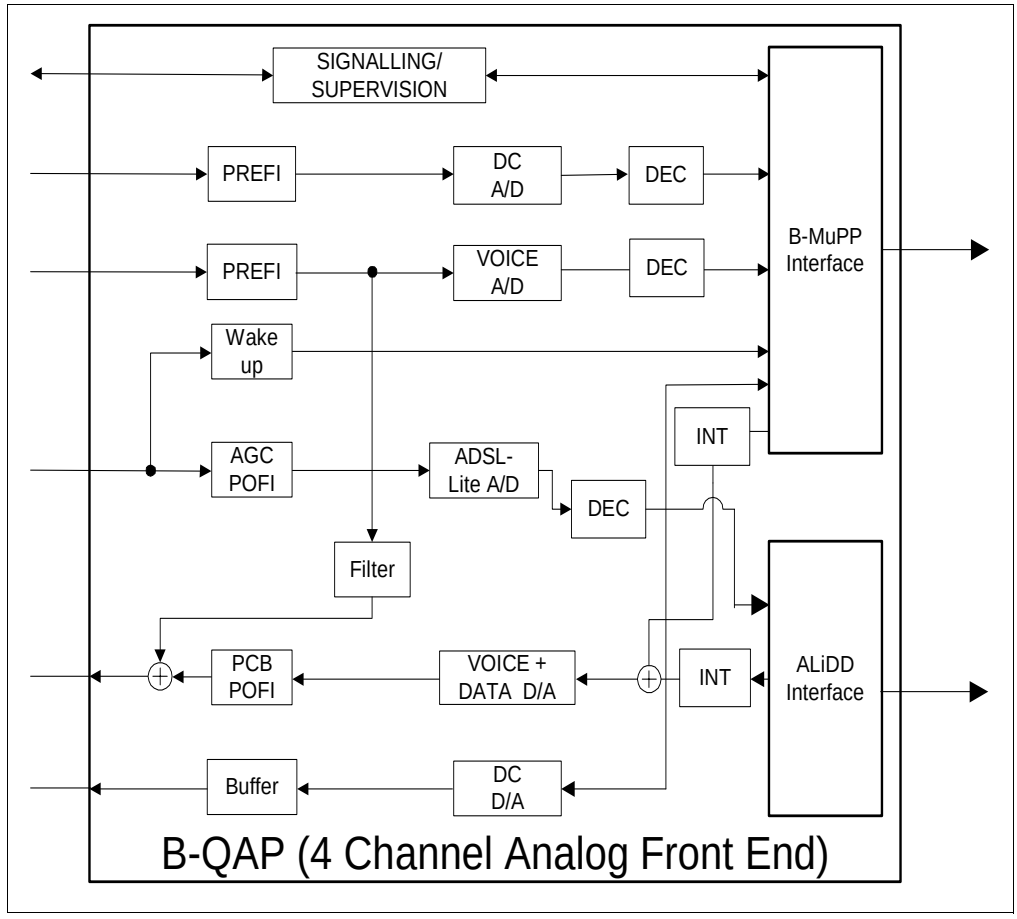


Figure 2-2 ADSL-Lite Analog Frontend B-QAP (Only 1 of 4 Channels Shown)

Features:

- 4-channel analog frontend for POTS and G.Lite data transmission
- No trimming or adjustments required
- Advanced low-power 0.5-µm BiCMOS technology
- High performance 13-bit A/D and D/A conversion
- 4-pin serial interface to B-MUPP for voice path
- Differential analog inputs/outputs
- 3 operating modes: Power-down, Active (voice and /or data) and Ringing
- Programmable transmit gain for power cut back on short lines
- Automatic gain control
- Very low noise and distortion in whole downstream path
- 5-pin serial interface to ALiDD for data path
- BiCMOS technology

- Standard SMD P-MQFP-100-2 package

2.3 ALiDD ADSL-Lite Data Pump Functions

The ALiDD is an ITU-T G.992.2-compliant data pump capable of handling up to 4 channels of G.Lite. The ALiDD has a flexible architecture to ensure compatibility with future versions and extensions of the standard.

Features

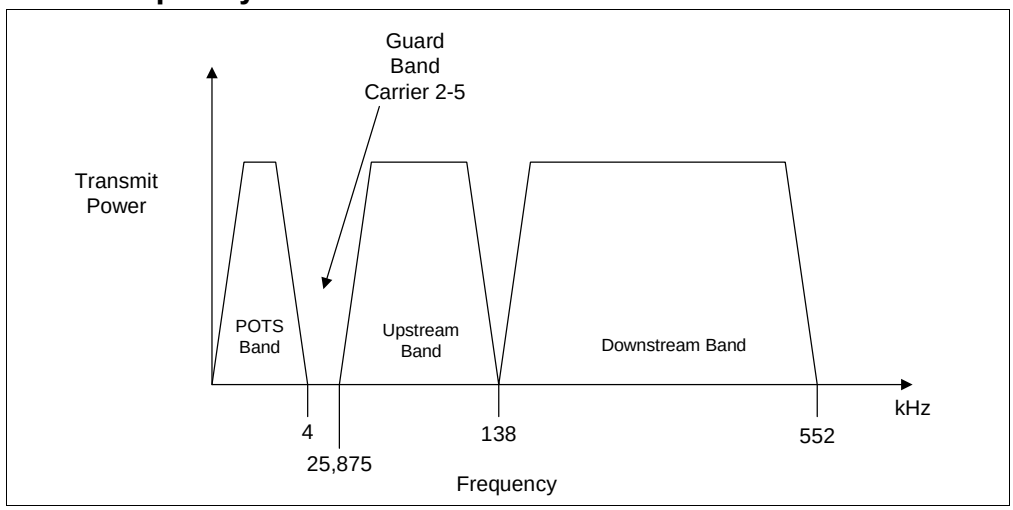
- DSP-based ITU-T G.992.2-compliant data pump for 4 channels
- Internal RAM eliminates need for external RAM and allows software upgradability
- 8/16-bit parallel µC interface with mailbox interface
- 8 bit Utopia-2 interface
- Built-in PLL; CLKO can be used to clock another ALiDD
- General-purpose I/O pins
- Power-down mode
- SMD P-TQFP-144-1 package
- Advanced low-power CMOS technology

ADSL.Lite, also called G.Lite, is a broadband transmission standard for the frequency range from 25 kHz (0 kHz optional) to 552 kHz. Because of the physical separation into two different frequency ranges for voice and data transmission the Frequency Division Multiplexing (FDM) allows concurrent voice and data transmission without the need for a splitter. Different frequency ranges are used for POTs band, and upstream and downstream bands. To ensure proper concurrent transmission of voice and data, a guard band is imposed between the POTs band and the upstream band.

G.Lite specifies DMT (Discrete Multitone Transmission) based on a Fast Fourier Transform (FFT) and a Inverse FFT to allocate the transmitted bits among many narrowband QAM-modulated tones. The number of bits depends on the transport capacity of each tone. Each of these narrowbands has a bandwidth of 4.3125 kHz.

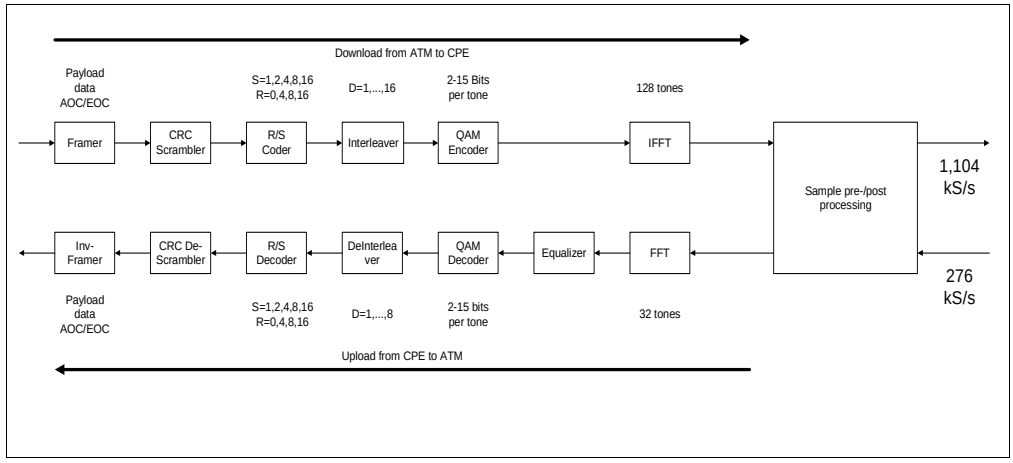
The different corner frequencies are shown in Figure 2-3.

Figure 2-3 Frequency Bands of FDM for G.Lite



The data processing of the upstream and downstream path is shown in Figure 2-4. For detailed information on data processing, refer to the Data Sheet for the ALiDD (**TBD**).

Figure 2-4 Simplified Block Diagram of Data Flow within ALiDD



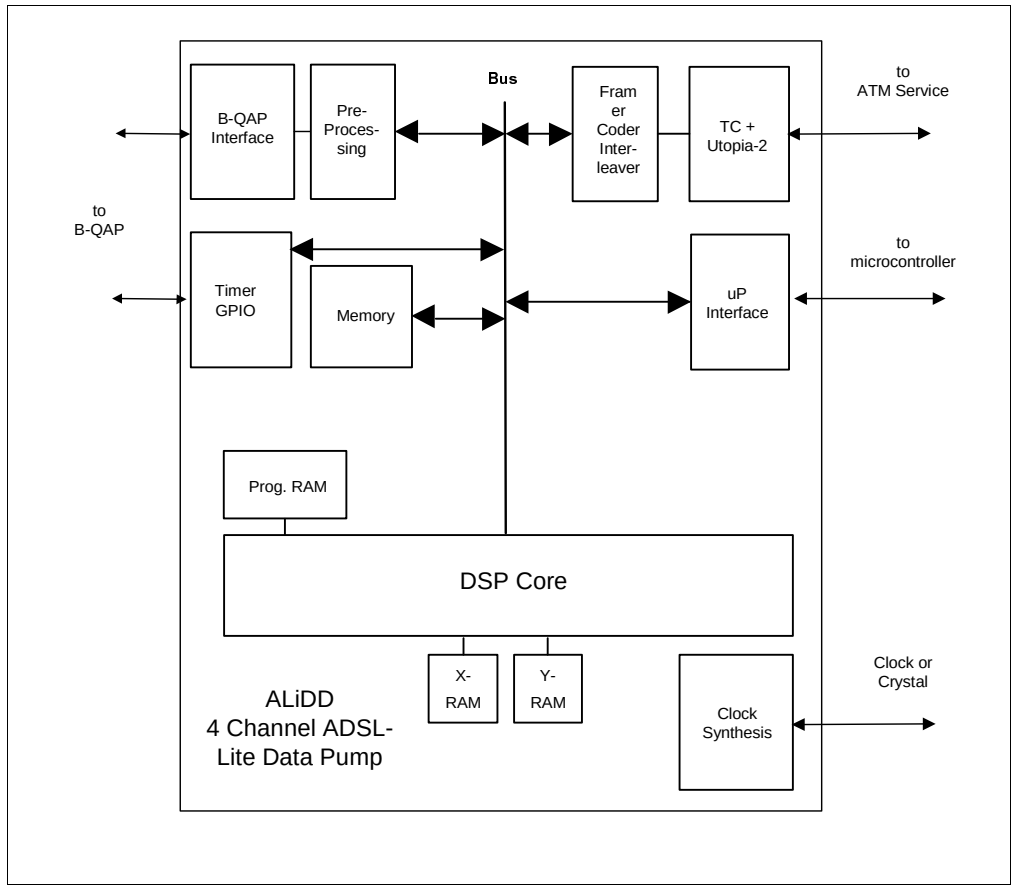


Figure 2-5 ALiDD Block Diagram

In downstream direction (CO to CPE), the ATM data stream received via the Utopia-2 interface is DMT-modulated and then transferred as a serial bitstream to the analog frontend B-QAP. The received serial bitstream from the B-QAP is demodulated and sent to the Utopia-2 interface as ATM cells.

Host Interface Mailbox Functions

To simplify communications across the host interface, the ALiDD has a mailbox for passing messages and control information between itself and the host. The mailbox consists of 512x16 bits in both read and write directions. Please refer to Section 4.5 ALiDD 8/16-bit Microcontroller Interface .

Clock Synthesis

The ALiDD has a flexible clock-synthesis circuit. Consequently, the ALiDD can be clocked internally at 4096 kHz, or with an external crystal. Also, the clock output is available to feed to other ALiDD chips, thereby eliminating the need for an external crystal for every other ALiDD on the board.

No External SRAM Required

The ALiDD has on-chip memory to support all internal processing of the ADSL-Lite channel. The ALiDD is fully software-upgradable.

General Purpose Input/Output

To facilitate system integration, the ALiDD has several programmable GPIO pins. These pins are accessed via the ALiDD parallel µC interface.

G.992.2 Compliance

The ALiDD complies with G.992.2, G.Lite.

2.4 B-MuPP

The B-MuPP performs the voice processing and controls the B-QAP. The programmable voice parameters can be controlled through the B-MuPP.

Features

- Digital chip optimized for control of a 8-channel POTS/G.Lite-based system
- Control of 2 B-QAP analog frontends (8 channels)
- Very small amount of glue logic required
- No trimming or adjustment required
- Specification according to ITU-T Q.552 Z interface, LSSGR, and DTAG recommendation
- 8-bit parallel microcontroller interface for Intel-, Motorola-like Processors
- Host interface running in multiplexed or demultiplexed mode
- Built-in PLL and clock generation
- PCM-encoded digital voice transmission (A-law, µ-law)
- IOM-2 or PCM highway for voice path
- Programmable digital filter for
  - Impedance matching
  - Transhybrid balancing
  - Frequency response
  - Gain
- Advanced test capabilities
  - Integrated line and circuit tests
  - 2 programmable tone generators
- Digital programmable DC characteristics
  - Programmable constant current from 0 to 50 mA
  - Programmable resistive values from 0 to 2 x 800 Ω
  - Programmable constant voltage
- Programmable integrated Teletax (TTX) injection and filtering during active mode in onhook and offhook states
  - Programmable up to 10 Vrms at tip-and-ring wire of the B-SLIC

  – Programmable frequency (12/16 kHz)
- Polarity reversal (either hard-coded or software-programmable)
- Integrated (balanced) ringing generation with zero crossing injection
  – Programmable frequency between 16.6 and 70 Hz
  – Programmable amplitude up to 85 Vrms at tip-and-ring of the B-SLIC
- Offhook detection with programmable thresholds for all operating modes
- Integrated ring trip detection with zero crossing turn-off function
- Ground start and loop start possible
- 4 GPIO pins
- 4 pins for linecard identification
- 3 operating modes: Power-down, active and ringing
- SMD P-MQFP-64 package
- Advanced low-power CMOS technology

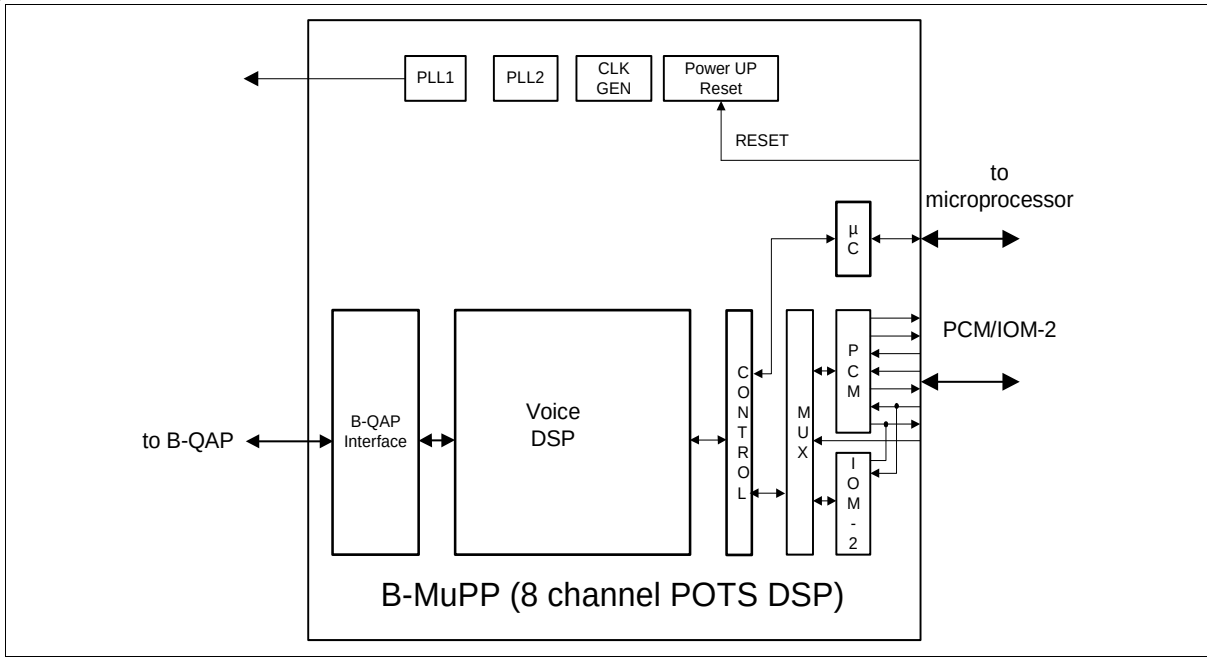


Figure 2-6 B-MuPP

2.5 Interfaces

The B-MuSLIC chipset has the following interfaces:

- 8-bit parallel µP interface for multiple processor types (B-MuPP)
- PCM/IOM2 interface B-MuPP
- 8/16-bit parallel µP interface for multiple processor types (ALiDD)
- Utopia-2 Interface (ALiDD)

The parallel µC interface can be set to Intel/Siemens multiplexed mode, Intel/Siemens demultiplexed mode, or Motorola demultiplexed mode. The chipset is programmed and controlled via this interface.

8-bit data traffic is moved through a Utopia-2 interface.

Voice data is moved through the PCM or IOM2 interface.

Please refer to **Chapter 4.3** for detailed information about the interfaces.

2.6 Programmable Voice-path Parameter

The B-MuSLIC forms a complete POTS interface via control loops for both the AC and DC paths. The transversal and longitudinal currents on the line are sensed in the B-SLIC and reported to the B-QAP. The current sense signal is converted to a voltage by an external resistor. A capacitor separates the transversal line current into DC and AC components.The AC and DC voltage signals are converted to digital in the B-QAP and sent to the B-MuPP for processing. The B-MuPP processes the AC and DC signals and sends them back to the B-QAP where they are converted to analog and sent to the B-SLIC. The B-SLIC then combines the AC and DC signals, amplifies them and drives them onto the subscriber line. Via this path the subscriber line current is sensed, processed and an appropriate voltage is then applied to the subscriber line. Since all of the processing is done in the digital domain, it is possible to change the electrical characteristics of the line by software.

2.6.1 BORSCHT Functions

Conventional linecard designs need a number of external components to adapt the circuit for use in different countries and applications. The B-MuSLIC chipset integrates the following programmable functions on-chip:

- DC (battery) feed characteristics
- AC impedance matching
- Transmit gain
- Receive gain
- Hybrid balance
- Frequency response in transmit and receive direction
- Ring frequency and amplitude
- Hook, ring-trip, and ground-key thresholds
- Test and diagnostic functions
- TTX/Pulse metering

One of the primary challenges of linecard development is to adapt the above-mentioned functions to country-specific requirements. Because these functions are software programmable, it is not necessary to change the linecard hardware to meet different country requirements or parameters. Because signal processing within the B-MuPP is

completely digital, it is possible to adapt to country-specific requirements by simply updating the coefficients that control the DSP that processes all the data. This means, for example, that changing impedance matching or hybrid balancing no longer requires hardware modifications. The digital nature of the filters and gain stages also assures high reliability, no drifts due to temperature or time, and minimal variability among different lines. Also, since each channel is processed independently, it is possible to configure different channels for different line characteristics.

Battery Feeding

An analog line circuit provides the voltage and current for subscriber equipment. In conventional line circuits, extra hardware is needed to adapt the battery feed characteristics to the requirements for different applications and countries. With the B-MuSLIC chipset, the battery-feed (DC) characteristics can be programmed in the B-MuPP itself and applied to the line via the B-SLIC.

Overvoltage Protection

Reliable overvoltage protection is provided by the robust 170 V SLIC technology together with a few inexpensive external parts such as varistors, resistors and thyristor diodes.

Ringing

The ringing signal is a low-frequency, high-voltage signal to the subscriber equipment. In conventional line circuits, the ringing voltage (40 to 85 Vrms) is generated in an external ringing generator and applied to the tip-and-ring lines by a relay. With the B-MuSLIC chipset, the ringing generator is integrated and no relay is needed (for balanced ringing only). The ringing signal is generated in the low-voltage B-MuPP and amplified in the high-voltage B-SLIC. The B-MuSLIC supports balanced and unbalanced ringing. With balanced ringing, the ringing voltage is applied differentially to the tip-and-ring lines. With unbalanced ringing, the ringing voltage is applied to either the tip or ring line against a potential that is near ground by an external ringing generator with relays.

Signaling (Supervision)

A linecard must detect onhook-to-offhook transitions in both non-ringing (hook switch detection) and ringing states (ring trip detection). With the B-MuSLIC chipset, the thresholds for offhook and ring trip detection can be programmed in the B-MuPP to suit different applications without changing external components.

Coding

The B-MuSLIC encodes an analog input signal to a digital PCM signal, and decodes a PCM signal to an analog signal. A-law, µ-law, and 16-bit linear coding is supported and is selected via software.

Hybrid for 2/4-wire Conversion

The subscriber equipment is connected to a 2-wire interface (tip-and-ring) where information is transmitted full-duplex. For digital transmission through the switching network, the information must be split into separate transmit and receive paths (4 wires). To avoid generating echoes, the hybrid function requires a balanced network matching the line impedance. Since the hybrid balance in the B-MuSLIC is performed in the digital domain, the hybrid balance can be changed without altering the external hardware.

Testing

Subscriber loops can have many kinds of faults. Access to the analog loop is necessary to perform the regular measurements involved in monitoring the local loop. Line-circuit functions must also be tested. In conventional line-circuit solutions, test units have to be switched to perform loop- and line-circuit tests. A remote testing unit and relays are normally necessary to perform a full range of tests. The only external component required by the B-MuSLIC chipset is 1 test relay to measure the reference voltage, all other functions are provided within the chipset, See “ITDF (Integrated Test and Diagnostic Functions) with the B-MuSLIC” on page 34 .

2.6.2 Additional Line Circuit Functions:

Teletax Metering

In many countries, pulse-metering TTX signals can be sent to the subscriber for billing purposes. A 12/16-kHz sinusoidal metering burst has to be transmitted. A 12/16-kHz notch filter is provided in the transmit path to prevent overloading the transmit A/D converter.

Polarity Reversal of Tip-and-ring

The B-MuSLIC also supports metering by polarity reversal by changing the polarity of the tip-and-ring lines. Polarity reversal is user-programmable to be either hard-coded or soft-coded.

Ground Start Mode

In applications using ground-start-loop signaling, the B-MuSLIC can be set in the ground-start mode. In this mode, the tip wire is switched to high-impedance mode. The

input voltage to the B-QAP is compared to a programmable threshold value in the B-MuPP.

2.6.3 DC Feeding Characteristics

Analog telephones are supplied with a DC current in the offhook state. AC speech signals in the receive and transmit directions are superimposed on this DC current.

Once the offhook state has been detected, the B-SLIC must supply a DC current to the subscriber line. The current is typically in the range of 14 to 40 mA, depending on local country specifications. Conventional linecard solutions require additional hardware to adjust the DC feed current to meet different country specifications. By comparison, DC feeding with the B-MuSLIC is fully programmable.

DC Characteristic

Transversal and longitudinal currents on the subscriber line are sensed by the B-SLIC and reported to the B-QAP. The currents are separated, digitized, and fed to the digital DC characteristic of the B-MuPP.

The B-MuSLIC DC-feed characteristic has 3 different zones: The constant-current zone, the resistive zone, and the constant-voltage zone. A programmable voltage reserve can be selected to avoid clipping the high AC signals (e.g. TTX).

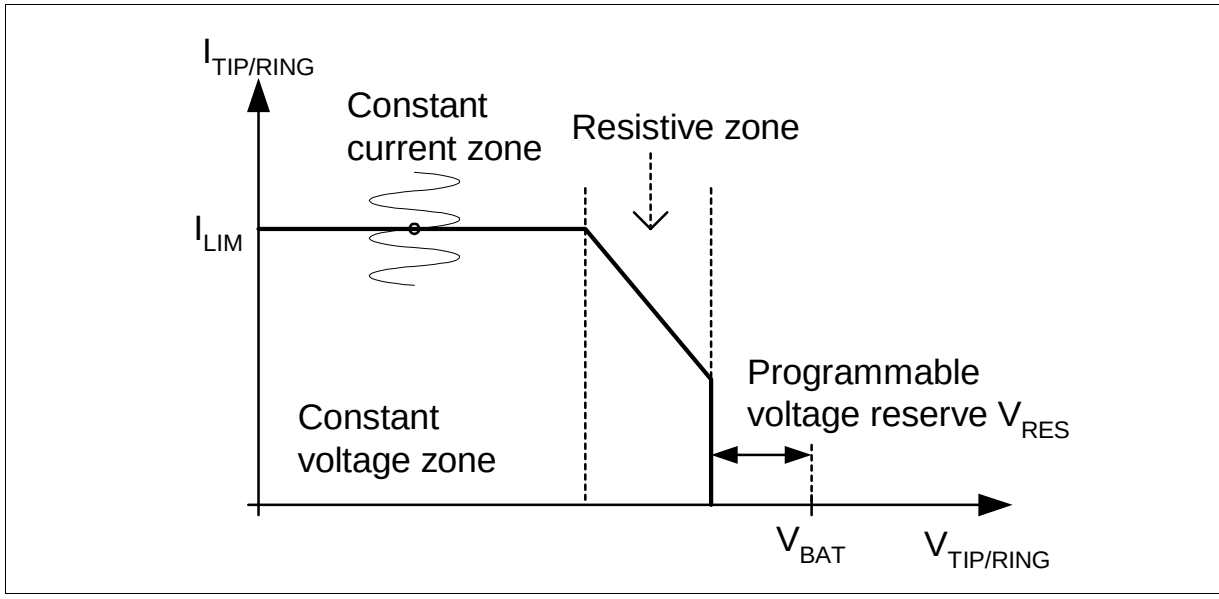


Figure 2-7 Simplified DC-feed Characteristic

Constant Current Zone

In the offhook state and under normal conditions, the feed current must be kept at a constant value, independent of load. B-SLIC measures the DC current, and supplies this

information to the B-QAP via the IT pin (input pin for DC control). The B-MuPP compares the actual current with the programmed value, and adjusts the B-SLIC drivers as necessary. $I_{TIP/RING}$ in the constant-current zone is programmable from 0 to 70 mA.

Resistive Zone

The resistive zone is used for very long lines where the battery voltage is incapable of feeding a constant current to the line. In the B-MuSLIC, the resistance is programmable from 0 to 1600 Ω.

Constant-voltage Zone

The constant-voltage zone is used in some applications to supply current through the line. In this case, $V_{TIP/RING}$ is constant and the current depends on the load between the tip-and-ring pins.

Boosted Battery Feed

If the battery voltage is not sufficient to supply the minimum required current through the line even in the resistive zone, an auxiliary positive battery voltage, in addition to the negative battery voltage V_{BAT}, is used to expand the voltage swing between tip-and-ring (boosted battery mode). With this increased voltage range (V_H to V_{BAT}), it is possible to supply the constant current through very long lines.

2.7 Power Dissipation

Power dissipation is a critical component of all system design. The B-MuSLIC is optimized to minimize power dissipation while keeping overall systems cost low through the IVD approach. Power dissipation in the B-MuSLIC chipset depends upon a number of system parameters such as V_{BAT}, loop length. and operating mode. (**Table 2-1**)

Table 2-1 Power Dissipation (mW) per channel of B-MuSLIC with 68 V Battery Voltage

Operating Mode	B-SLIC (V_{BAT} = 68 V)	B-QAP	B-MuPP	ALiDD	Total
Idle	10	60	15	50	135
Data & Voice	2517	300	25	300	3142
Data Only	2550	250	25	300	3125
Voice Only *	850 -2050	150	25	50	1075 - 2275

* Dependent on loop length

2.8 Programmable Parameters

Table 2-2 B-MuSLIC Programmable Parameters

Programmability	Range	Step size[1)]	Unit	Comments
DC-Indicators				
Hook Indication Active	0 - 50	1.50	mA	Hysteresis 2mA
Line Supervision	0 - 50	1.50	mA	Hysteresis 2mA
Ground Key Detection	0 - 50	1.50	mA	High/low current threshold
Ring trip detection	0 - 50	1.50	mA	
Hook indication power down	0 - 5	0.15	mA	
Ringing				
Ringing frequency	0 - 80	2.00	Hz	
Ringing offset	0 - 50	1.50	V	
Ringing amplitude: programmable range I programmable range II	 0 - 20 20 - 90	 2.00 1.00	 V_{RMS} V_{RMS}	
DC Characteristics				
Constant current range	0 - 50	0.70	mA	
Resistive range	0 - 1600	100.00	Ω	External protection excluded
Corner voltage: programmable range I programmable range II	 0 - 60 60 - 120	 1.50 3.00	 V V	
Constant voltage: programmable range I programmable range II	 0 - 60 60 - 120	 1.50 3.00	 V V	
Debouncing counter				
Hook indication	1.0 - 16.0	1.00	ms	The signal must be stable for the given period
Ground key detection	4.0 - 64.0	4.00	ms	
General IO pins	1.0 - 16.0	1.00	ms	

Table 2-2 B-MuSLIC Programmable Parameters (cont'd)

Programmability	Range	Step size[1)]	Unit	Comments
AC-Characteristics:				
Impedance matching filters				1 real pole 1 real zero 1st order WDF, 4th order FIR, Digital gain factor, Analog gain factor
Transhybrid filters				2 real poles 2 real zeroes, 2nd order WDF, 6th order FIR, Digital gain factor
Equalizers				4th order FIR
Absolute gain	-15 - +15 -30 - -15 +15 - +30	0.06 0.50 0.50	dB dB dB	
2 tone generators				
Frequency	200 - 2k	40.00	Hz	
Amplitude	-40 - 3.14	0.50	dB	
Metering signals:				
Frequency	12/16		kHz	
Amplitude	0.5 - 2.5	0.10	Vrms	

1) Worst case stepsize for respective programing range.

3 Operational Description

The operational description contains a brief overview of the operation of the B-MuSLIC chipset. The topics in this chapter are arranged as follows:

- 3 Operational Description
- 3.1 Active with Concurrent Data and Voice Transmission
- 3.2 Active-voice-only
- 3.3 Ringing
- 3.4 Power-saving Modes
- 3.5 Subscriber Loop Modes
- 3.6 Line Testing

The B-MuSLIC generates an internal reset at system power-up to begin initializing the chipset (Figure 3-1). The local controller then downloads setup values to the registers of the B-MuPP and the ALiDD, and places the B-MuSLIC into power-down mode. Power-down mode allows only essential loop monitoring activities in the B-SLIC to be operational. The local controller then proceeds to monitor the interrupt vectors of the B-MuSLIC for loop activity, and respond appropriately for the type of signal and application

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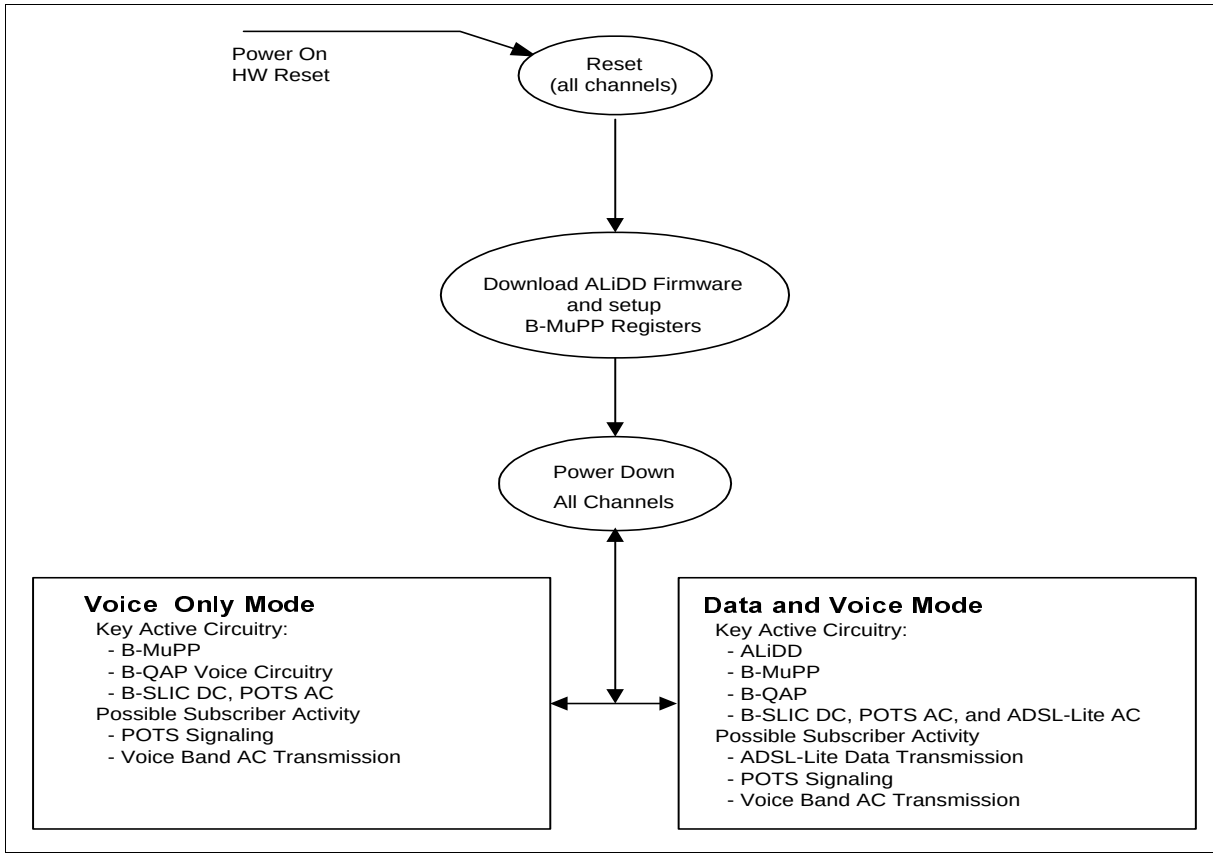

Figure 3-1 B-MuSLIC Simplified Mode Diagram

3.1 Active with Concurrent Data and Voice Transmission

While in the active data and voice mode, the B-MuSLIC chipset can simultaneously respond to all POTS signalling activity (ringing, hook status, etc.), send and receive voice band AC transmission, and operate a G.992.2-compliant ADSL-Lite modem.

Always-on

ALiDD supports the always-on state, meaning that there is no need to initiate a data connection manually whenever data traffic occurs. The G.Lite data connection will stay active. Different power modes (active, standby, power-down) can be used.

Fast-retrain

ALiDD supports the fast-retrain mode. Whenever line condition change (e.g., transition from onhook to offhook) for a longer period of time, the fast-retrain mode adapts the G.Lite data connection to the new conditions in order to achieve higher performance and higher data throughput.

3.2 Active-voice-only

The active-voice-only mode is designed for linecard operation where the subscriber is not supplied with an ADSL-Lite service. In this mode, the ALiDD and portions of the B-QAP are powered down, the only functional block is the voice path.

3.3 Ringing

Balanced Ringing

The ringing sine wave is generated in the B-MuPP. The frequency and amplitude are programmable between 16 and 70 Hz and up to 85 V_{RMS} at the tip-and-ring wires, respectively. The DC-offset voltage is programmable. When the ring-burst-on command is sent to the B-MuPP, the start (ring-burst-on) and end (ring-pause) of the ring burst is automatically synchronized at the zero voltage crossing. If the DC current at the IT pin exceeds the programmed value, offhook is detected within 2 periods of the ringing signal, and ring burst is switched off. When off-hook is detected, the B-MuSLIC remains in the ring-pause mode.

Unbalanced Ringing

The ringing voltage is generated by an external ring generator and connected to the tip-and-ring line with an external relay. The B-MuSLIC has integrated functionality to control the external ring relay with a zero voltage ring burst and ring trip signal.

3.4 Power-saving Modes

In either power-down mode, power consumption is minimized by disabling all non-required functions. The B-MuSLIC enters the power-down mode after a reset (including a Power On reset) or by programming. If power-down is initiated via software, each separate channel can operate in a different mode.

In power-down mode, the B-MuSLIC's IOM-2 or µC programming interface is ready to receive and transmit commands and data. The registers and coefficient RAM can be loaded and read in this mode. Received voice data on the PCM, IOM-2, or Utopia-2 interface will be ignored.

There are 2 power-down options:

- **PDNR (Power-DowN Resistive)**
  This power-down mode places 5 kΩ resistors from tip-and-ring to battery ground (B_{GND}) and the battery voltage (V_{BAT}), respectively. These resistors allow loop activity monitoring with minimal circuitry for POTS as well as remote modem requests.
- **PDNH (Power-DowN High-impedance)**
  This power-down mode provides a high impedance at tip-and-ring.

If the PDNR mode has been selected, line supervision remains active. Any change of line mode is reported via the hook bit in the IOM-2 data upstream channel or the B-MuPP µC SCR8 register. To avoid spurious offhook information caused by longitudinal induction, the hook bit is low-pass filtered.

An activate request from an ADSL-Lite modem issues an interrupt to the µC which has to start the activation of that specific ADSL channel.

3.5 Subscriber Loop Modes

Signaling in the subscriber loop is supervised internally by the B-MuSLIC chipset. Supervision is performed by sensing the longitudinal and transverse line currents on the tip-and-ring wires. The scaled values of these currents are generated in the B-SLIC, and fed to the B-QAP via the IT and IL pins.

Off-hook Detection

Loop-start signaling is the most common type of signaling. The subscriber loop is closed by the hook switch inside the subscriber's equipment.

In active mode, the transversal loop current is sensed by the internal current sensor in the B-SLIC. The IT pin of the B-SLIC indicates the loop current flow to the B-QAP. An external resistor converts the current information to a voltage on the IT pin.

The analog information is first converted to a digital value. It is then filtered and processed to suppress line disturbances. If the result exceeds a programmable threshold, an interrupt is generated to indicate off-hook detection.

A similar mechanism is used in power-down mode. In this mode, the internal current sensor is switched off to minimize power consumption. The loop current is therefore fed and sensed through 5 kΩ resistors. The information is made available at the IT pin and interpreted by the B-QAP.

Ring-trip Detection

A common method for ring-trip detection is to add a DC voltage to the ringing signal and sense the transversal DC loop current. The B-SLIC automatically applies a programmable DC offset to its internally-generated balanced ringing signal.

The DC voltage for ring-trip detection can be generated by the B-MuSLIC chipset and the internal ring-trip function, even if an external ringing generator is present.

Ground-start Mode

In applications using ground-start-loop signaling, the B-MuSLIC can be set in the ground-start mode. In this mode, the tip wire is switched to high-impedance mode. Ring-ground detection is performed by the internal current sensor in the B-SLIC, and transferred to the B-QAP via the IT pin. The input voltage to the B-QAP is compared to a programmable threshold value. After further processing (for example, deglitching the status information from tip-and-ring wire through the use of a programmable persistency counter), this information generates an interrupt, and offhook detection is indicated.

Table 3-1 B-MuSLIC Operating Modes

Mode	Sub-mode	SLIC supply voltages (+/-)	System functionality	Active circuits	Tip-and-ring voltage
Power-down	PDNH	Open / V_{BAT}	None	None	High impedance
	PDNR	Open / V_{BAT}	Off-hook detect	Off-hook, DC transmit path	0 / V_{BAT} (via 5 kΩ)
Active	ACT-V	0 / V_{BAT}	Voice and/or TTX transmission (no data)	Buffer, sensor, DC+ AC loop, TTX generator (opt.)	V_{BAT} / 2 [1]
	ACT-D	0 / V_{BAT}	data only or voice and data transmission	Buffer, sensor, DC+ AC loop, TTX generator (opt.)	V_{BAT} / 2
	BB	V_H / V_{BAT}	Voice and/or TTX transmission	Buffer, sensor, DC+ AC loop, TTX generator (opt.)	(V_H+V_{BAT}) / 2 [1]
	Ground Start	V_H / V_{BAT}	Voice and/or TTX transmission	Buffer, sensor, DC+ AC loop, TTX generator (opt.)	RING:(V_H+V_{BAT}) / 2 [1] TIP: High impedance
Ring	RING	V_H / V_{BAT}	Balanced ring signal feed (incl. DC offset)	Buffer, sensor, DC loop, ring generator	(V_H+V_{BAT}) / 2 [2]

Table 3-1 B-MuSLIC Operating Modes

Mode	Sub-mode	SLIC supply voltages (+/-)	System functionality	Active circuits	Tip-and-ring voltage
Special Modes	HIRT	V_H / V_{BAT}	e.g., Sensor offset calibration	Sensor, DC transmit path	High impedance
	HIR	V_H / V_{BAT}	e.g., Line test (TIP)	TIP buffer, sensor, DC transmit path	TIP: (V_H+V_{BAT}) / 2 [1)] RING: high impedance
	HIT	V_H / V_{BAT}	e.g., Line test (RING)	RING buffer, sensor, DC transmit path	RING:(V_H+V_{BAT}) / 2 [1)] TIP: high impedance

1) Plus diff. AC and DC signals via AC and DC interface

2) Plus diff. ring and DC signals via DC interface

3.6 Line Testing

3.6.1 Introduction

Subscriber loops are subject to many types of failure, and therefore have to be monitored. This requires easy access to the subscriber loop to perform regular measurements. Line testing involves measuring resistance, leakage, and capacitance, and measurements of foreign currents and voltages.

3.6.2 Traditional Line Testing

Conventional analog line cards in CO applications usually include 3 to 4 relays per channel. One relay is normally required to switch an external ring generator to the line, and some applications need an additional relay for polarity reversal. Two test relays are used to monitor the local loop (test-out relay) and to verify the line circuit itself (test-in relay).

The test-out relay switches an external test unit to the subscriber line (Figure 3-2). The external test unit measures capacitance, resistance, and leakage current, to detect any changes in the line condition or to detect any line failures.

The test in relay makes it possible to switch a test impedance to the SLIC, and thereby separate the subscriber line from the SLIC. With a test tone, it is possible to check the entire linecard loop from the codec through the SLIC.

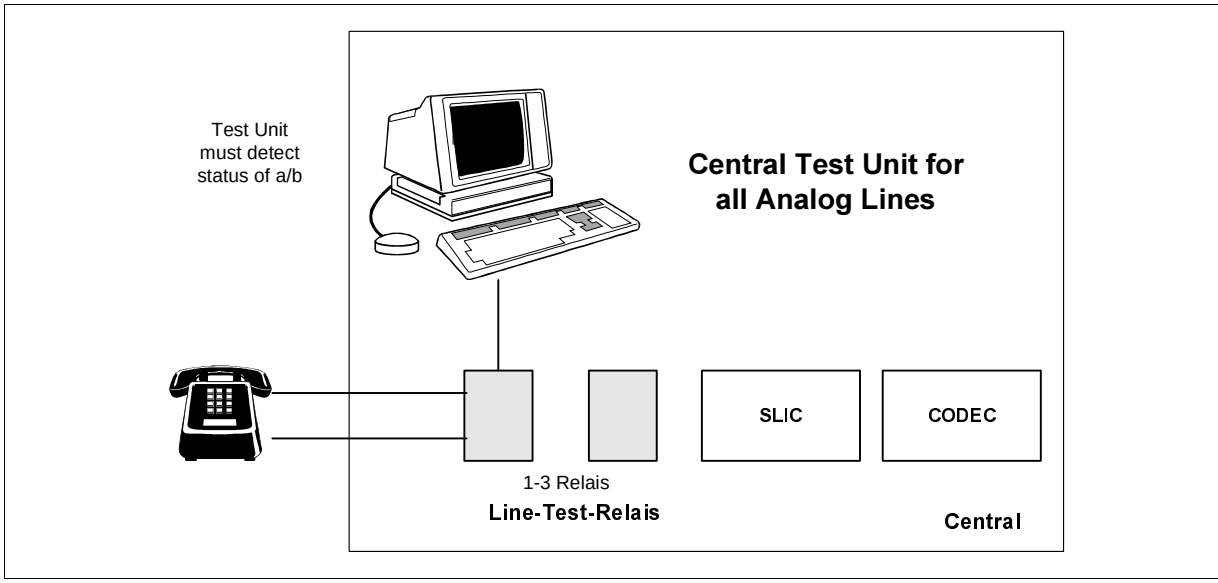

Figure 3-2 Traditional Line Testing

By offering integrated test features in silicon, the B-MuSLIC chipset has the capability to do all these tests without the need for an additional external test unit.

When testing lines with an external test unit, every line has to be connected separately to the test unit, and the tests have to be done line-by-line, which can take several hours for several thousand lines. Due to the long measurement time, these tests are typically done once per week or once per month. Therefore, any failures are usually detected very late. This drastically reduces the network quality for customers.

The absolute error in accuracy of all these line tests is typically 5%-10% or more because the line parameters (ε, μ, Z) are usually unknown and can only be roughly estimated.

3.6.3 ITDF (Integrated Test and Diagnostic Functions) with the B-MuSLIC

The B-MuSLIC offers a variety of unique and flexible test features called ITDF.

ITDF includes:

- Integrated subscriber-line testing
- Integrated codec self-diagnostics

ITDF reduces testing time, lowers manufacturing cost, accelerates the test flow in the field, and provides more flexibility for system manufacturers and their customers than conventional line testing does. All these features are provided **on silicon** without the need for any additional and expensive test equipment.

With the B-MuSLIC, usually only one relay is used for separating the line from the B-SLIC and for switching a test impedance to the B-SLIC. This test impedance can also be used for calibration. Two integrated tone generators can be used to send test tones to the reference impedance.

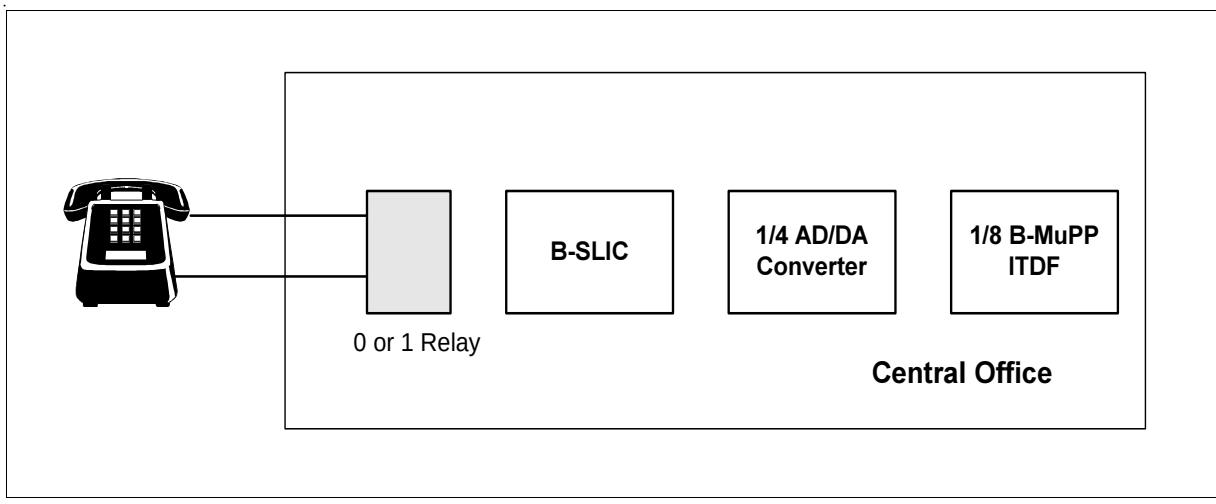

Figure 3-3 Line Testing with IDTF

Integrated Subscriber-line Testing

Integrated Line Testing functions make it possible to monitor the status of the subscriber loop remotely without any further test equipment. Compared to traditional testing, all

these tests can be done in parallel. This shortens the total test time for several thousand lines to several seconds. It is therefore possible to perform periodic tests on the subscriber loop, which means that the test time per line could be increased to several minutes, for example. Line failures can be detected much earlier, making the network much more reliable.

The B-MuSLIC has integrated test functions to measure the following line values:

– Subscriber-loop resistance, e.g., to localize short circuits (0 to 10 KΩ) (Figure 3-4)
– Isolation measurement with boosted battery to detect leakage currents on the line, and to monitor line quality (10 KΩ to 5 MΩ)
– Ringer capacitance
– Line capacitance (e.g., if the line breaks) (Figure 3-5)
– Foreign currents

The absolute error in accuracy is typically in the range of < 5 %, which is comparable to measurements with external test units.

There are 2 important on-chip integrated test functions that formerly required external devices. The first is the B-MuSLIC's integrated ramp generator for testing ringer capacitance. The second is the TTX signal generator, whose primary function is to generate high frequency (up to 16 kHz) metering pulses for billing purposes. It can also be used to measure the onboard capacitance when the subscriber line is disconnected.

Basic Measurement Principle

Line testing with the B-MuSLIC is based on a voltage-feeding, current-sensing principle (Figure 3-4). An incoming PCM word is converted to a voltage on the tip-and-ring line. The load on the line affects the current flowing into it. This current is sensed via the B-SLIC, and relevant information is fed to the codec where it is transferred as a PCM-out-word to the PCM highway. The DC-feed characteristic is switched off in the line-test mode.

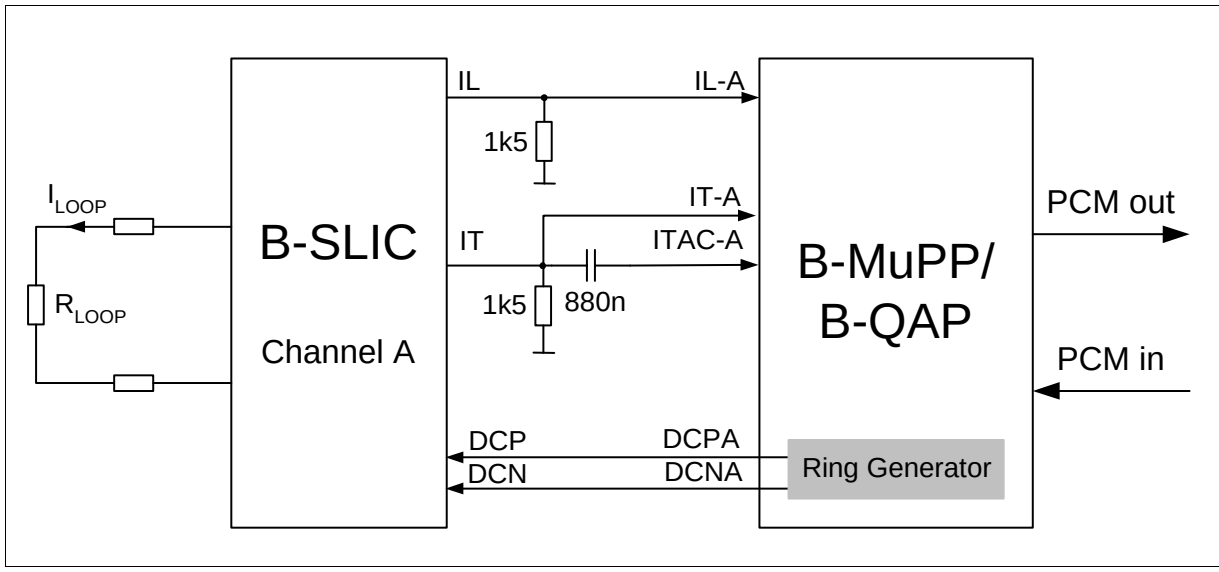

Figure 3-4 Resistance Measurement

The same principle is also used for capacitance measurements (Figure 3-5). The only difference is that for feeding the tip-and-ring line, no PCM-in-word is required, but the internal ramp generator can be used for producing a time-varying trapezoidal signal for capacitance measurements.

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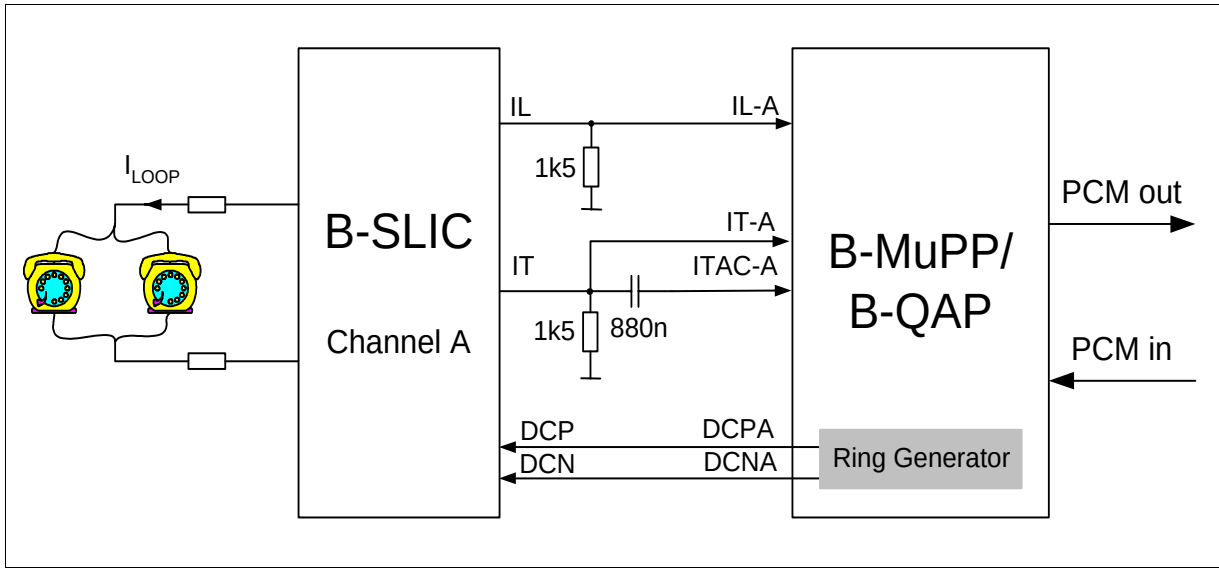


Figure 3-5 Capacitance Measurement

The current on the tip-and-ring line is proportional to the derivative of the feed voltage. The capacitance can be calculated directly by measuring the peak current and the programmed feed voltage (Figure 3-6):

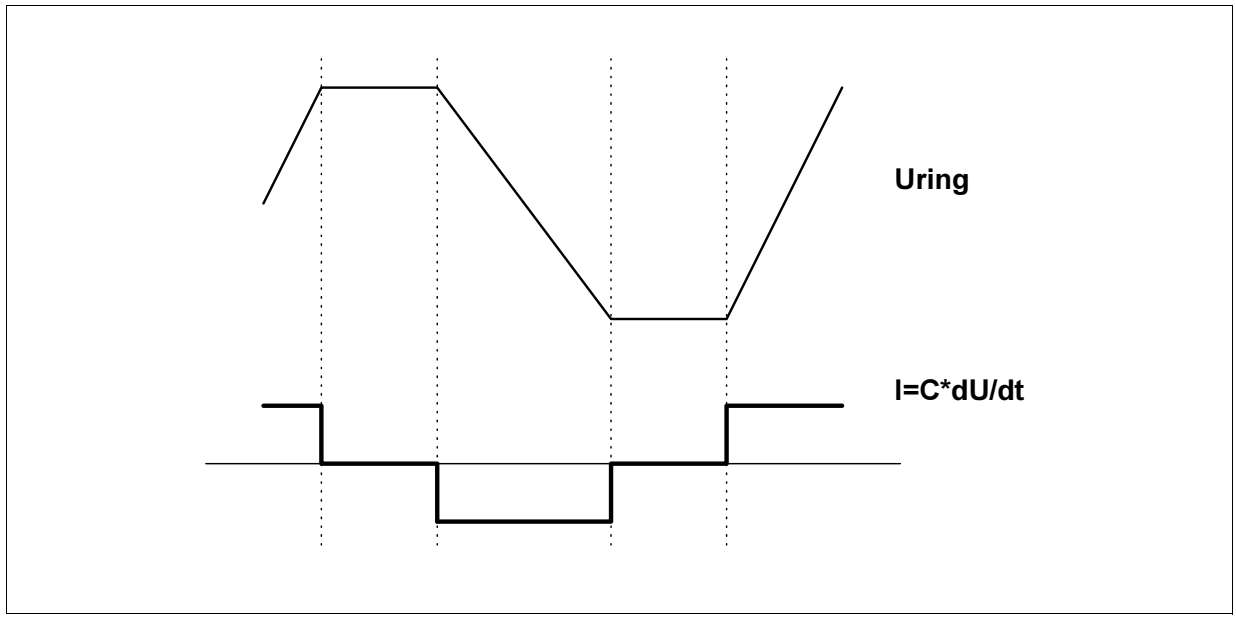


Figure 3-6 Capacitance Calculation

Integrated codec Self-diagnosis

The integrated codec self-diagnostic features can be used to perform a functional inspection of a complete analog linecard at the end of the manufacturing process. This method has 2 important benefits. Test time is drastically reduced, and no additional, expensive test equipment is required except for 1 reference resistor with relays. The external resistor and relay serve as an external reference.

The B-MuSLIC has integrated test functions to measure the following codec values:

- Various analog and digital loops to test the analog and digital interfaces of the linecard
- Digital loop to test interface to codec (e.g. backplane)
- Digital loop for codec self-diagnosis
- Various analog loops to test the codec in production
- Level-metering to test ring voltage, metering pulses, voice levels, and noise (S/N).
- Automatic internal ALiDD diagnostics and self-test.

4 Interfaces

The B-MuSLIC chip set has several interfaces. The B-MuPP is controlled through either an IOM-2 interface, or a parallel µC interface. Voice data is sent to/from the B-MuPP in the IOM-2 structure or though a PCM interface. The ALiDD is also controlled with a parallel µC interface, and data is sent though a Utopia-2 interface with 8-bit data.

The topics in this chapter are arranged as follows:

- 4.1 PCM Interface
- 4.2 IOM-2 Interface
- 4.3 Utopia-2 Interface
- 4.4 B-MuPP 8-bit Microcontroller Interface
- 4.5 ALiDD 8/16-bit Microcontroller Interface
- 4.6 Tip-and-ring Interface

4.1 PCM Interface

Two serial PCM highways are used to transfer voice data. A PCM interface consists of 8 pins:

PCLK:	PCM CLocK, 512 kHz to 8192 kHz
FSC:	Frame Synchronization Clock, 8 kHz
DRA:	Receive Data input for PCM highway A
DRB:	Receive Data input for PCM highway B
DXA:	Transmit Data output for PCM highway A
DXB:	Transmit Data output for PCM highway B
TCA:	Transmit Control output for PCM highway A, active low during transmission
TCB:	Transmit Control output for PCM highway B, active low during transmission

The Frame-Sync Clock (FSC) pulse identifies the beginning of a receive and transmit frame for all 8 channels. The PCLK synchronizes data transfer on both lines DXA (DXB) and DRA (DRB) to the PCM highways. Bytes in all channels are serialized to 8-bit width with the MSB first.

The data rate of the interface can vary from 2*512 kb/s to 2*8192 kb/s (two highways). **Table 4-1** shows sample frequencies for the PCM interface.

Table 4-1 B-MuSLIC PCM Interface Configuration

	Frequency [kHz]	Single/Double [1/2]	Time Slots [per highway]	Data Rate [kbit/s per highway]
	512	1	8	512
	1024	2	8	512
	1024	1	16	1024
	2048	2	16	1024
	2048	1	32	2048
	4096	2	32	2048
	4096	1	64	4096
	8192	2	64	4096
	8192	1	128	8192

4.2 IOM-2 Interface

The IOM-2 interface consists of 2 data lines and 2 clock lines. Data Upstream (DU) carries data from the B-MuSLIC to a master device. Data Downstream (DD) carries data from the master device to the B-MuSLIC. An 8-kHz FSC signal and a 4096-kHz Data CLock (DCL) signal have to be supplied to the B-MuSLIC. The B-MuSLIC handles data as described in the IOM-2[1)] specification for analog devices.

4.3 Utopia-2 Interface

The ALiDD supports a complete 8-bit Utopia-2 interface as defined by ATM Forum document UTOPIA Level 2, Version 1.0. The table below describes the pins used to implement the Utopia-2 interface on the ALiDD. The Utopia-2 interface allows up to 31 physical layer devices on a single interface. Using a proprietary in-band signaling protocol, Infineon has added a feature to the standard Utopia-2 interface. This feature allows connections for up to 124 physical layer devices.

U_RxData [1:8]: Utopia Data Receive

U_TxData [1:8]: Utopia Data Transmit

U_RxADDR [1:5]: Utopia ADDRess Receive

U_TxADDR [1:5]: Utopia ADDRess Transmit

1) Available on request from your local Infineon office

U_RxCLAV [0:3]:	Receive Interface CelL AVailable
U_TxCLAV[0:3]:	Transmit Interface CelL AVailable
U_RxENB:	Receive ENaBle
U_TxENB:	Transmit ENaBle
U_RxSOC	Receive interface Start Of Cell indication
U_TxSOC	Transmit interface Start Of Cell indication
U_RxCLK	Receive interface Utopia CLocK
U_TxCLK	Transmit interface Utopia CLocK
rx_data	receive data within serial bypass mode (ATU to TC Logic Interface according to G.992.2, if no ATM is used as high-layer protocol)
sbp_clk	serial bypass clock

4.4 B-MuPP 8-bit Microcontroller Interface

This parallel µC interface is used to communicate with external master devices such as linecard controllers. The B-MuPP µC interface consists of 6 control lines (ALE/DS, CS, RD/RW, WR, DEMUX/MUX, INT/MOT), 8 bidirectional address/data lines (DIO0 to DIO7), and 8 address lines (A0 to A7). The interface provides fast parallel data transfer to a µC (Intel- and Motorola-compatible). It supports a multiplexed/non-multiplexed 8-bit address/data bus, and connects to µCs of the Intel 8051-(MCS51/251-), Siemens C16X and Motorola M68HCXX or M683XX families.

The following interface specifications can be selected using pin strapping:

- Intel multiplexed mode
- Intel demultiplexed mode
- Motorola mode

Table 1 Address Layout of the µC-Interfaces (PCM-Mode)

Address	Command	Function
00000000, 00_H	Channel	Preselect channel for channel-specific commands BSOP, SOP, TOP, COPI
00000001, 01_H	Status	Status register to control the read/ write operations
00000010, 02_H	Interrupt Register (Read Only)	Indicates channel and sources of pending interrupts
00000011, 03_H	Reset	Reset the µC interface by writing $0AA_H$ data to this address

Table 1 Address Layout of the µC-Interfaces (PCM-Mode)

00000100, 04_H	Reserved	
00000101, 05_H	Interrupt Channel register 1	Indicate pending interrupts on channels 0 to 7
00000110, 06_H	Reserved	
00000111, 07_H	Data	Data port for all register read/write operations

4.5 ALiDD 8/16-bit Microcontroller Interface

The parallel interface of the ALiDD is similar to the one in the B-MuPP (Section 4.4), but also offers a mode with a 16-bit-wide data bus (DIO0 to DIO15). After power-up, the ALiDD µC interface is in 8-bit mode and can be configured to 16-bit mode via a control register.

The communication between ALiDD and the µC uses a mailbox interface with 2 mailboxes (send and receive), each 512x16 bits (**Table 4-2**).

Table 4-2 Registers in ALiDD Mailbox for Host Access

Address	Command/Function
00000000, 00_H	read: Mailbox input data from ALiDD write: Mailbox output data to ALiDD
00000001, 01_H	write: Mailbox address for write to ALiDD[9:2]
00000010, 02_H	write: Mailbox address for write to ALiDD[1:0]
00000011, 03_H	write: Mailbox address for read from ALiDD[9:2]
00000100, 04_H	write: Mailbox address for read from ALiDD[1:0]
00000101, 05_H	read: Host interrupt acknowledged by ALiDD write: Host status to ALiDD
00000110, 06_H	read: ALiDD status register
00000111, 07_H	read/write: Configuration register

For communication from µC to ALiDD, e.g., a write operation, a byte or word of data has to be written to the data register. Then the address has to be written to the write address register. If additional data has to be sent, the address register is incremented automatically so that only further data writes are necessary. A read operation is performed similarly, but uses different registers. The configuration register makes it possible to configure PLL, 8/16-bit host interface, and reset.

The ALIDD provides three types of µP buses that are selected via pin ALE.T

Table 4-3 Host Interface Operating Modes

	Multiplexed A/D	Demultiplexed A/D
8 bit	Addr: AD(0:7) Data: AD(0:7)	Addr: A(0:7) Data: AD(0:7)
16 bit	Addr: AD(0:7) Data: AD(0:15)	Addr: A(0:7) Data: AD(0:7

4.5.1 Host Interface Signals

Table 4-4 Host Interface Signals

Symbol	Input (I) Output (O)	Function
AD(0:7)/ (0:15) D(0:15)	I/O	**Address/Data Bus (multiplexed mode)** Transfers addresses and data between the host and the ALIDD. **Data Bus (non-multiplexed mode)** Transfers data between the host and the ALIDD.
A(0:7)	I	**Address Bus (non-multiplexed mode)** Input address to the ALIDD registers.
RD DS	I	**Read (Siemens/Intel bus mode)** This signal indicates a read operation. **Data Strobe (Motorola bus mode)** The rising edge marks the end of a valid read or write operation.
WR R/W	I	**Write (Siemens/Intel bus mode)** This signal indicates a write operation. **Read/Write (Motorola bus mode)** A "1" identifies a valid host access as a read operation and a "0" identifies it as a write operation.
CS	I	**Chip Select** A "0" on this line selects the ALIDD for a read/write operation.

Table 4-4 Host Interface Signals

Symbol	Input (I) Output (O)	Function
ALE	I	**Address Latch Enable** A “1” on this line indicates an address on AD (0:7), that is latched by the ALIDD (multiplexed mode only). ALE also selects the interface mode (multiplexed or non-multiplexed).
INT	O (OD)	**Interrupt Request** This is the interrupt output line to the host for all mailbox interrupt status requests. It is an open drain output.

4.6 Tip-and-ring Interface

The tip-and-ring interface connects the subscriber line to the B- MuSLIC. The interface meets the ITU-T recommendation Q.552 for a Z-interface.

5 Application Circuit and Tools

The topics in this chapter are:

- 5.1 Typical Application Circuit (Figure 5-1)
- 5.2 Support Tools

5.1 Typical Application Circuit

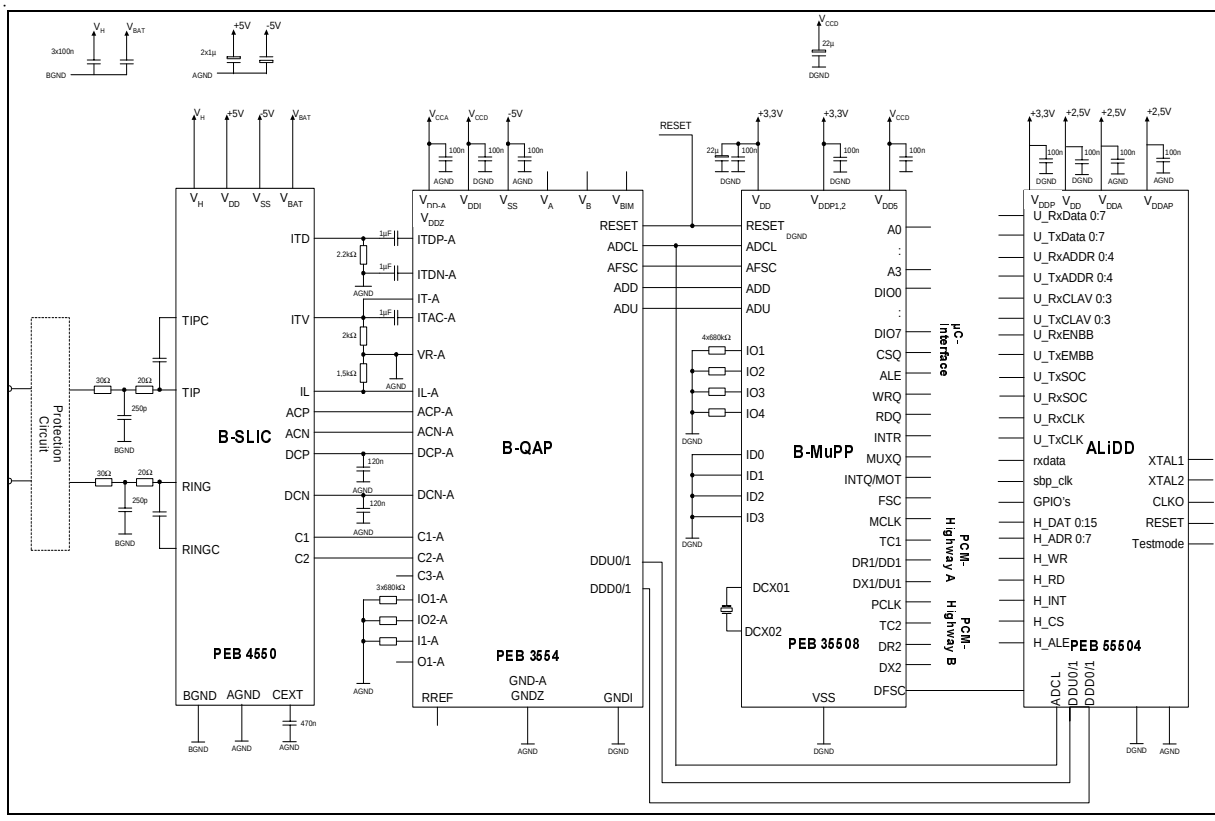


Figure 5-1 Application Circuit

5.2 Support Tools

- B-MuSLICOS Coefficient Calculating Software
- SMART35508 B-MuSLIC Evaluation Board
- SMART55504 ALiDD Evaluation Board

5.2.1 B-MuSLICOS Coefficient Calculating Software

The B-MuSLICOS Coefficient Calculating Software is a project-oriented, Windows-compatible program. It is designed to assist the user in developing sets of DSP filter coefficients for different country and PTT requirements. The on-line help and structured program flow guide the user through the coefficient calculation process.

B-MuSLICOS calculates coefficients for the following filters.

- AC Filters
  - Impedance matching to adapt the system to the required line impedance of the local loop (return-loss calculation)
  - Frequency response correction for both receive and transmit paths
  - Level adjustment for both receive and transmit paths
  - Transhybrid balancing
  - 2 programmable tone generators.
- DC Filters
  - DC-Feed characteristic (battery-feed characteristic values such as constant current, resistive range, and constant range)
  - Ringing signal
  - Level metering
  - TTX signals
  - Threshold calculation for offhook and onhook.

After defining the required inputs for B-MuSLICOS, the user can start calculating the filter coefficients. All calculation results are stored in the result file, which can be displayed by the B-MuSLICOS program. Some of the calculations are also displayed graphically to enable the product designer to verify the required behavior quickly, and make any additional optimizations manually. The following calculations are displayed graphically:

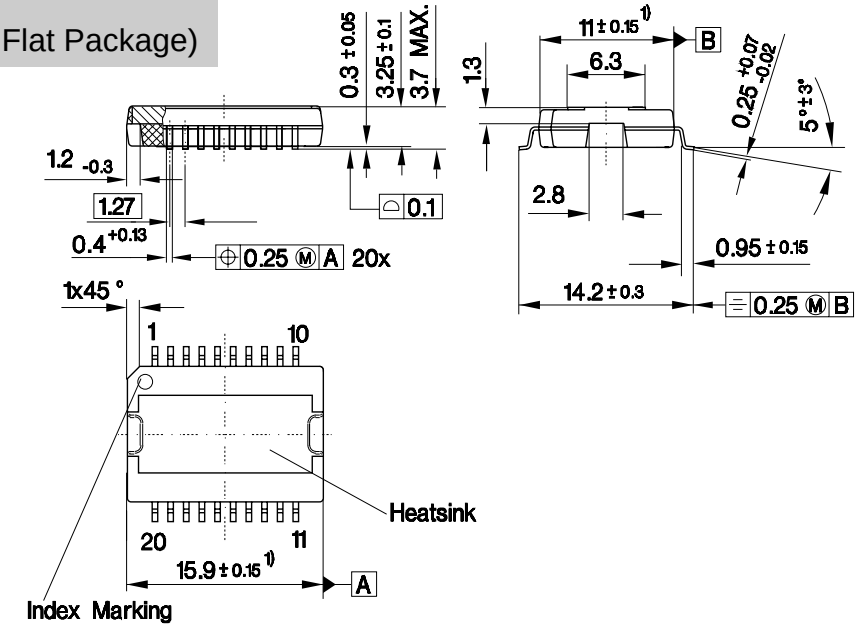
- Return loss
- Input impedance
- Frequency responses in the receive and transmit paths
- Transhybrid loss
- DC characteristic

5.2.2 SMART 35508 and SMART 55504 Tool Packages

The SMART 35508 and SMART 55504 tool packages include an evaluation board and intuitive Windows-based software enabling simple configuration and programming of the B-MuSLIC data and voice functions. Each evaluation tool gives complete access to all data and voice interfaces, facilitating complete system performance measurements. Either evaluation system can be connected to test equipment in order to measure the transfer characteristics and to fine-tune system performance.

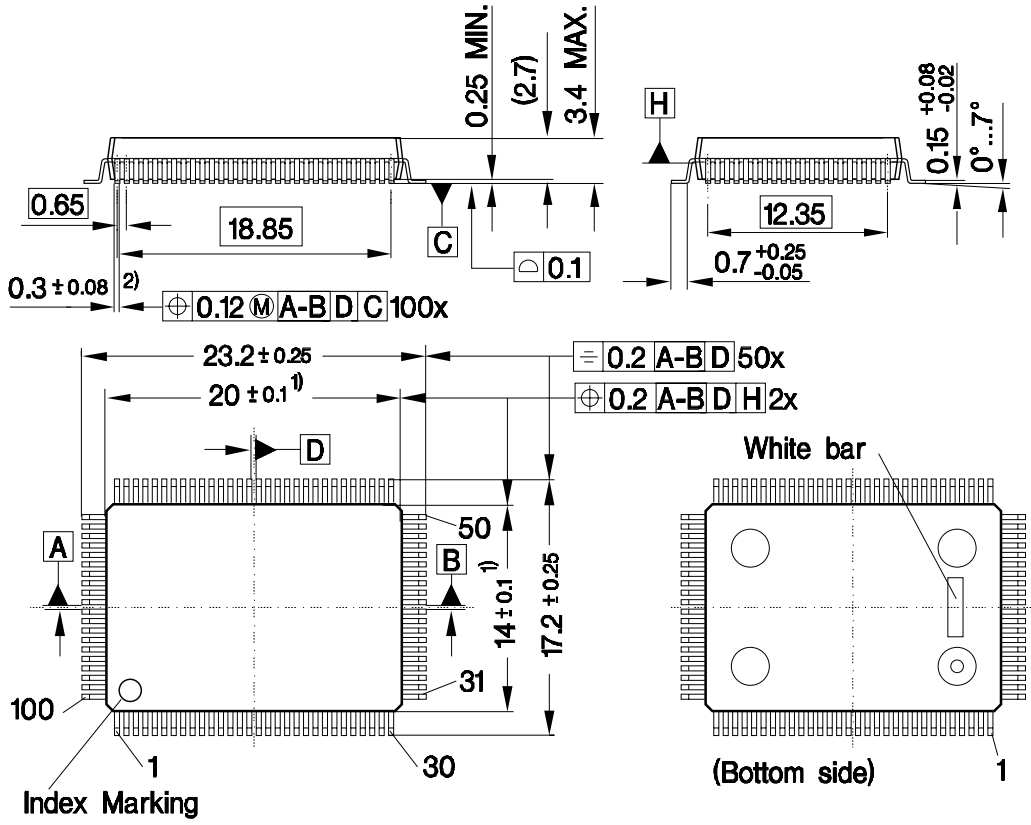
6 Package Outlines

P-DSO 20-5
(Plastic Metric Quad Flat Package)



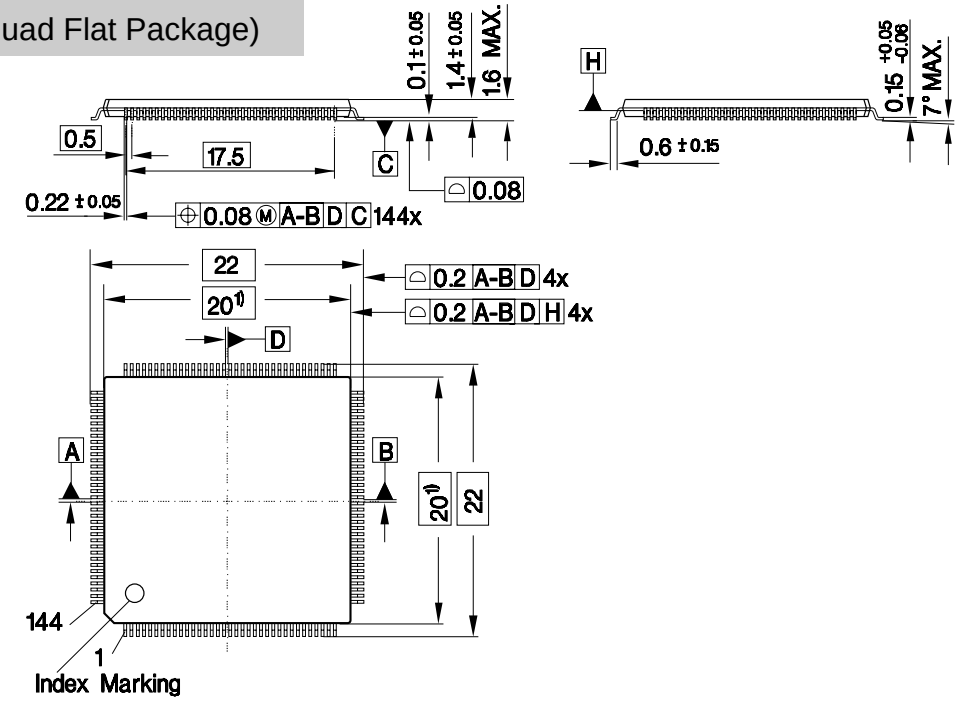
1) Does not include plastic or metal protrusion of 0.15 max. per side

P-MQFP-100-2
(Plastic Metric Quad Flat Package)



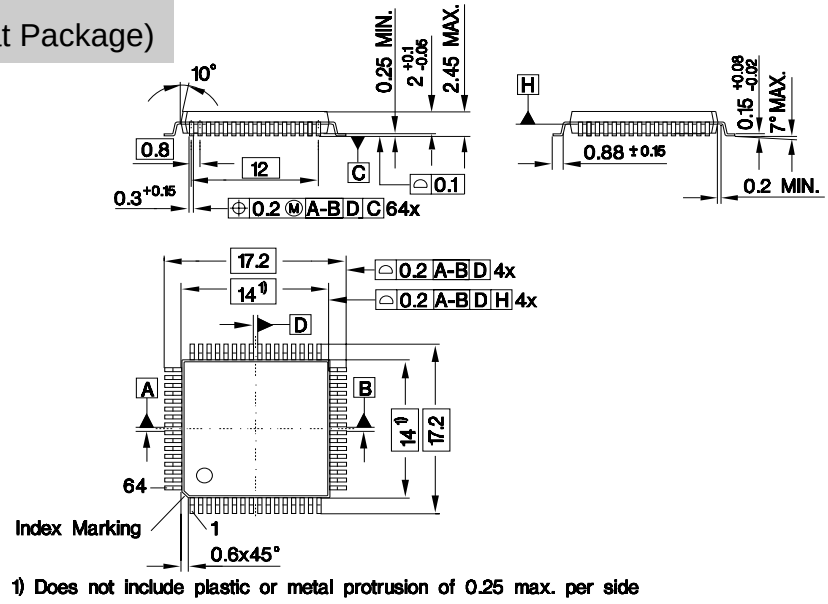
2) Does not include dambar protrusion of 0.08 max. per side
1) Does not include plastic or metal protrusion of 0.25 max. per side

P-TQFP-144
(Plastic Thin Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

P-MQFP-64-1
(Plastic Metric Quad Flat Package)



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

Packaging
Package outlines for tubes, trays etc. are described in our Data Book “Package Information”.

SMD = Surface-Mounted Device

Dimensions in mm

Abbreviations and Acronyms

AHV-SLIC	Advanced High-Voltage SLIC
BB	Boosted Battery
BORSCHT	Battery feeding, Overvoltage protection, Ringing, Signaling (Supervision), Coding, Hybrid for 2/4-wire conversion, Testing
CO	Central Office
COP	Coefficient Operation Command
COPI	Coefficient Operation Initialize
DCL	Data Clock Signal
DD	Data Downstream
DRA (B)	Receive Data input for PCM highway A (B)
DSP	Digital Signal Processor
DTAG	Deutsche Telecom AG
DTMF	Dual Tone Multi Frequency
DU	Data Upstream
DXA (B)	Transmit Data for PCM highway A (B)
FSC	Frame Synchronization Clock
IOM	ISDN-Oriented Module
IOM CI	IOM Control Interface
ITDF	Integrated Test and Diagnostic Functions
LSSGR	Local area transport access Switching System Generic Requirements
µC	MicroController
MSB	Most Significant Bit
B-MuPP	Broadband Multichannel Processor for POTS
B-MuSLIC	Broadband Multichannel signal-processing Subscriber-Line Interface Circuit
PBX	Private Branch Exchange
PCLK	PCM CLocK
PCM	Pulse Code Modulation
POTS	Plain Old Telephone System
PSTN	Public Switched Telephone Network

B-QAP	Broadband Quad Analog frontend Processor
B-SLIC	Broadband Subscriber Line Interface Circuit
SMD	Surface-Mounted Device
SOP	Status OPeration
TCA (B)	Transmit Control output for PCM highway A (B)
TG	Tone Generator
TOP	Transfer OPeration
TTX	TeleTaX