

SN54ABT646A, SN74ABT646A OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS0069E – JULY 1991 – REVISED JULY 1994

- State-of-the-Art **EPIC-II[®]** BICMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Drive Outputs (–32-mA I_{OH} , 64-mA I_{OL})
- Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages, Ceramic Chip Carriers (FK), and Plastic (NT) and Ceramic (JT) DIPs

description

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'ABT646A.

Output-enable ($\overline{OE}$) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The direction control (DIR) determines which bus will receive data when $\overline{OE}$ is low. In the isolation mode ($\overline{OE}$ high), A data may be stored in one register and/or B data may be stored in the other register.

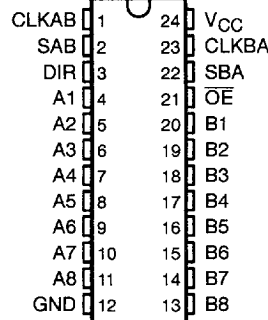
When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

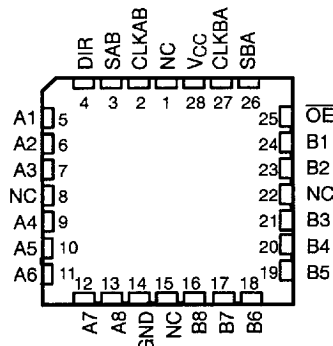
The SN74ABT646A is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT646A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT646A is characterized for operation from -40°C to 85°C .

SN54ABT646A ... JT PACKAGE
SN74ABT646A ... DB, DW, OR NT PACKAGE
(TOP VIEW)



SN54ABT646A ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

EPIC-II[®] is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA Information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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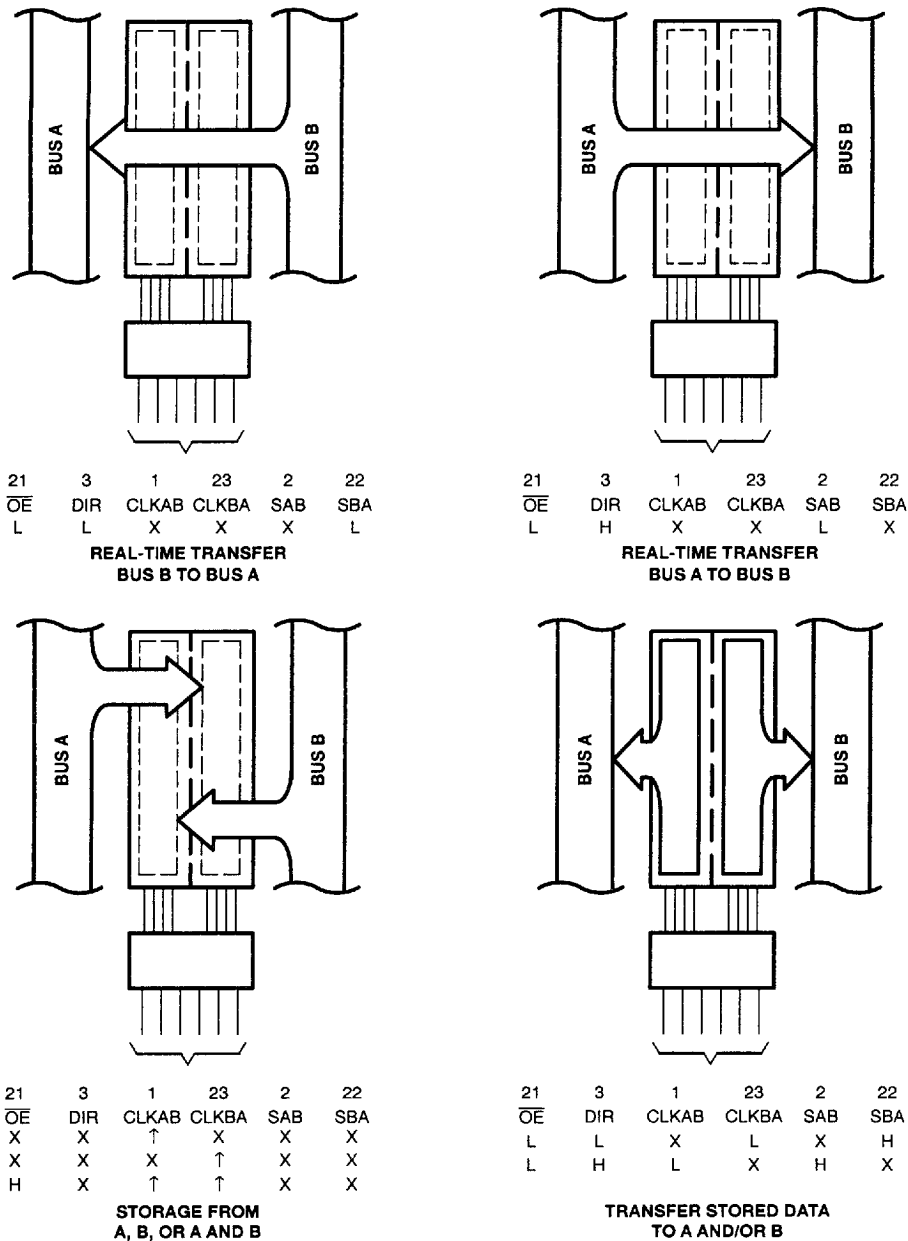


Figure 1. Bus-Management Functions

Pin numbers shown are for the DB, DW, JT, and NT packages.



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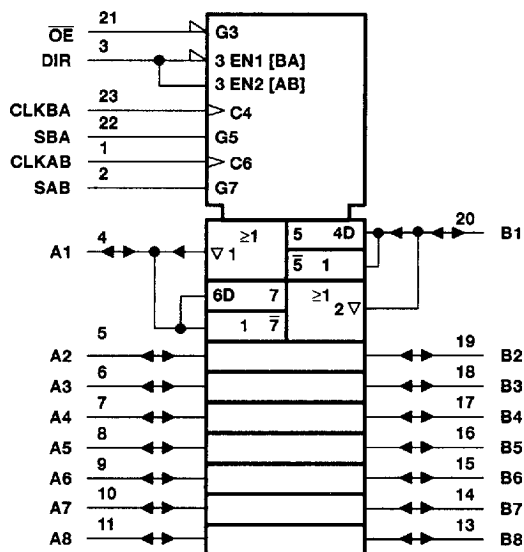
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FUNCTION TABLE

INPUTS						DATA I/Os		OPERATION OR FUNCTION
OE	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

† The data output functions may be enabled or disabled by various signals at the OE and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DB, DW, JT, and NT packages.

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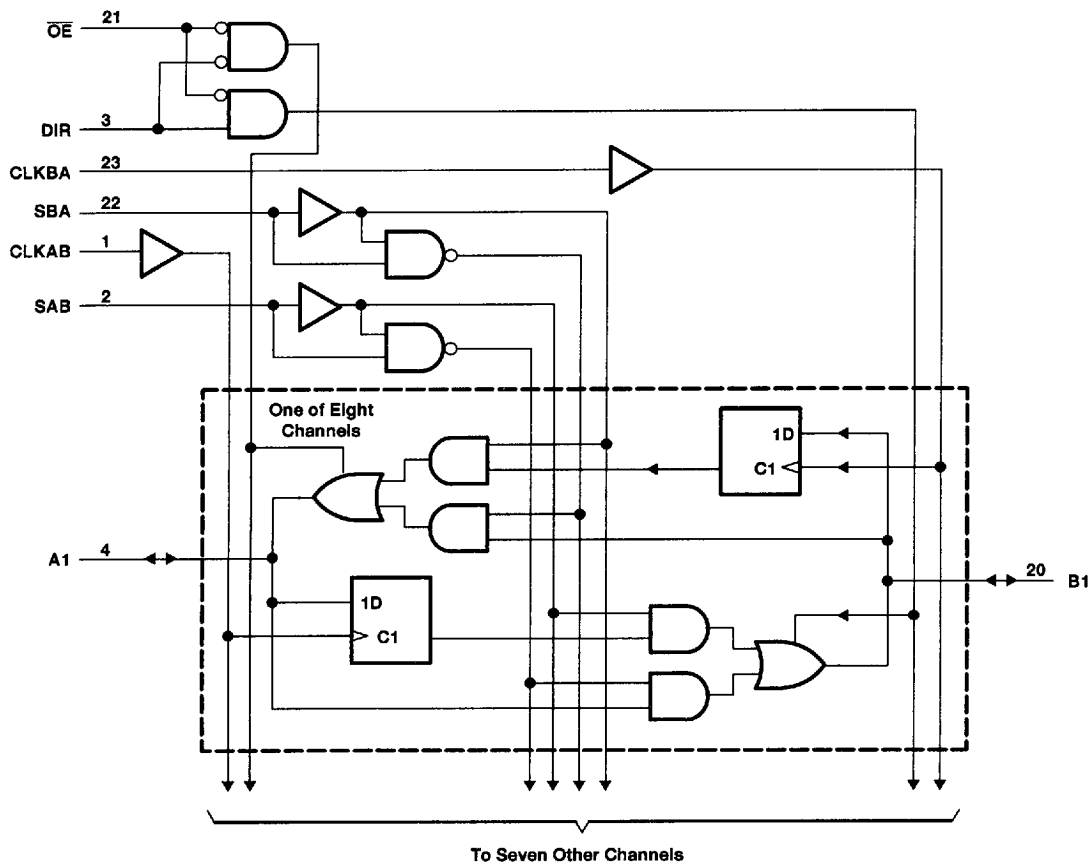
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SN54ABT646A, SN74ABT646A OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, and NT packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O	-0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT646A	96 mA
SN74ABT646A	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	-18 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DB package	0.65 W
DW package	1.7 W
NT package	1.3 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the NT package, which has a trace length of zero. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 3)

		SN54ABT646A		SN74ABT646A		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		-24		-32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		5		5	ns/V
T_A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.



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SN54ABT646A, SN74ABT646A

OCTAL BUS TRANSCEIVERS AND REGISTERS

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T _A = 25°C			SN54ABT646A		SN74ABT646A		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA				-1.2		-1.2		-1.2	V
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -3 mA		2.5			2.5		2.5		V
	V _{CC} = 5 V, I _{OH} = -3 mA		3			3		3		
	V _{CC} = 4.5 V	I _{OH} = -24 mA	2			2				
		I _{OH} = -32 mA	2*					2		
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 48 mA			0.55		0.55			V
		I _{OL} = 64 mA			0.55*				0.55	
I _I	V _{CC} = 5.5 V, V _I = V _{CC} or GND	Control inputs			±1		±1		±1	μA
		A or B ports			±100		±100		±100	
I _{OZH} ‡	V _{CC} = 5.5 V, V _O = 2.7 V				10§		50§		10§	μA
I _{OZL} ‡	V _{CC} = 5.5 V, V _O = 0.5 V				-10§		-50§		-10§	μA
I _{off}	V _{CC} = 0, V _I or V _O ≤ 4.5 V				±100				±100	μA
I _{CEX}	V _{CC} = 5.5 V, V _O = 5.5 V	Outputs high			50		50		50	μA
I _O ¶	V _{CC} = 5.5 V, V _O = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA
I _{CC}	V _{CC} = 5.5 V, V _I = V _{CC} or GND, I _O = 0,	Outputs high			250		250		250	μA
		Outputs low			30		30		30	mA
		Outputs disabled			250		250		250	μA
ΔI _{CC} #	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND				1.5		1.5		1.5	mA
C _I	V _I = 2.5 V or 0.5 V	Control inputs			7					pF
C _{IO}	V _O = 2.5 V or 0.5 V	A or B ports			12					pF

* On products compliant to MIL-STD-883, Class B, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ This data sheet limit may vary among suppliers.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

		V _{CC} = 5 V, T _A = 25°C		SN54ABT646A		SN74ABT646A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	0	125	0	125	0	125	MHz
t _w	Pulse duration, CLK high or low	4		4		4		ns
t _{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	3		3.5		3		ns
t _h	Hold time, A or B after CLKAB↑ or CLKBA↑	0		1.5		0		ns

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ$ C			SN54ABT646A		SN74ABT646A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{max}			125			125		125		MHz
t_{PLH}	CLKBA or CLKAB	A or B	2.2	4	5.1	2.2	6.7	2.2	5.6	ns
t_{PHL}			1.7	4	5.1	1.2	6.7	1.7	5.6	
t_{PLH}	A or B	B or A	1.5	3	4.3	1.5	5	1.5	4.8	ns
t_{PHL}			1.5	3.3	4.6	1.5	5.6	1.5	5.4	
t_{PLH}	SAB or SBA†	B or A	1.5	4	5.1	1.5	7.8	1.5	6.5	ns
t_{PHL}			1.5	3.6	4.9	1.5	6.2	1.5	5.9	
t_{PZH}	$\overline{OE}$	A or B	1.5	4.3	5.3	1.5	7	1.5	6.3	ns
t_{PZL}			3	5.8	7.4	3	10.5	3	8.8	
t_{PHZ}	$\overline{OE}$	A or B	1.5	3.5	4.5	1	7.3	1.5	5	ns
t_{PLZ}			1.5	3	4	1.5	5.7	1.5	4.5	
t_{PZH}	DIR	A or B	1.5	4.5	5.7	1.5	7.3	1.5	6.7	ns
t_{PZL}			2.5	6.5	9	2.5	11	2.5	9.5	
t_{PHZ}	DIR	A or B	1.5	3.8	5	1	9	1.5	5.7	ns
t_{PLZ}			1.5	3.8	4.7	1.2	6.7	1.5	6	

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.



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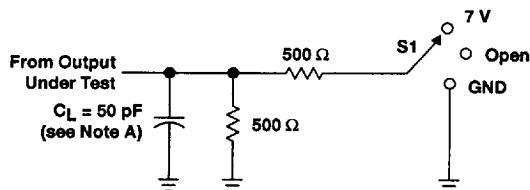
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SN54ABT646A, SN74ABT646A OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

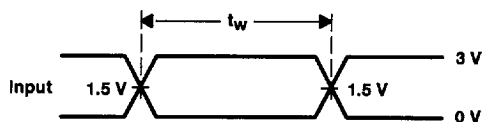
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PARAMETER MEASUREMENT INFORMATION

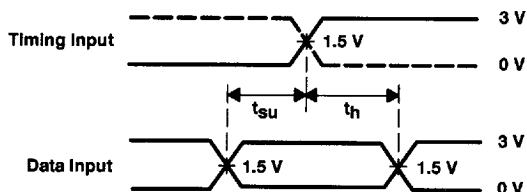


LOAD CIRCUIT FOR OUTPUTS

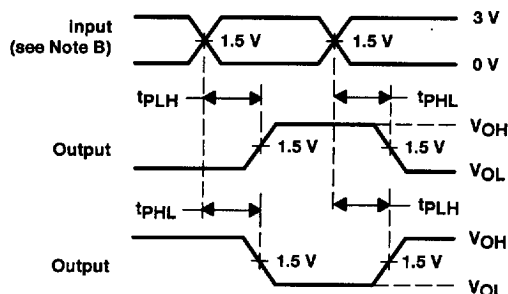
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



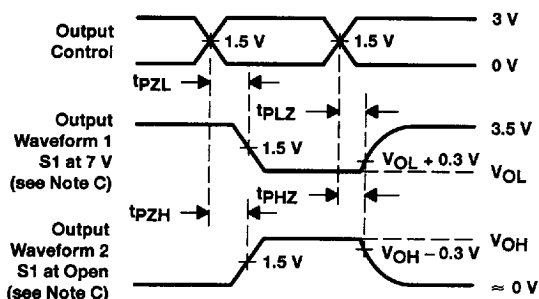
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

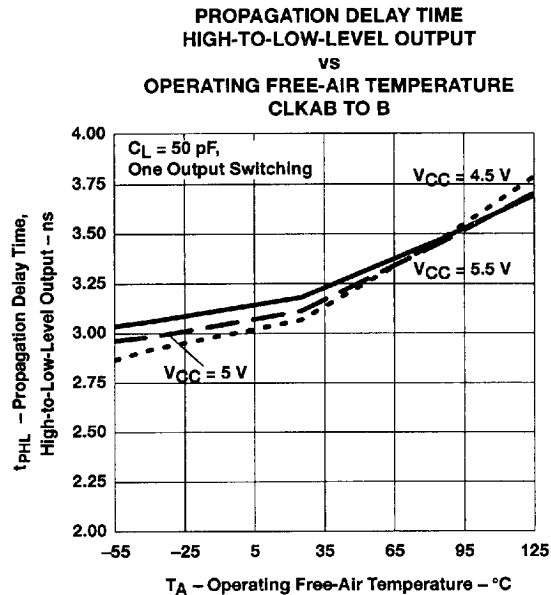
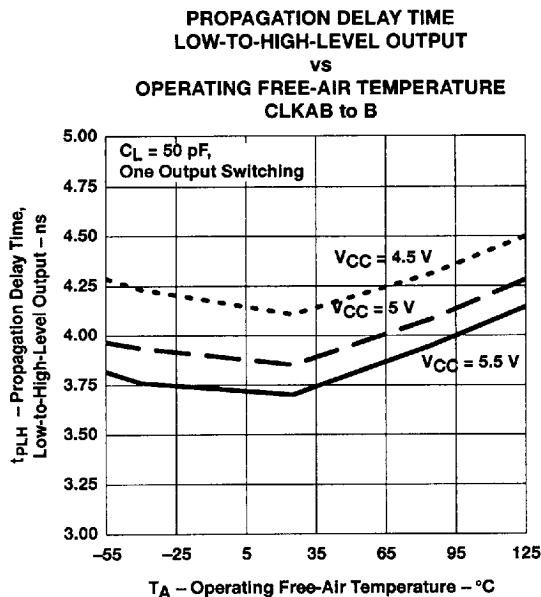
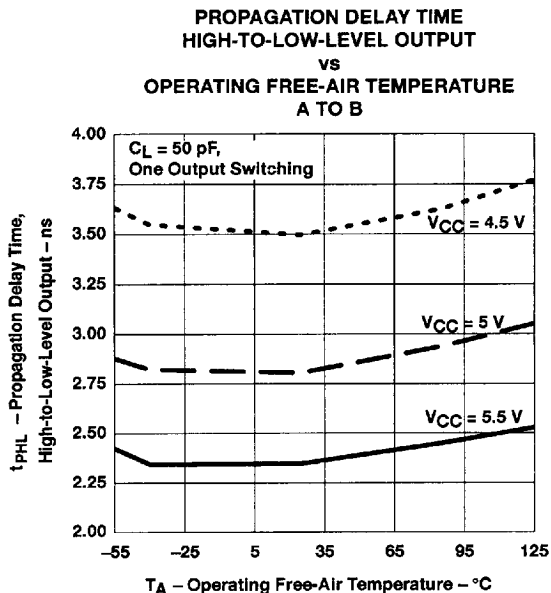
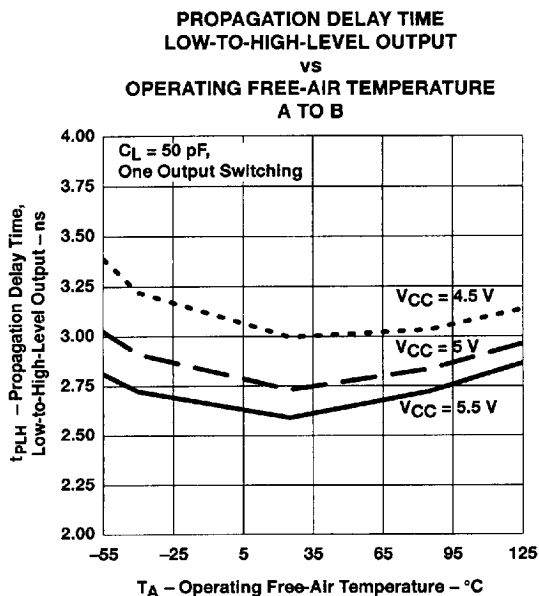
Figure 2. Load Circuit and Voltage Waveforms

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Propagation Delay Time vs Temperature



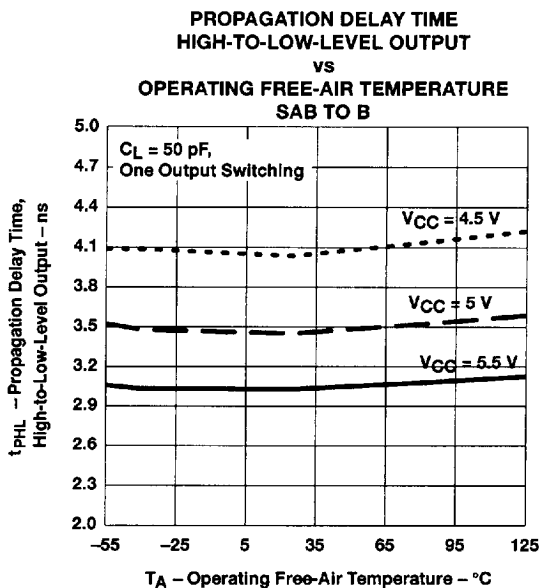
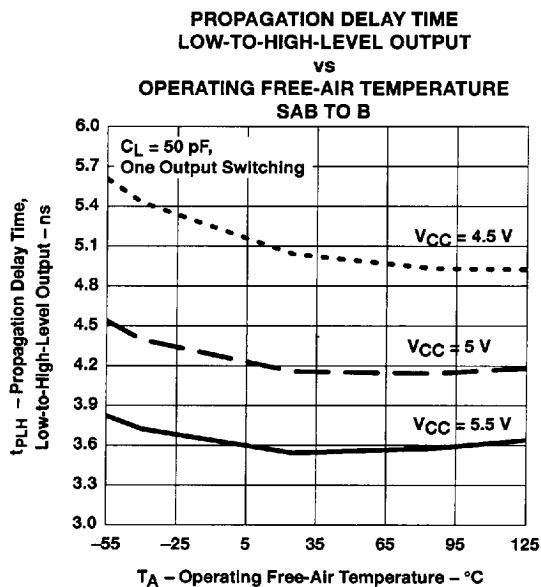
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Propagation Delay Time vs Temperature

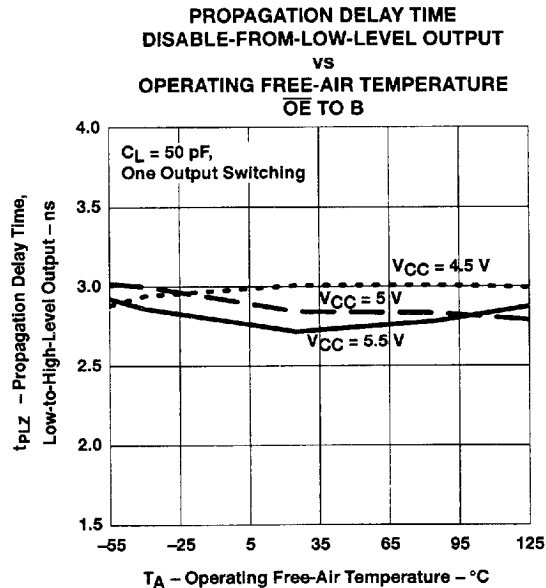
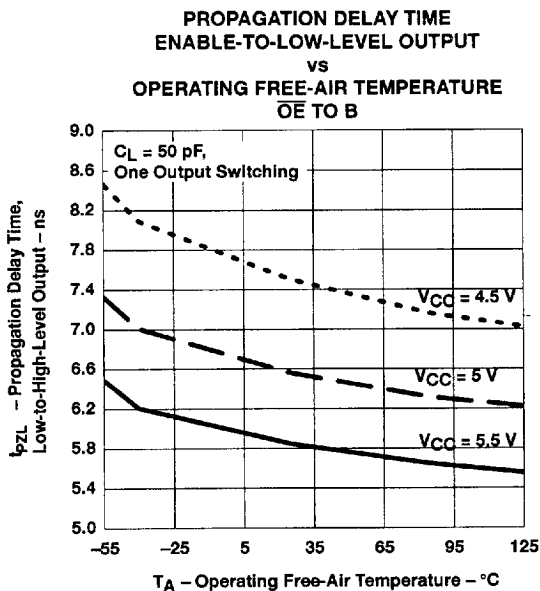
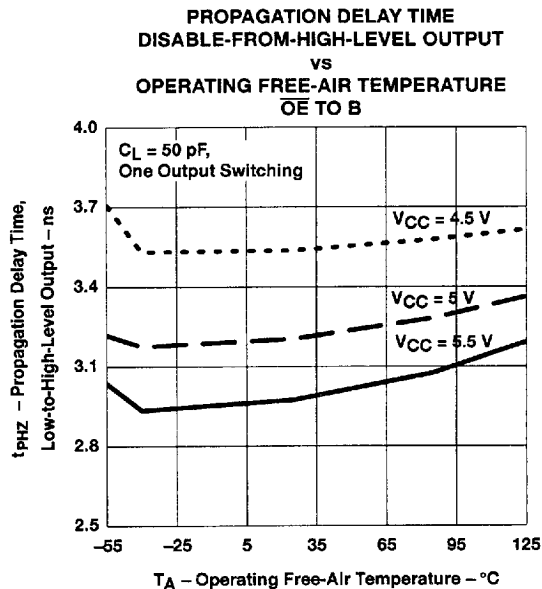
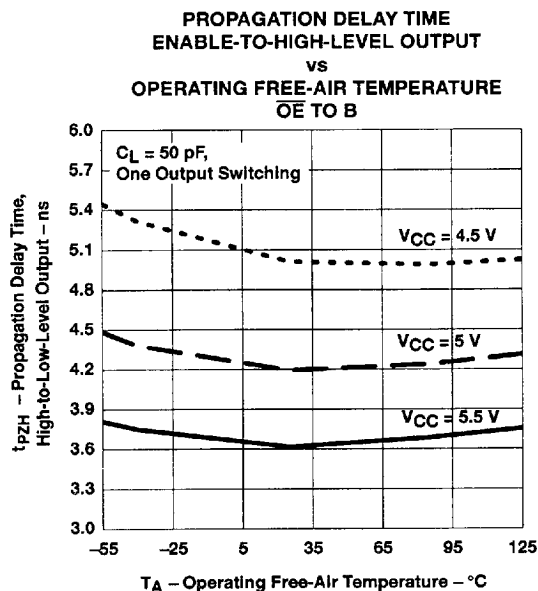


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Propagation Delay Time vs Temperature



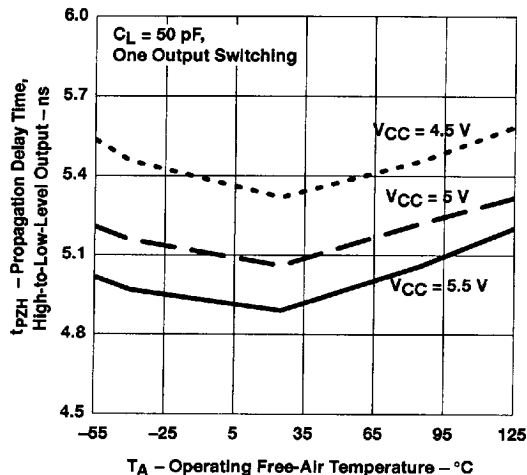
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Propagation Delay Time vs Temperature

PROPAGATION DELAY TIME ENABLE-TO-HIGH-LEVEL OUTPUT

vs

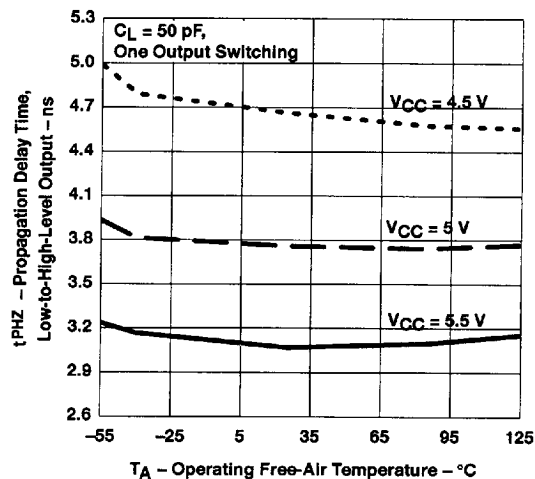
OPERATING FREE-AIR TEMPERATURE
DIR TO B



PROPAGATION DELAY TIME DISABLE-FROM-HIGH-LEVEL OUTPUT

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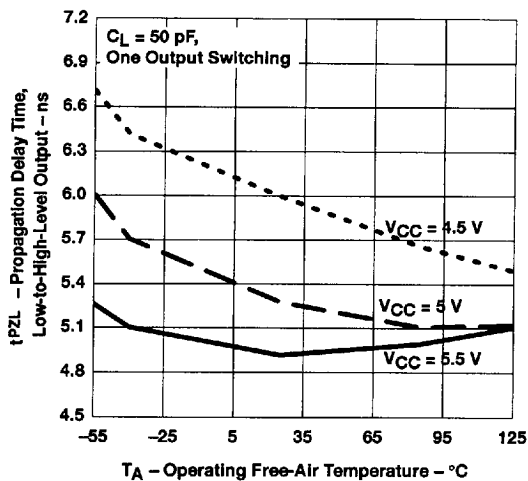
OPERATING FREE-AIR TEMPERATURE
DIR TO B



PROPAGATION DELAY TIME ENABLE-TO-LOW-LEVEL OUTPUT

vs

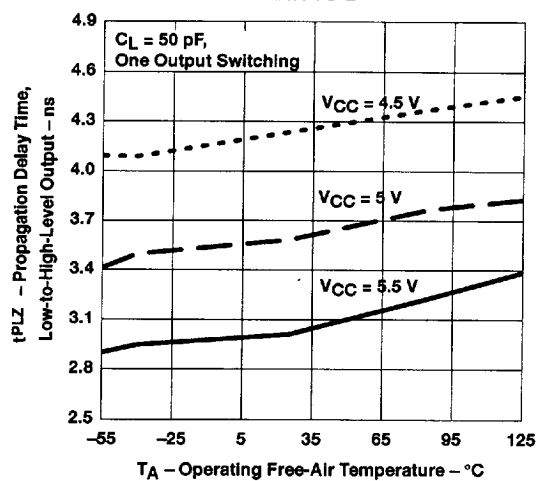
OPERATING FREE-AIR TEMPERATURE
DIR TO B



PROPAGATION DELAY TIME DISABLE-FROM-LOW-LEVEL OUTPUT

vs

OPERATING FREE-AIR TEMPERATURE
DIR TO B

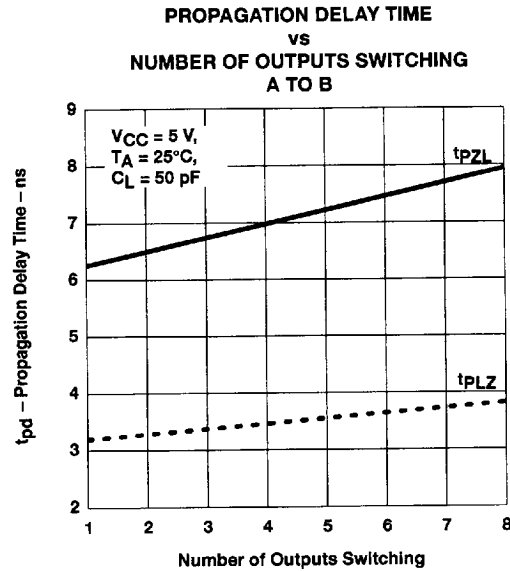
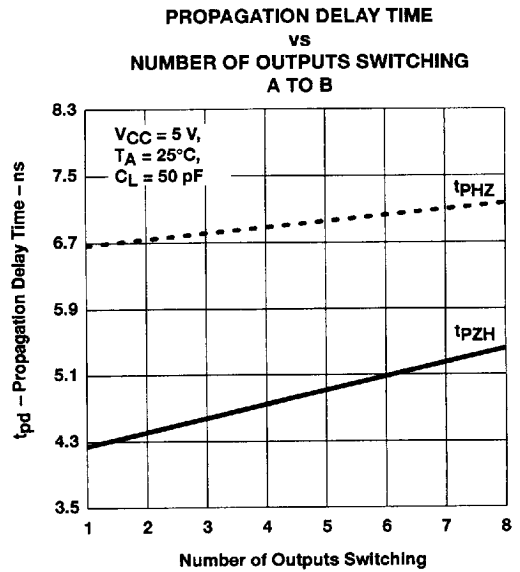
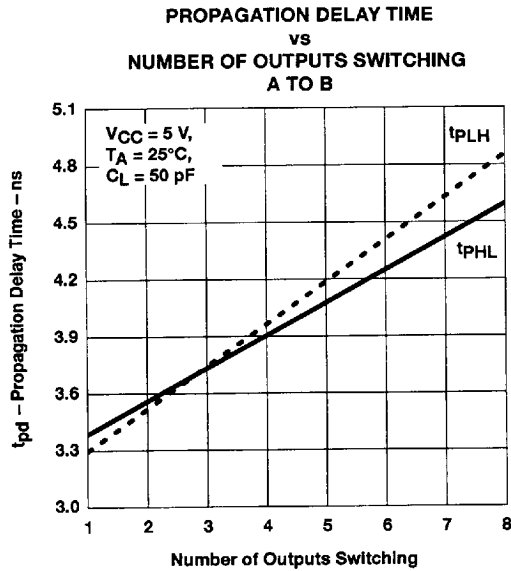


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Propagation Delay Time vs Number of Outputs Switching

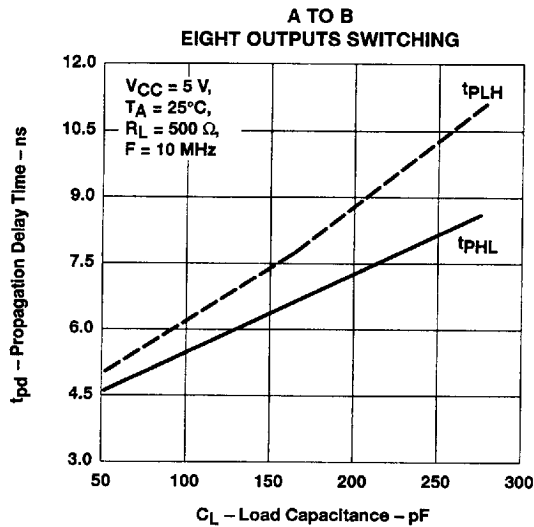
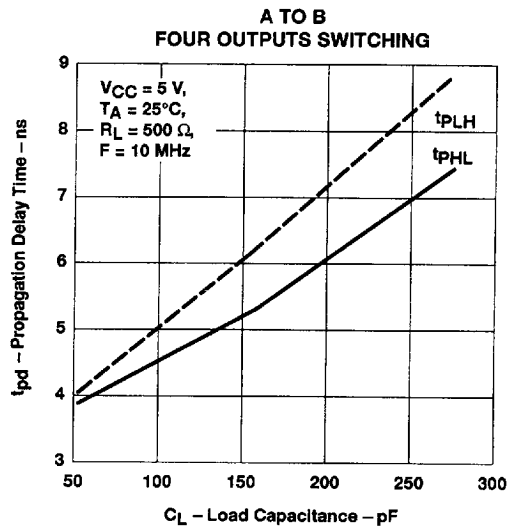
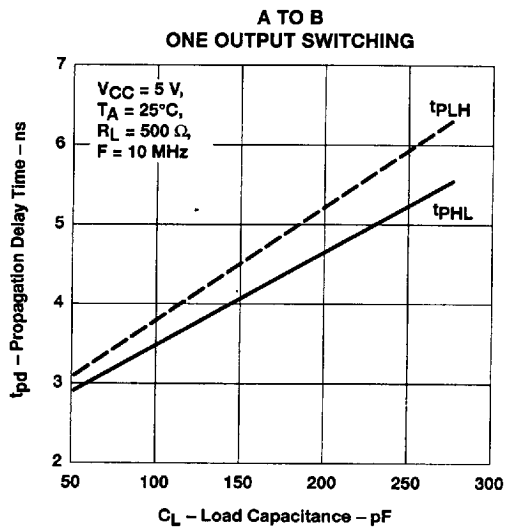


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Propagation Delay Time vs Load Capacitance

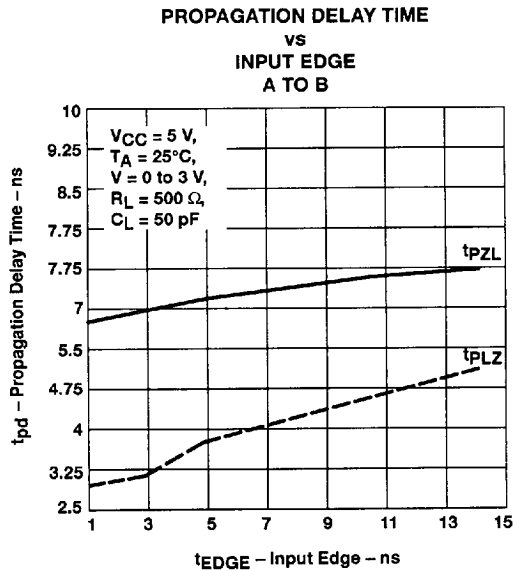
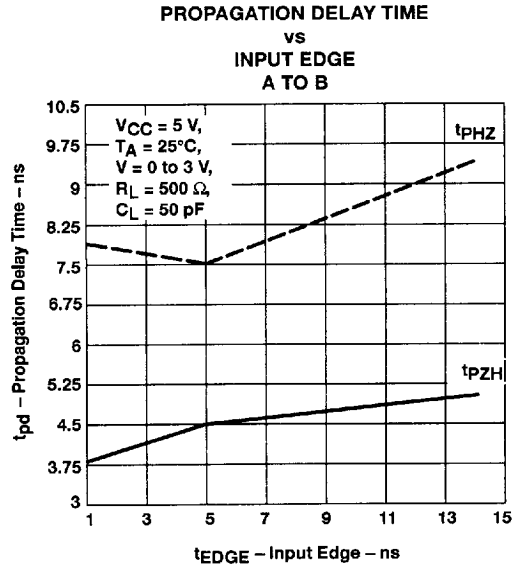
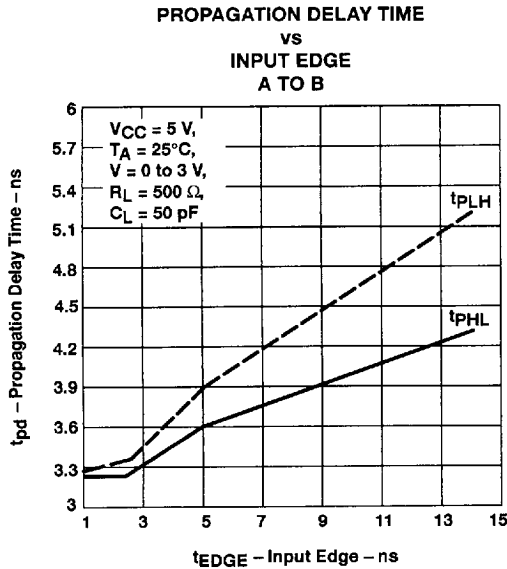


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Propagation Delay Time vs Input Edge



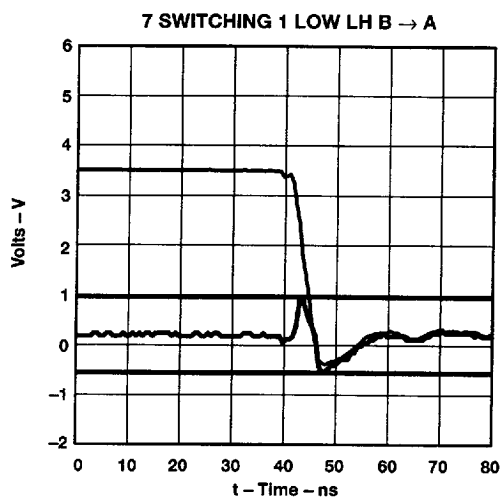
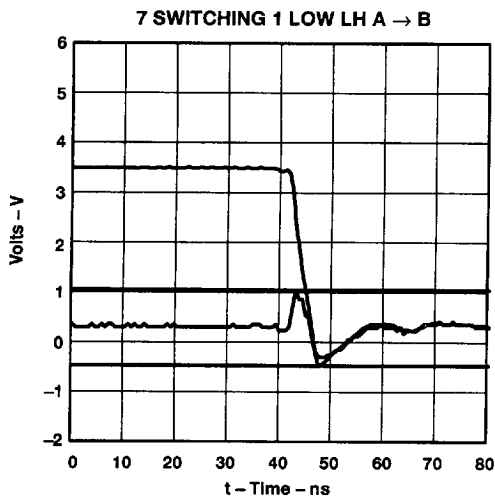
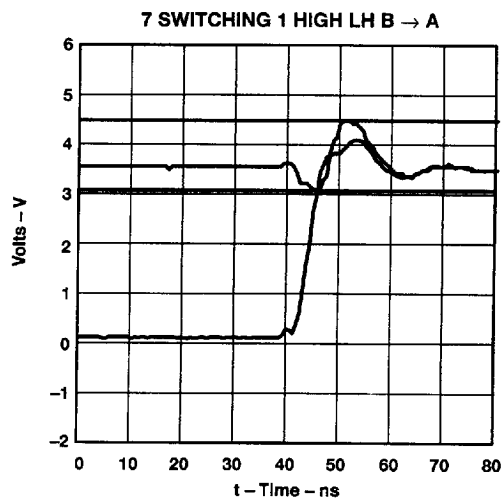
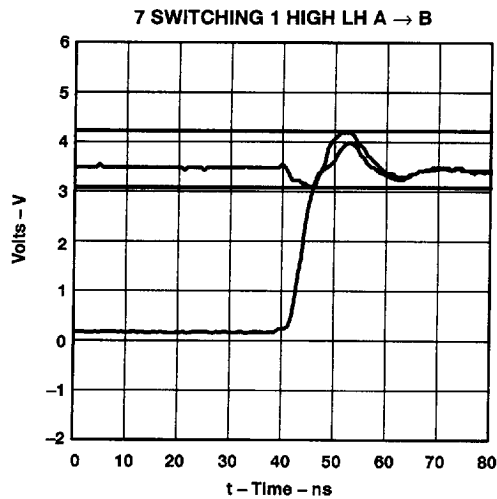
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VOHV and VOLP



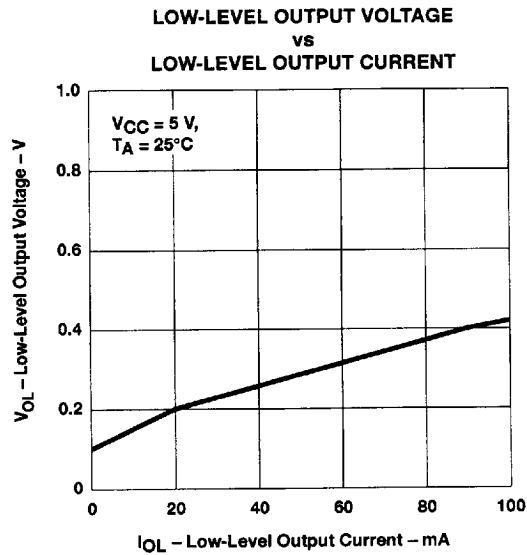
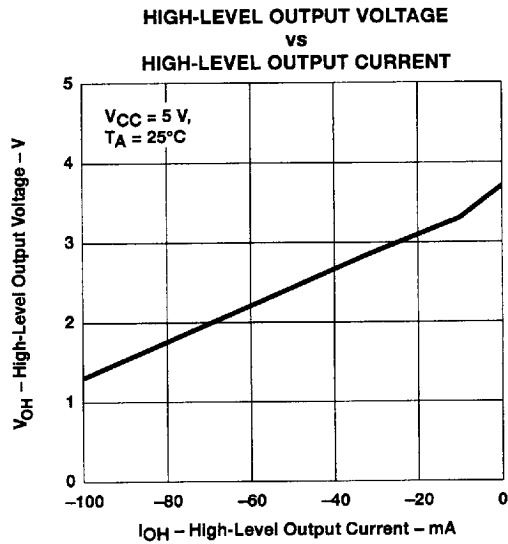
VOHV = Minimum (valley) voltage induced on a quiescent high-level output during switching of other outputs.
VOLP = Maximum (peak) voltage induced on a quiescent low-level output during switching of other outputs.

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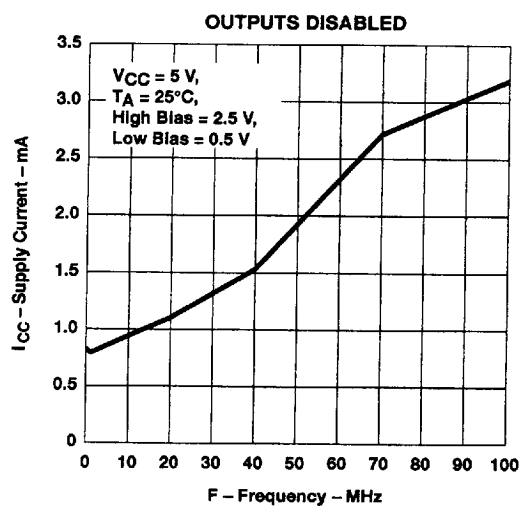
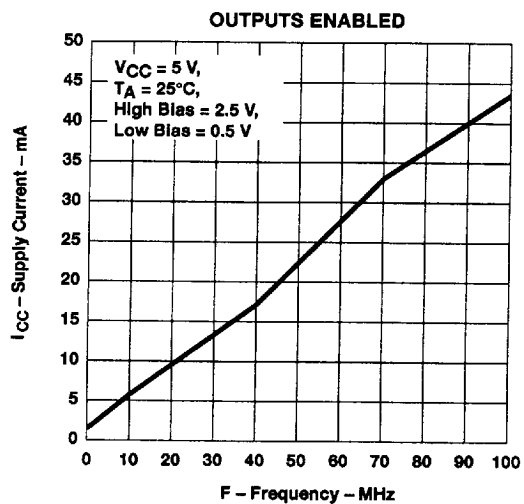
Typical Characteristics



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Supply Current vs Frequency



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