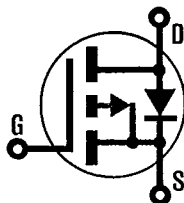


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HEXFET® TRANSISTORS IRFF9210

P-CHANNEL
POWER MOSFETs
TO-39 PACKAGE

IRFF9211

IRFF9212

IRFF9213

-200 Volt, 3.0 Ohm HEXFET

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The P-Channel HEXFETs are designed for applications which require the convenience of reverse polarity operation. They retain all of the features of the more common N-Channel HEXFETs such as voltage control, very fast switching, ease of paralleling, and excellent temperature stability. The P-Channel IRFF9210 device is an approximate electrical complement to the N-Channel IRFF110 HEXFET.

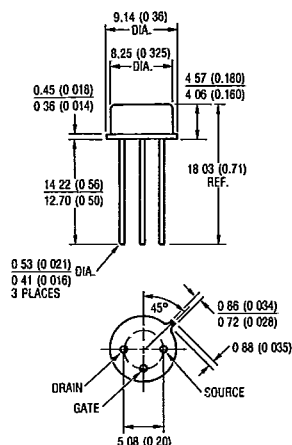
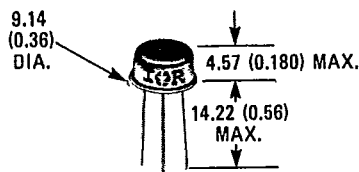
P-Channel HEXFETs are intended for use in power stages where complementary symmetry with N-Channel devices offers circuit simplification. They are also very useful in drive stages because of the circuit versatility offered by the reverse polarity connection. Applications include motor control, audio amplifiers, switched mode converters, control circuits and pulse amplifiers.

Features:

- P-Channel Versatility
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- Excellent Temperature Stability

Product Summary

Part Number	V _{DS}	R _{DS(on)}	I _D
IRFF9210	-200V	3.0Ω	-1.6A
IRFF9211	-150V	3.0Ω	-1.6A
IRFF9212	-200V	4.5Ω	-1.3A
IRFF9213	-150V	4.5Ω	-1.3A

CASE STYLE AND DIMENSIONS

Conforms to JEDEC Outline TO-205AF (TO-39)
Dimensions in Millimeters and (Inches)

TO-39

IRFF9210, IRFF9211, IRFF9212, IRFF9213 Devices

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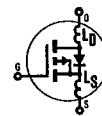
Absolute Maximum Ratings

T-39-17

Parameter	IRFF9210	IRFF9211	IRFF9212	IRFF9213	Units
V_{DS} Drain – Source Voltage ①	-200	-150	-200	-150	V
V_{DGR} Drain – Gate Voltage ($R_{GS} = 20\text{ k}\Omega$) ①	-200	-150	-200	-150	V
$I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current	-1.6	-1.6	-1.3	-1.3	A
I_{DM} Pulsed Drain Current ③	-6.5	-6.5	-5.5	-5.5	A
V_{GS} Gate – Source Voltage	± 20				V
$P_D @ T_C = 25^\circ\text{C}$ Max. Power Dissipation	15 (See Fig. 14)				W
Linear Derating Factor	0.12 (See Fig. 14)				W/K ④
I_{LM} Inductive Current, Clamped	(See Fig. 15 and 16) $L = 100\mu\text{H}$				A
T_J Operating Junction and T_{stg} Storage Temperature Range	-55 to 150				$^\circ\text{C}$
Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				$^\circ\text{C}$

Electrical Characteristics @ $T_C = 25^\circ\text{C}$ (Unless Otherwise Specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS} Drain – Source Breakdown Voltage	IRFF9210	-200	—	—	V	$V_{GS} = 0\text{V}$
	IRFF9212	—	—	—	V	
	IRFF9211	-150	—	—	V	$I_D = -250\mu\text{A}$
	IRFF9213	—	—	—	V	
$V_{GS(th)}$ Gate Threshold Voltage	ALL	-2.0	—	-4.0	V	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$
I_{GSS} Gate – Source Leakage Forward	ALL	—	—	-100	nA	$V_{GS} = -20\text{V}$
I_{GSS} Gate – Source Leakage Reverse	ALL	—	—	100	nA	$V_{GS} = 20\text{V}$
I_{DSS} Zero Gate Voltage Drain Current	ALL	—	—	-250	μA	$V_{DS} = \text{Max. Rating}, V_{GS} = 0\text{V}$
		—	—	-1000	μA	$V_{DS} = \text{Max. Rating} \times 0.8, V_{GS} = 0\text{V}, T_C = 125^\circ\text{C}$
$I_{D(on)}$ On-State Drain Current ②	IRFF9210	-1.6	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)} \text{ max.}, V_{GS} = -10\text{V}$
	IRFF9211	—	—	—	A	
	IRFF9212	-1.3	—	—	A	
	IRFF9213	—	—	—	A	
$R_{DS(on)}$ Static Drain-Source On-State Resistance ②	IRFF9210	—	2.3	3.0	Ω	$V_{GS} = -10\text{V}, I_D = -0.8\text{A}$
	IRFF9211	—	—	—	Ω	
	IRFF9212	—	3.5	4.5	Ω	
	IRFF9213	—	—	—	Ω	
g_{fs} Forward Transconductance ②	ALL	0.7	0.9	—	S (W)	$V_{DS} > I_{D(on)} \times R_{DS(on)} \text{ max.}, I_D = -0.8\text{A}$
C_{iss} Input Capacitance	ALL	—	170	300	pF	$V_{GS} = 0\text{V}, V_{DS} = -25\text{V}, f = 1.0\text{ MHz}$ See Fig. 10
C_{oss} Output Capacitance	ALL	—	50	100	pF	
C_{rss} Reverse Transfer Capacitance	ALL	—	15	35	pF	$V_{DD} = 0.5 BV_{DSS}, I_D = -0.8\text{A}, Z_\theta = 50\Omega$ See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
$t_{d(on)}$ Turn-On Delay Time	ALL	—	8.0	15	ns	
t_r Rise Time	ALL	—	15	25	ns	
$t_{d(off)}$ Turn-Off Delay Time	ALL	—	10	15	ns	
t_f Fall Time	ALL	—	8.0	15	ns	
Q_g Total Gate Charge (Gate – Source Plus Gate-Drain)	ALL	—	8.0	11	nC	$V_{GS} = -15\text{V}, I_D = -3.5\text{A}, V_{DS} = 0.8\text{V Max. Rating.}$ See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs} Gate-Source Charge	ALL	—	5.0	—	nC	
Q_{gd} Gate-Drain ("Miller") Charge	ALL	—	3.0	—	nC	
L_D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.
L_S Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.



Thermal Resistance

R_{thJC} Junction-to-Case	ALL	—	—	8.33	K/W ④	
R_{thJA} Junction-to-Ambient	ALL	—	—	175	K/W ④	Typical socket mount

Source-Drain Diode Ratings and Characteristics

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I_S	Continuous Source Current (Body Diode)	IRFF9210 IRFF9211	—	—	-1.6	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRFF9212 IRFF9213	—	—	-1.3	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFF9210 IRFF9211	—	—	-6.5	A	
		IRFF9212 IRFF9213	—	—	-5.5	A	
V_{SD}	Diode Forward Voltage ②	IRFF9210 IRFF9211	—	—	-5.8	V	$T_C = 25^\circ\text{C}$, $I_S = -1.6\text{A}$, $V_{GS} = 0\text{V}$
		IRFF9212 IRFF9213	—	—	-5.5	V	$T_C = 25^\circ\text{C}$, $I_S = -1.3\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	ALL	—	240	—	ns	$T_J = 150^\circ\text{C}$, $I_F = -1.6\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	—	1.7	—	μC	$T_J = 150^\circ\text{C}$, $I_F = -1.6\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25^\circ\text{C}$ to 150°C . ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

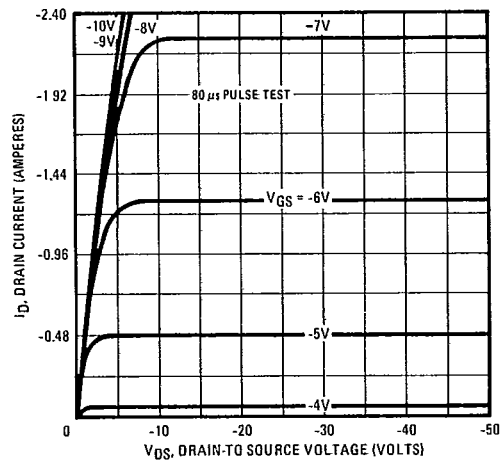
④ $\text{K/W} = ^\circ\text{C/W}$
 $\text{W/K} = \text{W}/^\circ\text{C}$ 

Fig. 1 — Typical Output Characteristics

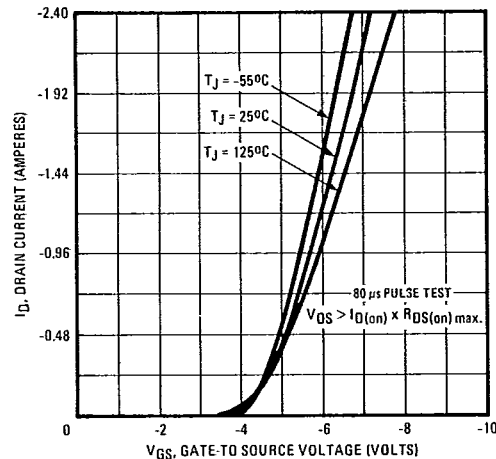


Fig. 2 — Typical Transfer Characteristics

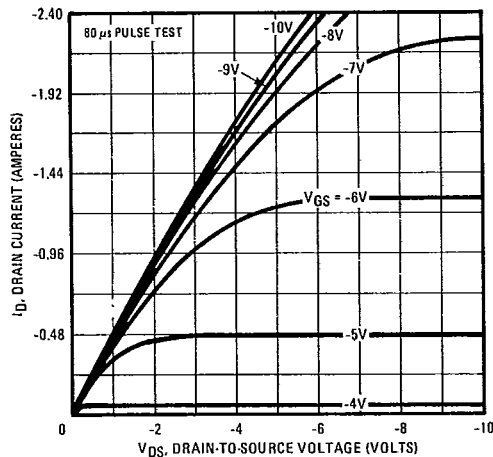


Fig. 3 — Typical Saturation Characteristics

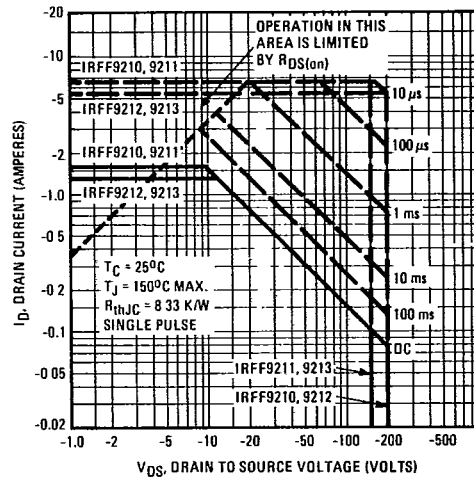


Fig. 4 — Maximum Safe Operating Area

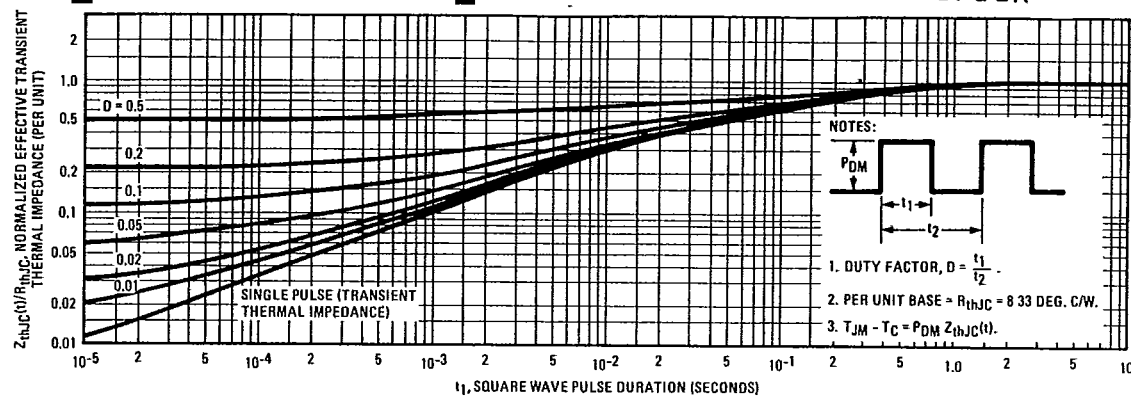


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

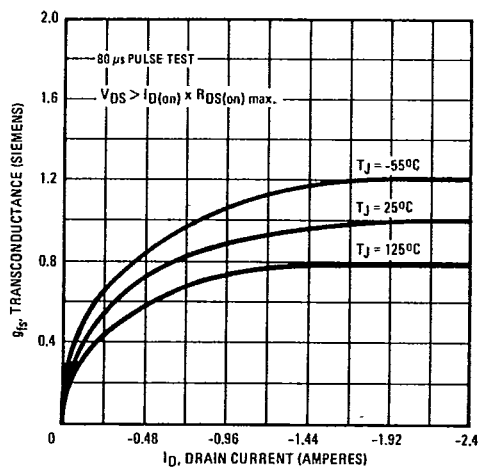


Fig. 6 — Typical Transconductance Vs. Drain Current

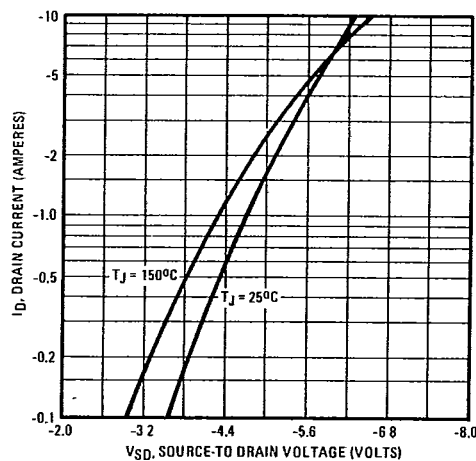


Fig. 7 — Typical Source-Drain Diode Forward Voltage

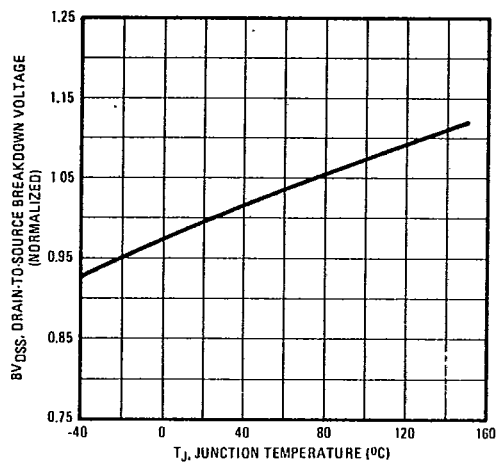


Fig. 8 — Breakdown Voltage Vs. Temperature

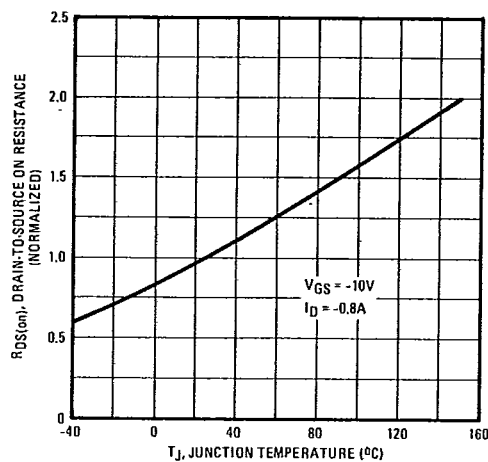


Fig. 9 — Normalized On-Resistance Vs. Temperature

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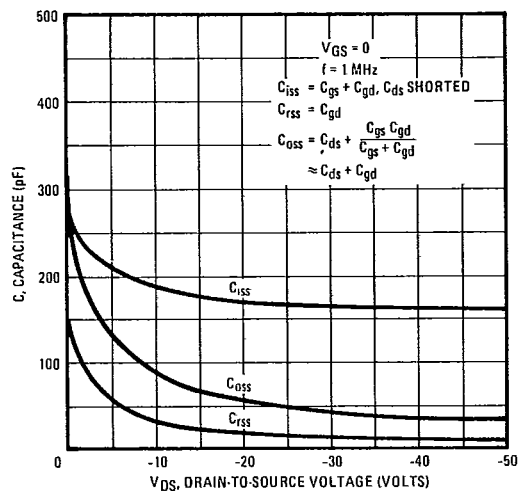


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

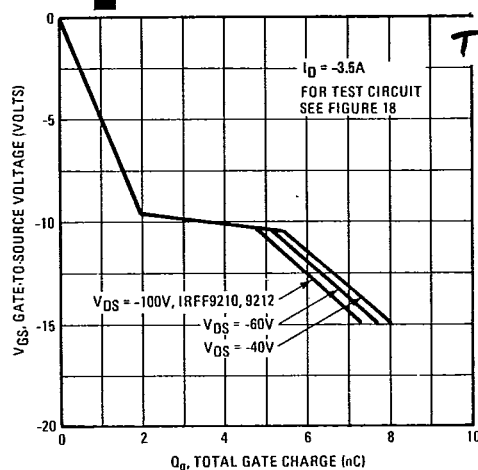


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

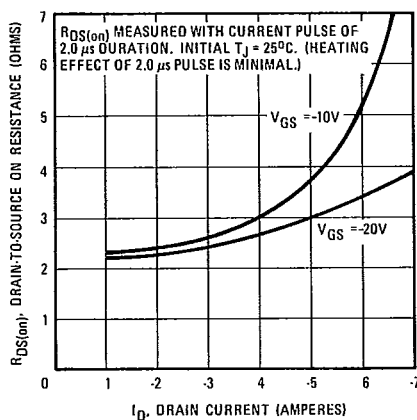


Fig. 12 - Typical On-Resistance Vs. Drain Current

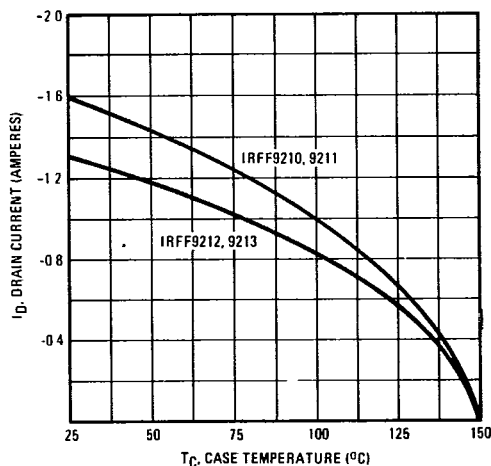


Fig. 13 - Maximum Drain Current Vs. Case Temperature

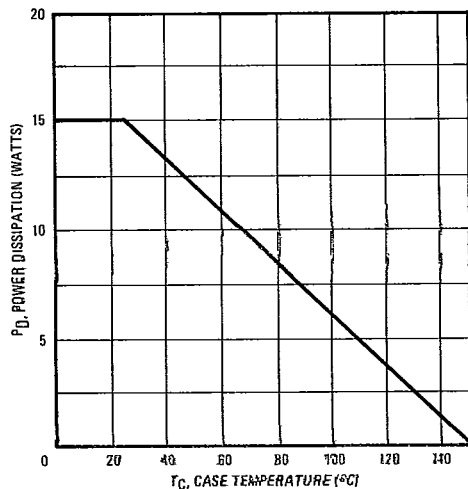


Fig. 14 - Power Vs. Temperature Derating Curve

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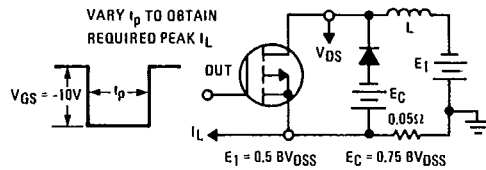


Fig. 15 - Clamped Inductive Test Circuit

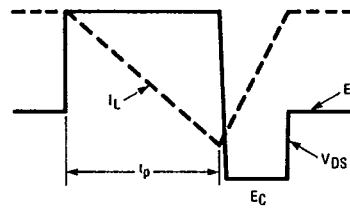


Fig. 16 - Clamped Inductive Waveforms

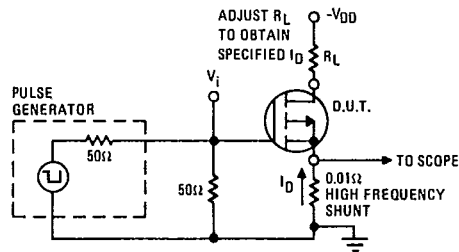


Fig. 17 - Switching Time Test Circuit

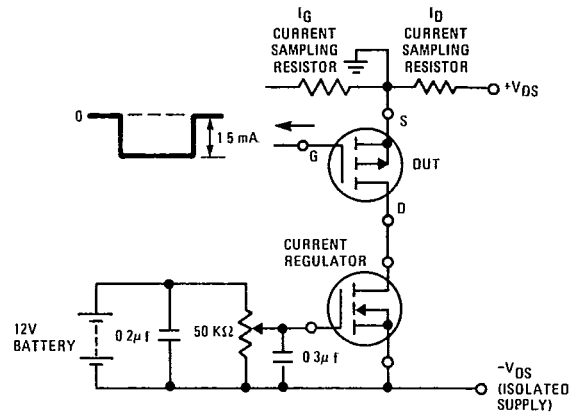


Fig. 18 - Gate Charge Test Circuit

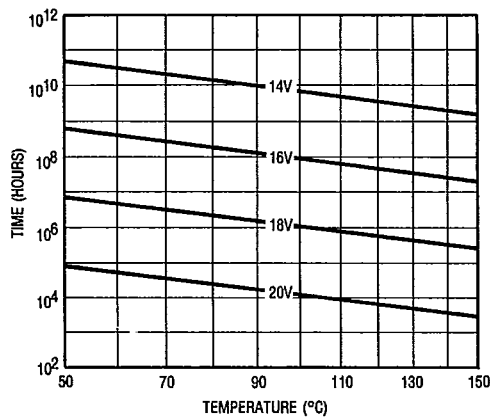


Fig. 19 - Typical Time to Accumulated 1% Failure

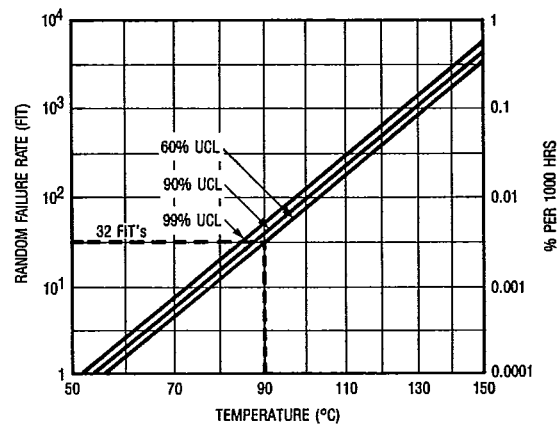


Fig. 20 - Typical High Temperature Reverse Bias (HTRB) Failure Rate

*The data shown is correct as of April 15, 1987. This information is updated on a quarterly basis; for the latest reliability data, please contact your local IR field office.