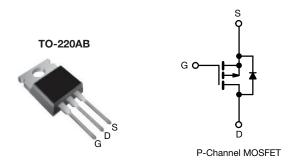


www.vishay.com

Vishay Siliconix

Power MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	-60				
$R_{DS(on)}(\Omega)$	V _{GS} = -10 V	0.14			
Q _g max. (nC)	34				
Q _{gs} (nC)	9.9				
Q _{gd} (nC)	16				
Configuration	Single				



FEATURES

- Dynamic dV/dt rating
- · Repetitive avalanche rated
- P-channel
- 175 °C operating temperature
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non-RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details.

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION			
Package	TO-220AB		
Lead (Pb)-free	IRF9Z34PbF		
Lead (FD)-life	SiHF9Z34-E3		
SnPb	IRF9Z34		
SIFU	SiHF9Z34		

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-Source Voltage		V_{DS}	-60		
Gate-Source Voltage		V_{GS}	± 20	V	
Continuous Drain Current	V_{GS} at -10 V $\frac{T_C = 25 ^{\circ}\text{C}}{T_C = 100 ^{\circ}\text{C}}$		-18		
Continuous Drain Current	V_{GS} at -10 V $T_C = 100 ^{\circ}C$	l _D	-13	A	
Pulsed Drain Current a	I _{DM}	-72			
Linear Derating Factor		0.59	W/°C		
Single Pulse Avalanche Energy b	E _{AS}	370	mJ		
Repetitive Avalanche Current ^a	I _{AR}	-18	А		
Repetitive Avalanche Energy ^a	E _{AR}	8.8	mJ		
Maximum Power Dissipation $T_C = 25 ^{\circ}C$		P_{D}	88	W	
Peak Diode Recovery dV/dt c	dV/dt	-4.5	V/ns		
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +175	00		
Soldering Recommendations (Peak temperature) d for 10 s			300	°C	
Mounting Torque	6-32 or M3 screw		10	lbf ⋅ in	
Mounting Torque	0-32 OF IVIS SCIEW		1.1	N⋅m	

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. V_{DD} = -25 V, starting T_J = 25 °C, L = 1.3 mH, R_g = 25 Ω , I_{AS} = -18 A (see fig. 12).
- c. $I_{SD} \le -18$ A, $dI/dt \le 170$ A/ μ s, $V_{DD} \le V_{DS}$, $T_J \le 175$ °C.
- d. 1.6 mm from case.

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Vishay Siliconix

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient	R _{thJA}	-	62		
Case-to-Sink, Flat, Greased Surface	R _{thCS}	0.50	-	°C/W	
Maximum Junction-to-Case (Drain)	R _{thJC}	-	1.7		

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static		'		•	•		
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$		-60	-	-	V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference to	o 25 °C, I _D = -1 mA	-	-0.060	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V$	_{GS} , I _D = 250 μA	-2.0	-	-4.0	V
Gate-Source Leakage	I _{GSS}	V _G	_S = ± 20 V	-	-	± 100	nA
	I _{DSS}	V _{DS} = -60 V, V _{GS} = 0 V		_	-	-100	
Zero Gate Voltage Drain Current			V _{DS} = -48 V, V _{GS} = 0 V, T _J = 150 °C		-	-500	μA
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = -10 V	I _D = -11 A ^b	-	-	0.14	Ω
Forward Transconductance	9 _{fs}	V _{DS} = -2	5 V, I _D = -11 A ^b	5.9	-	-	S
Dynamic	0.0						
Input Capacitance	C _{iss}	.,	0.1/	_	1100	_	
Output Capacitance	C _{oss}		_{GS} = 0 V, _S = -25 V,	_	620	-	ρF
Reverse Transfer Capacitance	C _{rss}		f = 1.0 MHz, see fig. 5		100	-	- Pi
Total Gate Charge	Qg		$I_D = -1.8 \text{ A},$ $V_{DS} = -48 \text{ V},$ see fig. 6 and 13 b	-	-	34	nC
Gate-Source Charge	Q _{gs}	V _{GS} = -10 V		-	-	9.9	
Gate-Drain Charge	Q _{gd}			-	-	16	
Turn-On Delay Time	t _{d(on)}			-	18	-	
Rise Time	t _r	V_{DD} = -30 V, I_{D} = -18 A, R_{g} = 12 Ω , R_{D} = 1.5 Ω , see fig. 10 b		-	120	-	ns
Turn-Off Delay Time	t _{d(off)}			-	20	-	
Fall Time	t _f			-	58	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	n I I
Internal Source Inductance	L _S			-	7.5	-	nH
Gate Input Resistance	R_g	f = 1 MHz, open drain		0.7	-	3.9	Ω
Drain-Source Body Diode Characteristic	cs						
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p -n junction diode		-	-	-18	А
Pulsed Diode Forward Current ^a	I _{SM}			-	-	-72	
Body Diode Voltage	V _{SD}	$T_J = 25 ^{\circ}\text{C}, I_S$	$=$ -18 A, $V_{GS} = 0 V^b$	-	-	-6.3	V
Body Diode Reverse Recovery Time	t _{rr}	T _ 25 °C !	10 A dl/dt = 100 A/··- b	-	100	200	ns
Body Diode Reverse Recovery Charge	Q _{rr}	$T_J = 25 ^{\circ}\text{C}, I_F = -18 \text{A}, \text{dI/dt} = 100 \text{A/}\mu\text{s}^{\text{b}}$		-	0.28	0.52	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn		rn-on is dominated by L_S and L_Γ			L _D)

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width \leq 300 μ s; duty cycle \leq 2 %.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

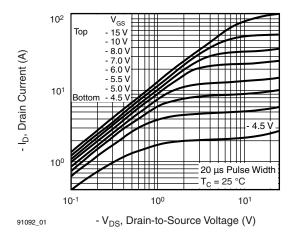


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

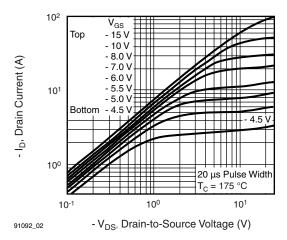


Fig. 2 - Typical Output Characteristics, $T_C = 175$ °C

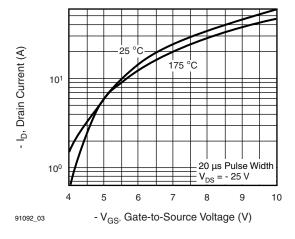


Fig. 3 - Typical Transfer Characteristics

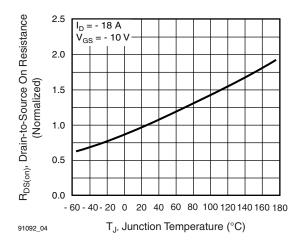


Fig. 4 - Normalized On-Resistance vs. Temperature

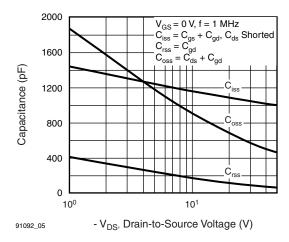


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

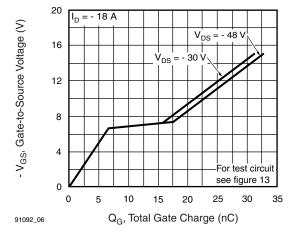


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



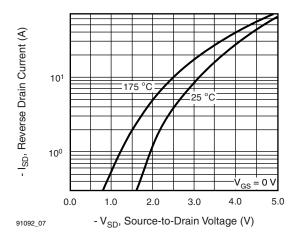


Fig. 7 - Typical Source-Drain Diode Forward Voltage

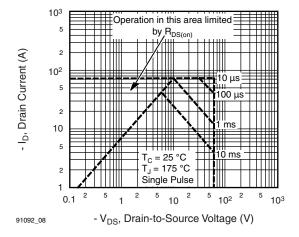


Fig. 8 - Maximum Safe Operating Area

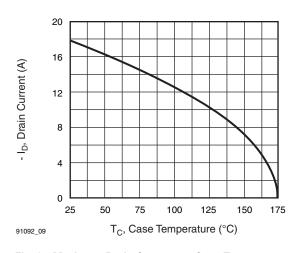


Fig. 9 - Maximum Drain Current vs. Case Temperature

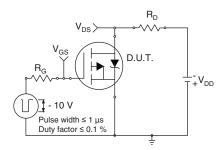


Fig. 10a - Switching Time Test Circuit

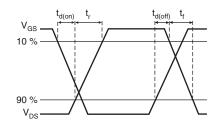


Fig. 10b - Switching Time Waveforms

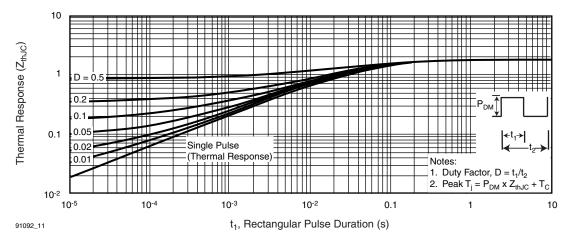


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

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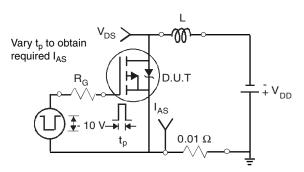


Fig. 12a - Unclamped Inductive Test Circuit

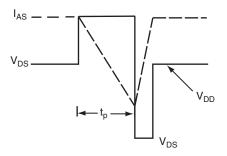


Fig. 12b - Unclamped Inductive Waveforms

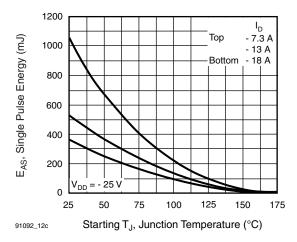


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

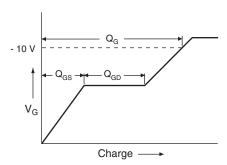


Fig. 13a - Basic Gate Charge Waveform

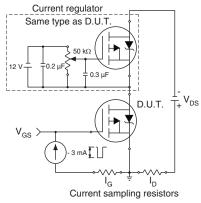
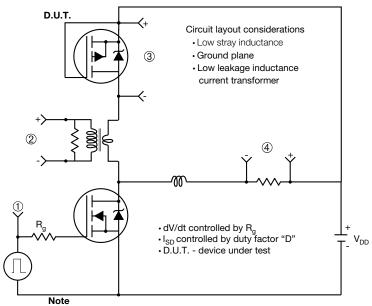


Fig. 13b - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



• Compliment N-Channel of D.U.T. for driver

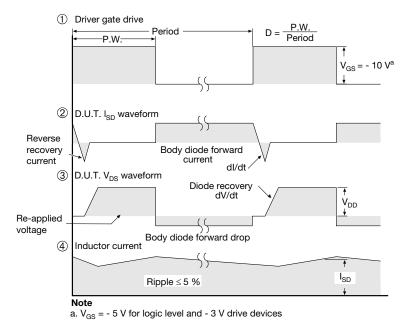
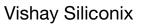


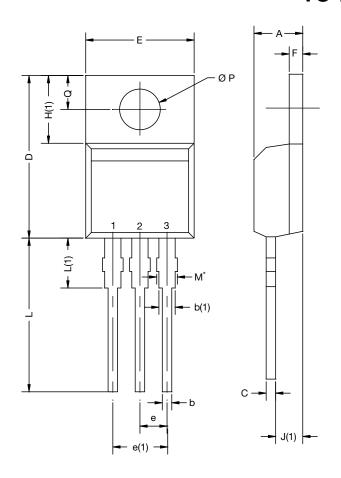
Fig. 14 - For P-Channel

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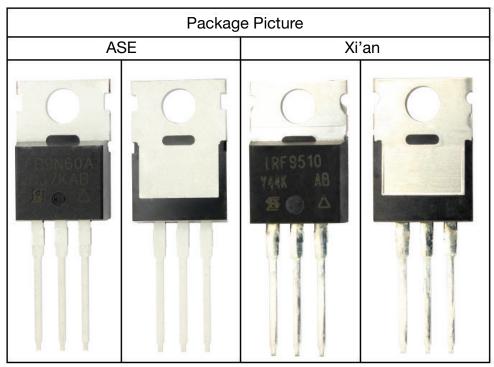
TO-220-1



DIM.	MILLIM	IETERS	INCHES		
	MIN.	MAX.	MIN.	MAX.	
Α	4.24	4.65	0.167	0.183	
b	0.69	1.02	0.027	0.040	
b(1)	1.14	1.78	0.045	0.070	
С	0.36	0.61	0.014	0.024	
D	14.33	15.85	0.564	0.624	
E	9.96	10.52	0.392	0.414	
е	2.41	2.67	0.095	0.105	
e(1)	4.88	5.28	0.192	0.208	
F	1.14	1.40	0.045	0.055	
H(1)	6.10	6.71	0.240	0.264	
J(1)	2.41	2.92	0.095	0.115	
L	13.36	14.40	0.526	0.567	
L(1)	3.33	4.04	0.131	0.159	
ØΡ	3.53	3.94	0.139	0.155	
Q	2.54	3.00	0.100	0.118	
ECN: X15-0364-Rev. C, 14-Dec-15 DWG: 6031					

Note

 \bullet $M^{\star}=0.052$ inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM



Revison: 14-Dec-15 1 Document Number: 66542



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