# Edge629
# 1 GHz Timing Deskew and Quad Fanout Element



## Description

The Edge629 is a monolithic timing delay and signal fanout solution manufactured in a high-performance bipolar process. In Automatic Test Equipment (ATE) applications, the Edge629 buffers, distributes, and aligns timing signals across multiple channels (typically found inside Memory Test Systems). It is also suitable for per pin deskew in Logic Testers.

The Edge629 supports:

- Minimum pulse width = 330 ps with Falling Edge Adjust disabled, 500 ps with Falling Edge Adjust enabled
- Net usable delay span ≥ 4.0 ns
- Falling Edge Adjust ±250 ps
- On Board DACs to generate 5 ps minimum resolution.

With a maximum operating frequency of 1 GHz, the Edge629 is optimized for extremely high speed, high accuracy testers, particularly those aimed to test RAMBUS memory devices.

The Edge629 solves several difficult problems associated with aligning multiple timing signals because it can:

- delay very narrow pulses over a long timing span
- adjust the falling edge independently from the overall propagation delay
- maintain extreme timing accuracy for very narrow (sub-ns) pulses
- maintain tight timing accuracy over changes in frequency, duty cycle, and pattern.

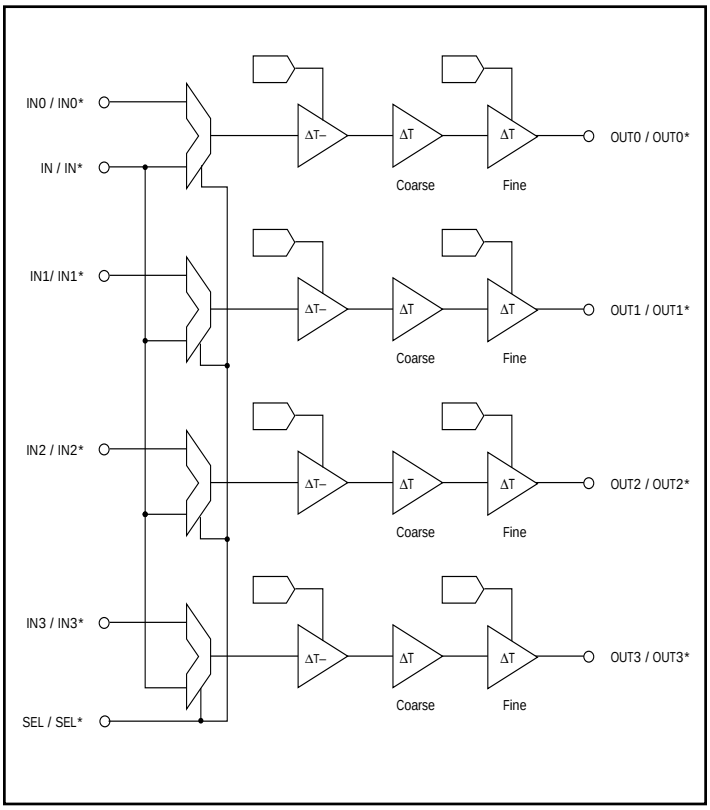
## Applications

- Memory Test Equipment
  - Data Fanout
  - Channel Deskew
- Logic Testers
  - Per Pin Deskew
- Clock / Signal Fanout

## Features

- Fmax ≥ 1 GHz
- Independent Falling Edge Adjust
- Small Footprint (10 mm x 10 mm)
- Excellent Timing Accuracy
- Very Stable Timing Delays
- 5 ps Minimum Resolution
- ECL, CMOS Compatible Inputs

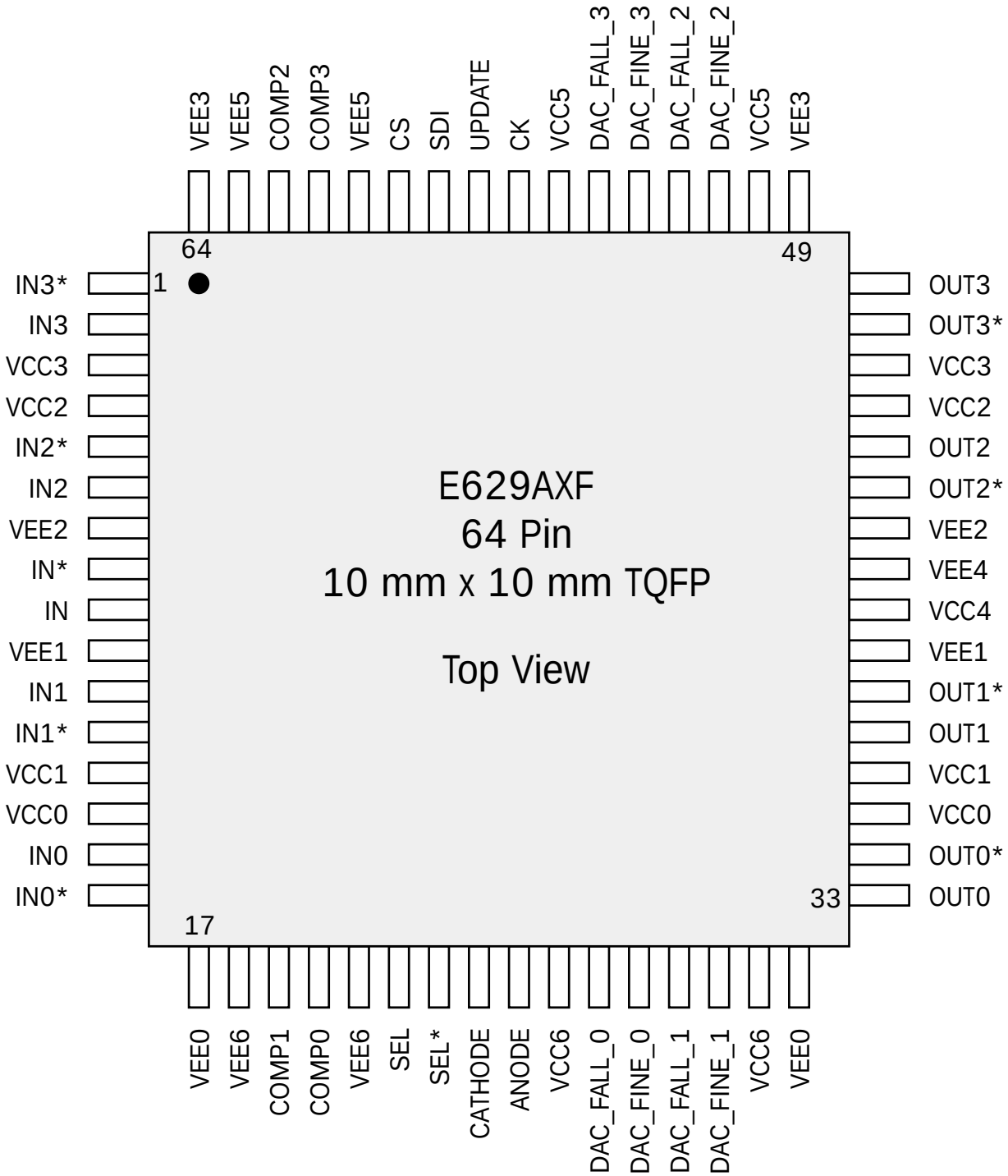
## Functional Block Diagram



## PIN Description

| Pin Name | Pin # | Description |
|---|---|---|
| IN/IN* | 9, 8 | Differential input signal used for 1:4 signal fanout. |
| IN0, IN0*<br>IN1/IN1*<br>IN2/IN2*<br>IN3/IN3* | 15, 16<br>11, 12<br>6, 5<br>2, 1 | Differential input signals used for 1:1 signal fanout. |
| OUT0/OUT0*<br>OUT1/OUT1*<br>OUT2/OUT2*<br>OUT3/OUT3* | 33, 34<br>37, 38<br>44, 43<br>48, 47 | Differential output signals. |
| SEL/SEL* | 22, 23 | Differential input signals used to select the input signal source. |
| SDI | 58 | Serial data input. |
| CK | 56 | Clock used to latch in SDI. |
| CS | 59 | Chip select. |
| UPDATE | 57 | Digital input which loads the delay registers. |
| CATHODE, ANODE | 24, 25 | Terminals of an on-chip thermal diode string. |
| COMP0-3 | 20, 19, 62, 61 | External op amp compensation pins. |
| DAC_FALL_(0-3) | 27, 29, 52, 54 | Falling edge adjust DAC outputs. For test purposes only; nothing should be connected to these pins. |
| DAC_FINE_(0-3) | 28, 30, 51, 53 | Fine delay DAC outputs. For test purposes only; nothing should be connected to these pins. |
| VCC | 3, 4, 13, 14, 26, 31, 35, 36, 40, 45, 46, 50, 55 | Positive power supply. |
| VEE | 7, 10, 17, 18, 21, 32, 39, 41, 42, 49, 60, 63, 64 | Negative power supply. |

## PIN Description *(continued)*



## Circuit Description

### Introduction

The Edge629 is a quad channel delay element with 2 basic operating modes:
1) Fanout – 1 signal in, 4 signals out
2) Pass Through – 4 signals in, 4 signals out

In all modes, each channel supports 3 delay functions:
1) Coarse timing delay
2) Fine timing delay
3) Falling edge adjust

All 3 delay functions are independent of each other, and independent for each channel.

The programming of the delay functions is done using a 16 bit register, loaded serially, which contains both a delay and an address value.

### Coarse Delay

Coarse propagation delay adjustment is accomplished using a series of gate delays and multiplexers (see Figure 1). Coarse delay provides a total delay span of:

1 Coarse LSB = 90 ps
2 Coarse LSB = 180 ps
4 Coarse LSB = 360 ps
8 Coarse LSB = 720 ps
16 Coarse LSB = 1.44 ns
32 Coarse LSB = 2.88 ns

0 ns ≤ Coarse Delay Range ≤ 5.67 ns

Each channel has its own unique coarse delay setting and may be programmed independently from all other channels. The coarse delay of any channel will not affect the fine delay of that channel, nor will it affect the overall delay of any other channel.

The propagation delay of a rising edge and falling edge will track each other over the entire coarse delay span. (Adding or subtracting coarse delay does not cause pulse width distortion.)

| Delay Code | | |
|---|---|---|
| 000000 | Minimum Delay | 0.0 ns |
| 111111 | Maximum Delay | 5.67 ns |

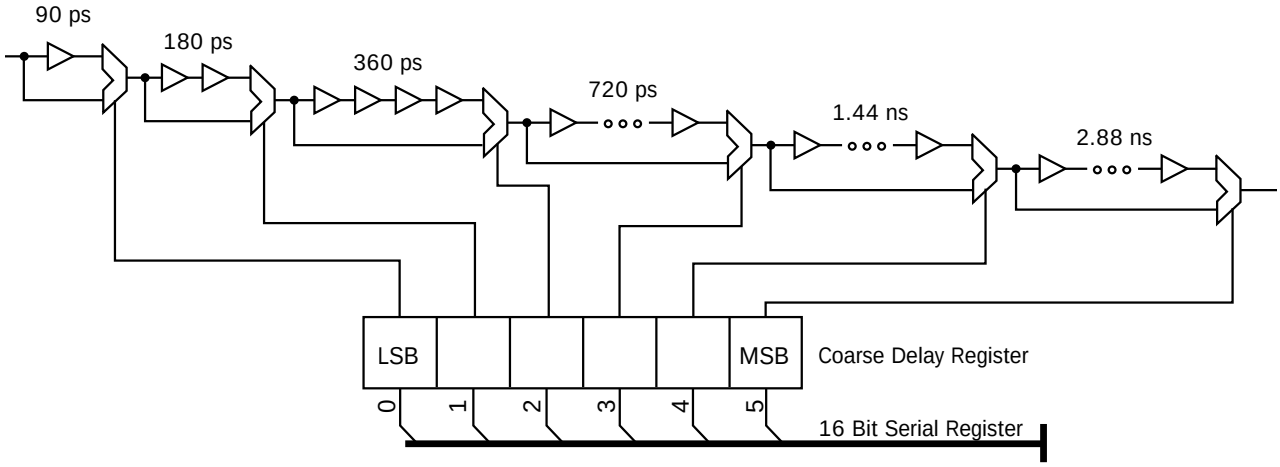



***Figure 1. Coarse Delay Architecture***

## Circuit Description *(continued)*

### Fine Delay

Fine delay is accomplished using an analog delay cell and an on-chip 6 bit DAC (see Figure 2). The fine delay range is designed to be ~2X the coarse delay resolution.

Fine delay provides a total delay span of:

| | | | |
|---|---|---|---|
| LSB | 1 Fine LSB | = | 2.5 ps (see note) |
| | 2 Fine LSB | = | 5 ps |
| | 4 Fine LSB | = | 10 ps |
| | 8 Fine LSB | = | 20 ps |
| | 16 Fine LSB | = | 40 ps |
| MSP | 32 Fine LSB | = | 80 ps |

0 ns ≤ Fine Delay Range ≤ 157.5 ps.

*Note:* Because the transfer function is non-linear, some LSB steps could be as large as 5 ps.

Each channel has its own unique delay setting and may be programmed independently from all other channels. The fine delay of any channel will not affect the coarse delay of that channel, nor will it affect the overall delay of any other channel.

The propagation delay of a rising and falling edge will track each other over the entire span of fine delay. (Adding or subtracting fine delay will not cause pulse width distortion.)

### Fine Delay Select

The fine delay section may be selected or bypassed by a multiplexer (see Figure 2). If SFD (Select Fine Delay) is high, Fine Delay will be used. If SFD is low, Fine Delay will be bypassed.

| DAC Code | SFD | Delay |
|---|---|---|
| XXXXXX | 0 | Fine Delay Bypassed |
| 000000 | 1 | Minimum Delay (0.0 ns) |
| 111111 | 1 | Maximum Delay (157 ps) |

### Fine Delay DAC Outputs

DAC_FINE_(0–3) are analog voltage outputs from the on-board DACs which program the fine delay elements of each channel.

***DAC_FINE_(0-3) pins are for test purposes only. Nothing should be connected to these pins.***

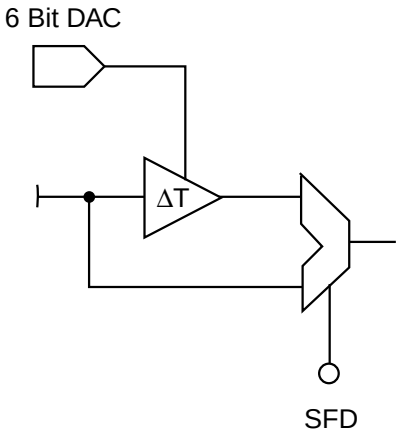



***Figure 2. Fine Delay Architecture***

## Circuit Description *(continued)*

### Falling Edge Adjustment

The falling edge of a signal may be adjusted to compensate for any system level pulse width distortion that may occur. Falling edge adjust (FEA) is accomplished using an analog delay cell and an on-chip 7 bit DAC (see Figure 3).

FEA may be bypassed completely by a multiplexer. Also, FEA affects only the propagation delay of the falling edge. It has no effect on the propagation delay of a rising edge.

Each channel has its own unique FEA setting and may be programmed independently from all other channels. The FEA of any channel will not affect the propagation delay of any other channel, nor will FEA affect the propagation delay of a rising edge.

| SFE | DAC Code | Falling Edge Delay | Resolution |
|---|---|---|---|
| 0 | XXXXXXX | FEA Bypassed | N/A |
| 1 | 0000000 | –250 ps | 2.5 ps |
| 1 | 1111111 | +250 ps | 2.5 ps |

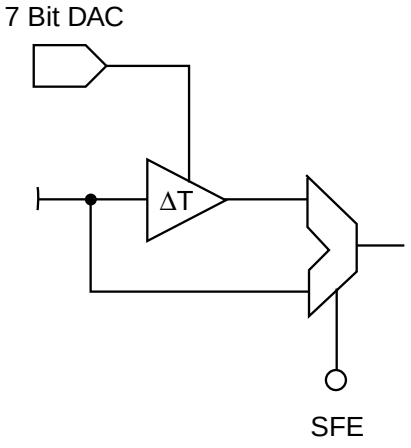



***Figure 3. Falling Edge Adjust Architecture***

There is a limitation on FEA range vs. pulse width.

| Input Pulse Width | FEA Range |
|---|---|
| 1.0 ns | ±250 ps |
| 900 ps | ±250 ps |
| 800 ps | ±250 ps |
| 700 ps | ±250 ps |
| 600 ps | ±200 ps |
| 500 ps | ±100 ps |

### Falling Edge Adjust DAC Outputs

DAC_FALL_(0–3) are analog voltage outputs from the on-board DACs which program the falling edge delay elements of each channel.

***DAC_FALL_(0-3) pins are for test purposes only. Nothing should be connected to these pins.***

### Thermal Monitor

The Edge629 features a thermal diode string consisting of 5 diodes as shown in Figure 4 below. This string allows accurate die temperature measurements.

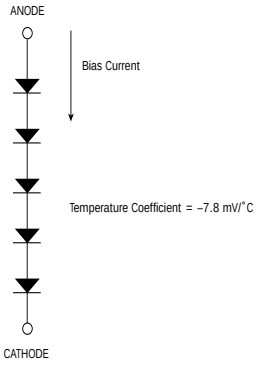



***Figure 4. Thermal Diode String***

When an external bias current of up to 100 µA is injected through the string, the voltage measured across the ANODE and CATHODE pins maps directly to the Edge629 junction temperature (see Figure 5).

## Circuit Description *(continued)*

### Programming

The Edge629 is programmed serially with 3 control lines:

SDI – serial data input
CS – chip select
UPDATE – register update

which are all synchronous with CK. With CS valid (high), rising edge of CK will load SDI into the 16 bit shift register.

With CS valid and UPDATE valid (high), CK high will make the selected latch go transparent. The falling edge of CK will then latch the data (see Figures 6 and 7).

Data and address information are combined in the 16 bit word. Bits 0–6 are used for data, bits 11–15 for address. Bits 11–14 select 1 of 16 destinations, bit 15, if high, selects all 16 locations to be loaded simultaneously (useful for preloading all registers to a default state).

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | |
|---|---|---|---|---|---|---|---|
| **Addr** | **LA** | **A3** | **A2** | **A1** | **A0** | | **Delay Function** |
| 0 | 0 | 0 | 0 | 0 | 0 | X | Channel 0, Coarse Delay |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | Channel 0, Fine Delay |
| 2 | 0 | 0 | 0 | 1 | 0 | 1 | Channel 0, Falling Edge Adjust |
| 3 | 0 | 0 | 0 | 1 | 1 | X | Not Used |
| 4 | 0 | 0 | 1 | 0 | 0 | X | Channel 1, Coarse Delay |
| 5 | 0 | 0 | 1 | 0 | 1 | 1 | Channel 1, Fine Delay |
| 6 | 0 | 0 | 1 | 1 | 0 | 1 | Channel 1, Falling Edge Adjust |
| 7 | 0 | 0 | 1 | 1 | 1 | X | Not Used |
| 8 | 0 | 1 | 0 | 0 | 0 | X | Channel 2, Coarse Delay |
| 9 | 0 | 1 | 0 | 0 | 1 | 1 | Channel 2, Fine Delay |
| A | 0 | 1 | 0 | 1 | 0 | 1 | Channel 2, Falling Edge Adjust |
| B | 0 | 1 | 0 | 1 | 1 | X | Not Used |
| C | 0 | 1 | 1 | 0 | 0 | X | Channel 3, Coarse Delay |
| D | 0 | 1 | 1 | 0 | 1 | 1 | Channel 3, Fine Delay |
| E | 0 | 1 | 1 | 1 | 0 | 1 | Channel 3, Falling Edge Adjust |
| F | 0 | 1 | 1 | 1 | 1 | X | Not Used |
| X | 1 | X | X | X | X | X | All Channels, All Functions |

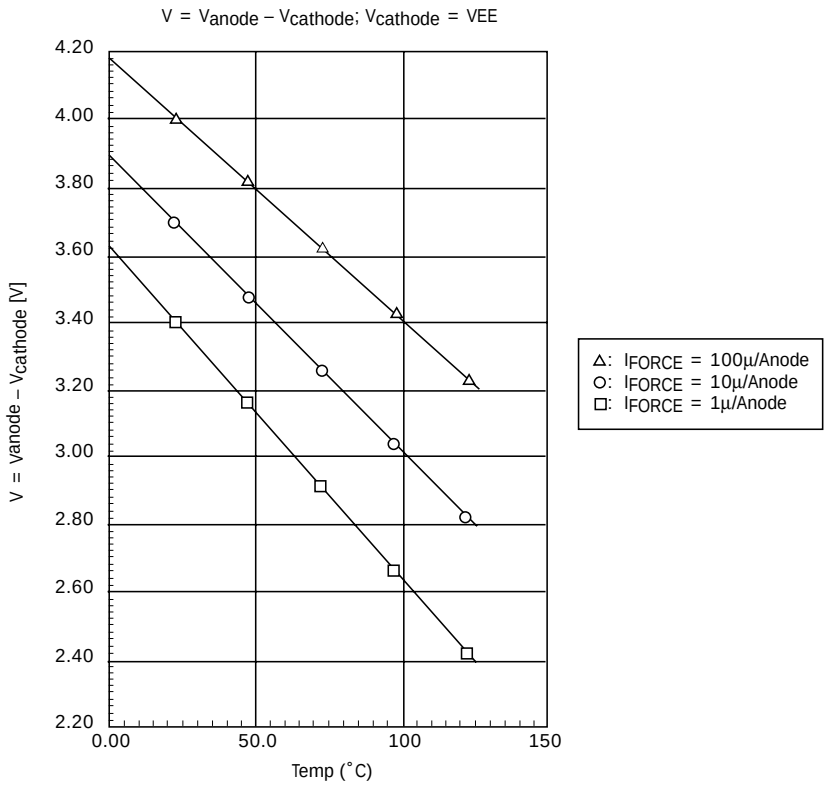



***Figure 5. Voltage vs. Temperature for Thermal Diode String***

## Circuit Description *(continued)*

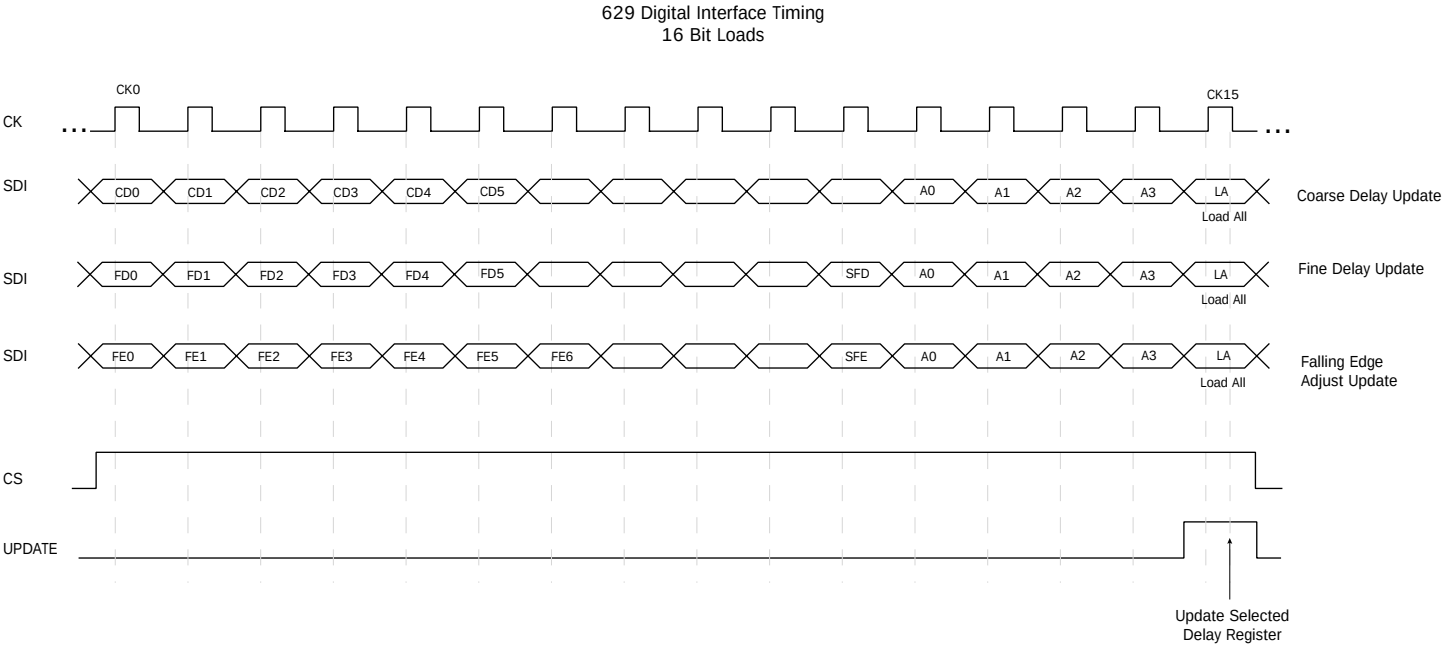



***Figure 6. Synchronous Loading***

## Circuit Description *(continued)*

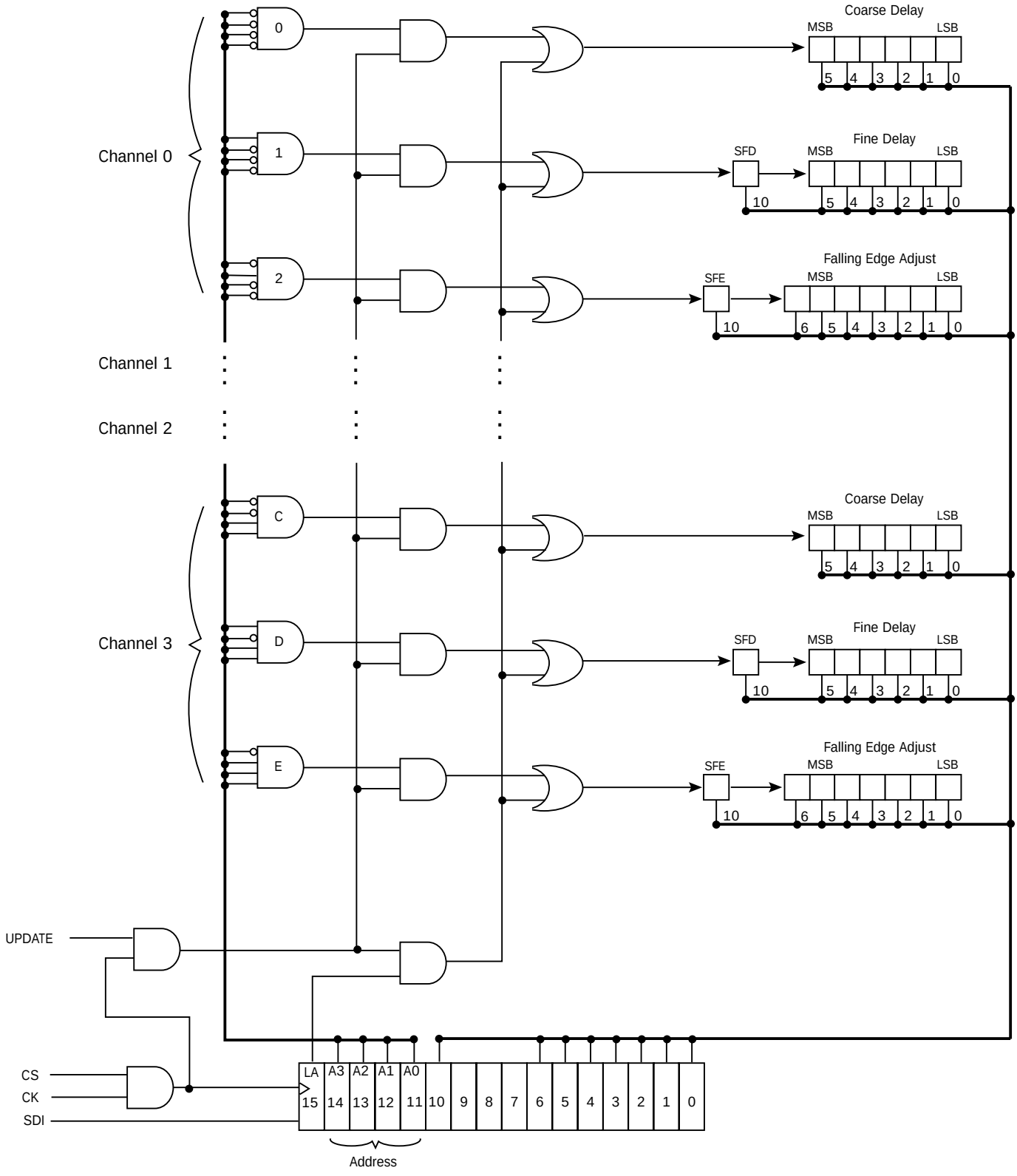



***Figure 7. Data Interface***

## Circuit Description *(continued)*

### Timing Inputs

IN/IN* and IN0/IN0* – IN3/IN3* are high speed differential inputs which require >300 mV of differential input voltage for reliable switching.

These inputs may receive differential input signals with amplitudes up to 3.3V. This wide range input voltage compliance allows CMOS signals to drive the Edge629 directly.

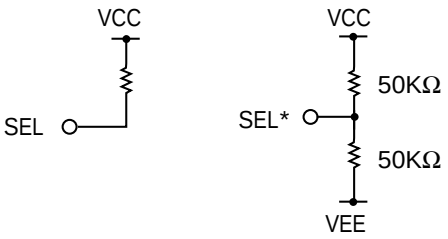
The inputs may go all the way up to VCC and still not cause any saturation. The Edge629 will operate at full performance under these input conditions.

***Do not leave any differential inputs floating as they will be in an indeterminate state. All unused inputs must be tied to either a high or low level. Connecting unused timing inputs to VCC is an acceptable method to make an input high. However, to make an input low, it must be connected to VEE +2.0V or higher.***

### Input Mux Select

Each delay channel can select its input from one of two sources. If Mux Select is high (SEL > SEL*), IN/IN* will be selected for all four channels. If Mux Select is low (SEL < SEL*), IN0/IN0* – IN3/IN3* will be selected for each channel.

| SEL/SEL* | Input Source |
|---|---|
| 0 | IN0/IN0* – IN3/IN3* |
| 1 | IN/IN* |




*SEL/SEL* have internal pull-up/pull-down resistors which, when left floating, place the chip in fanout mode.*

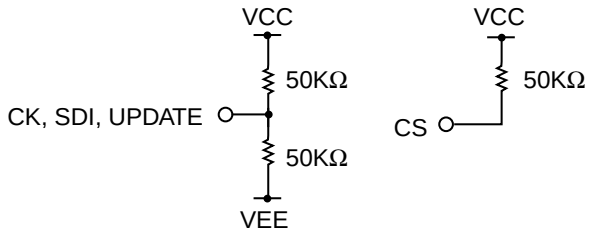
### Data Interface Digital Inputs

All data digital inputs are standard, single ended ECL inputs with $V_{bb}$ = –1.3V relative to VCC. However, all digital inputs may receive input signals anywhere between VCC and VEE. This wide input voltage compliance allows CMOS signals to program the Edge629 without causing saturation problems.

***All digital interface inputs are "3.3V rail to rail" CMOS compatible provided VCC = +3.3V and VEE = –2V.***

CK, SDI, and UPDATE all have an internal pull-down resistor network to establish a default condition of a logical 0 when left floating. CS has a large (~50 KΩ) internal pull-up resistor to VCC to establish a default condition of a logical 1 when left floating.

***For optimal performance, all data interface digital inputs should be static when the Edge 629 is actively delaying signals. (However, it is acceptable if CK continues to run.)***




### Timing Outputs

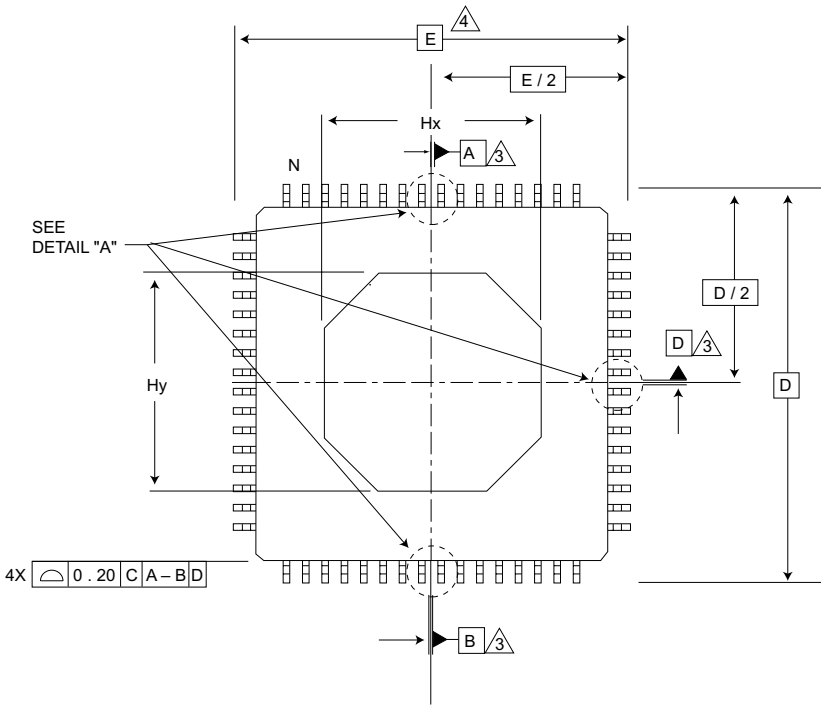
OUT0/OUT0* – OUT3/OUT3* are standard differential ECL open emitter outputs.

### Compensation Pins

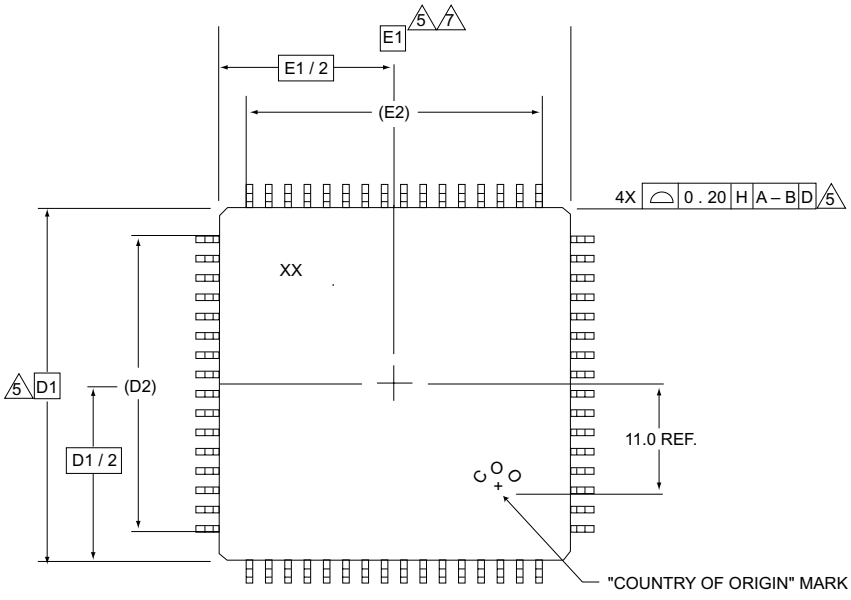
COMP0, COMP1, COMP2, and COMP3 are op amp compensation pins requiring external 100 pF capacitors to VEE.

**64-Pin TPQ4**
**10 mm x 10 mm**

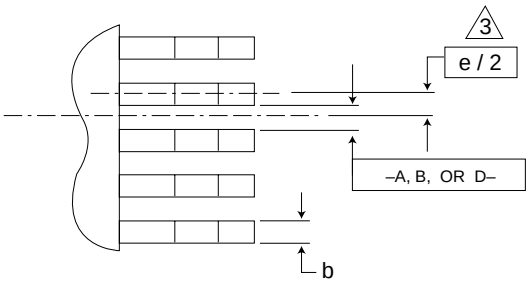
TOP VIEW



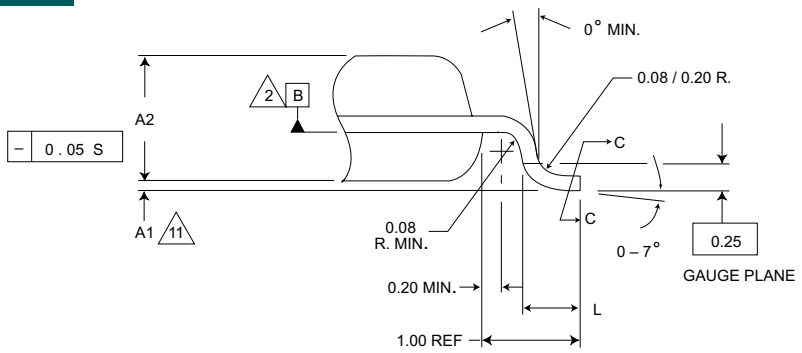

BOTTOM VIEW



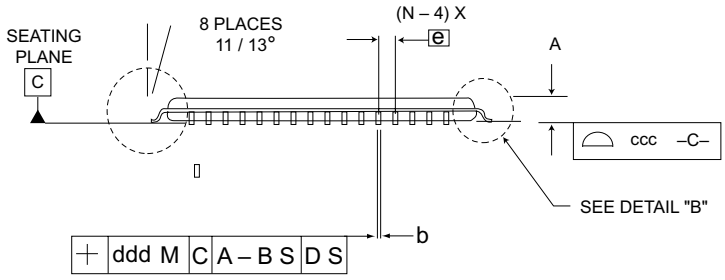
## Package Infor mation *(continued)*

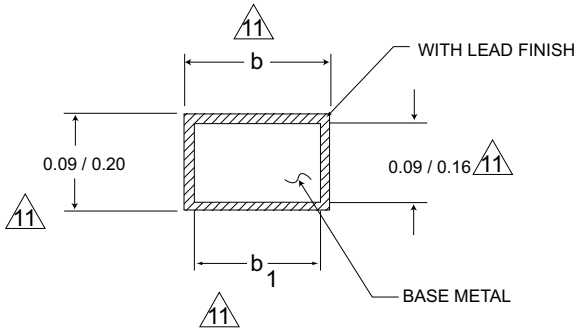



DETAIL "A"




DETAIL "B"




SECTION "C–C"

Notes:

1. All dimensioning and tolerancing conform to ASME Y14.5-1994.
2. Datum plane H, located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.
3. Datums A-B and D to be determined at centerline between leads where leads exit plastic body at datum plane H.
4. To be determined at seating plane C.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable mold protrusion is 0.254 mm on D1 and E1 dimensions.
6. "N" is the total number of terminals.
7. These dimensions to be determined at datum plane H.
8. The top of package is smaller than the bottom of package by 0.10 millimeters.
9. Dimension b does not include Dambar protrusion. Allowable Dambar protrusionshall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot.
10. Controlling dimension: Millimeter.
11. Maximum allowable die thickness to be assembled in this package family is 0.38 millimeters.
12. This outline conforms to JEDEC standard outline MS 026, variations BG, BH, BJ.

**JDEC Variation**
**All Dimensions in Millimeters**

| | BJ | | | | |
|---|---|---|---|---|---|
| **Sym** | **Min** | **Nom** | **Max** | **Note** | **Comments** |
| A | – | – | 1.60 | | Height above PCB |
| A1 | 0.05 | 0.10 | 0.15 | | PCB Clearance |
| A2 | 1.35 | 1.40 | 1.45 | | Body Thickness |
| D | | 12.00 BSC | | 4 | |
| D1 | | 10.00 BSC | | 7,8 | Package Body Length |
| E | | 12.00 BSC | | 4 | |
| E1 | | 10.00 BSC | | 7,8 | Package Body Width |
| L | 0.45 | 0.60 | 0.75 | | |
| Hx | 5.70 | 6.00 | 6.30 | | Heat Slug Width |
| Hy | 5.70 | 6.00 | 6.30 | | Heat Slug Length |
| M | 0.14 | – | – | | |
| N | | 64 | | | Pin Count |
| e | | 0.50 BSC | | | Lead Pitch |
| b | 0.17 | 0.22 | 0.27 | 9 | PCB Pad Dimension |
| b1 | 0.17 | 0.20 | 0.23 | | PCB Pad Dimension |
| ccc | – | – | 0.08 | | |
| ddd | – | – | 0.08 | | |

## Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Total Power Supply | VCC – VEE | 4.2 | 5.2 | +5.5 | V |
| Junction Temperature | TJ | 0 | | +100 | ˚C |

## Absolute Maximum Ratings

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Power Supply | VCC – VEE | 0 | | 7.0 | V |
| Voltage on any Digital Input Pin | | VEE – 0.5 | | VCC + 0.5 | V |
| Voltage on any Analog Input Pin | | VEE – 0.5 | | VCC + 0.5 | V |
| Output Current | | –50 | | | mA |
| Storage Temperature | TS | –65 | | +150 | ˚C |
| Junction Temperature | TJ | | | +150 | ˚C |
| Soldering Temperature (5 seocnds, .25" from the pin) | TSOL | | | +260 | ˚C |

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these, or any other conditions beyond those listed, is not implied. Exposure to absolute maximum conditions for extended periods may affect device reliability.

## DC Characteristics

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **Timing Inputs (IN / IN*, IN0 / IN0* – IN3 / IN3*)** | | | | | |
| Differential Input High Voltage | IN – IN* | .3 | | VCC – VEE | V |
| Differential Input Low Voltage | IN* – IN | .3 | | VCC – VEE | V |
| Input High Common Mode Range | VIH | VEE + 2.0 | | VCC | V |
| Input Low Common Mode Range | VIL | VEE + 2.0 | | VIH – .3 | V |
| Input High Current | IIH | –100 | | +100 | µA |
| Input Low Current | IIL | –100 | | +100 | µA |
| **Select Input (SEL / SEL*)** | | | | | |
| Differential Input High Voltage | SEL – SEL* | .3 | | VCC – VEE | V |
| Differential Input Low Voltage | SEL* – SEL | .3 | | VCC – VEE | V |
| Input High Common Mode Range | VIH | VEE + 2.0 | | VCC | V |
| Input Low Common Mode Range | VIL | VEE + 2.0 | | VIH – .3 | V |
| Input High Current | IIH | | | 250 | µA |
| Input Low Current | IIL | | | 250 | µA |
| **Programming Inputs (CK, UPDATE, CS, SDI)** | | | | | |
| Input High Voltage | VIH | VCC – 1.1 | | VCC | V |
| Input Low Voltage | VIL | VEE + 2.0 | | VCC – 1.5 | V |
| Input High Current | IIH | | | 250 | µA |
| Input Low Current | IIL | | | 250 | µA |
| **Digital Outputs** | | | | | |
| Digital Output High Voltage | OUT – OUT* | 600 | 690 | | mV |
| Digital Output Low Voltage | OUT* – OUT | 600 | 690 | | mV |
| Output Common Mode Range | $\frac{\text{OUT + OUT*}}{2}$ | VCC – 1.5 | VCC – 1.3 | VCC – 1.1 | V |
| Output Current | Iout | | | 30 | mA |
| **Power Supply Current** | | | | | |
| VCC – VEE = 4.2V | IEE | 35 | 561 | 900 | mA |
| VCC – VEE = 5.2V | IEE | 35 | 604 | 900 | mA |
| VCC – VEE = 5.5V | IEE | 35 | 613 | 900 | mA |

Test Conditions (unless other specified): “Recommended Operating Conditions.”

## AC Characteristics

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **Timing Inputs / Outputs** | | | | | |
| Minimum Propagation Delay (Note 2) | | | | | |
| IN to OUT (0,3) | Tpd Min | 1.282 | 1.357 | 1.432 | ns |
| IN0, 3 to OUT (0,3) | Tpd Min | 1.406 | 1.481 | 1.556 | ns |
| Rising Edge / Falling Edge Propagation Delay Variation (FEA disabled) | $\|Tpd^+ - Tpd^-\|$ | | TBD | | ps |
| Channel-to-Channel Skew (Note 2) | | | | | |
| IN to OUT (0,3) | Tskew1 | | 25 | 45 | ps |
| IN (0,3) to OUT (0,3) | Tskew2 | | 30 | 50 | ps |
| Programmable Delay (Note 2) | | | | | |
| Coarse Delay | Tspan_Coarse | 5.0 | 5.5 | 6.5 | ns |
| Fine Delay | Tspan_Fine | 110 | 145 | 180 | ps |
| Falling Edge Adjust (SFE = 1) (Note 1) | FEA | ±200 | ±250 | 300 | ps |
| Maximum Programmable Delay Step Size | | | | | |
| Coarse Delay | Tstep_Coarse | | 95 | 110 | ps |
| Fine Delay | Tstep_Fine | | 5 | 7 | ps |
| Falling Edge Adjust | Tstep_FEA | | 5 | 7 | ps |
| Maximum Operating Frequency (FEA Enabled) | Fmax | 1.0 | | | GHz |
| Maximum Operating Frequency (FEA Disabled) | Fmax | 1.5 | | | GHz |
| Minimum Pulse Width (at outputs) | PW min | 330 | | | ps |
| Output Rise and Fall Times (20% - 80%) | Tr / Tf | | 110 | 150 | ps |
| Temperature Coefficient | $\Delta Tpd / \Delta T$ | | | | |
| CD = Min, FD & FEA Disabled | | | 2.4 | | ps/° C |
| CD = Max, FD & FEA Disabled | | | 13.3 | | ps/° C |
| CD & FD = Min, FEA Disabled | | | 3.3 | | ps/° C |
| CD & FD = Max, FEA Disabled | | | 15.1 | | ps/° C |
| CD, FD, & FEA = Min | | | 5.2 | | ps/° C |
| CD, FD, & FEA = Max | | | 18.8 | | ps/° C |
| **Total Timing Error** | | | | | |
| $\Delta$Tpd vs. Frequency | | | <10 | | ps |
| Channel-to-Channel Crosstalk | | | | | |
| $\Delta$Tpd vs. Duty Cycle | | | TBD | | ps |
| Jitter | | | | | |

Test Conditions (unless otherwise specified): "Recommended Operating Conditions."

*Note 1:* Tested with an input pulse = 50 ns. This parameter is guaranteed by characterization for input pulse widths ≥700 ps.

*Note 2:* Coarse Delay = 0, Fine Delay and Falling Edge Adjust disabled. Case Temperature = 50°C.

## AC Characteristics *(continued)*

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **Data Interface** | | | | | |
| Set Up Time | | | | | |
| SDI to CK ↑ | Tsu | 10 | | | ns |
| CS to CK ↑ | Tsu | 10 | | | ns |
| UPDATE to CK ↓ | Tsu | 20 | | | ns |
| Hold Time | | | | | |
| CK ↑ to SDI | Th | 4 | | | ns |
| CK ↑ to CS | Th | 4 | | | ns |
| CK ↓o UPDATE | Th | 4 | | | ns |
| Minimum Pulse Widths | | | | | |
| CK High | | 13 | | | ns |
| CK Low | | 13 | | | ns |
| CK Period | T | 30 | | | ns |
| DAC Settling Time | | | TBD | | |

Test Conditions (unless otherwise specified): "Recommended Operating Conditions."

AC Characteristics are guaranteed by design and characterization. Not production tested.

## Ordering Information

| Model Number | Package |
|---|---|
| E629AXF | 10mm x 10 mm TQFP w/Exposed Heat Slug on Top |
| D629 | Die Form |
| EVM629AXF | Edge629 Evaluation Board |

## Contact Information

Semtech Corporation
High-Performance Division
10021 Willow Creek Rd., San Diego, CA 92131
Phone: (858)695-1808 FAX (858)695-2633