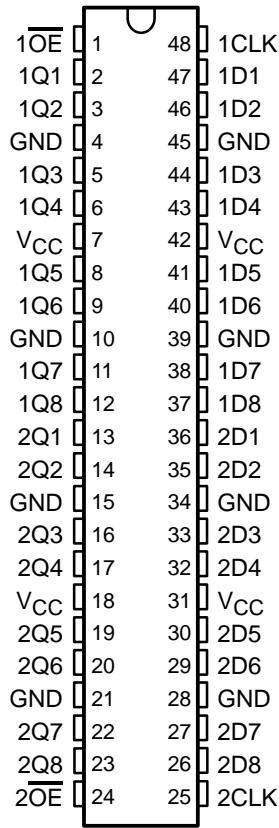


- **Members of the Texas Instruments Widebus™ Family**
- **Output Ports Have Equivalent 22- $\Omega$  Series Resistors, So No External Resistors Are Required**
- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )**
- **Support Unregulated Battery Operation Down to 2.7 V**
- **Typical  $V_{OLP}$  (Output Ground Bounce) <0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$**
- **$I_{off}$  and Power-Up 3-State Support Hot Insertion**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Distributed  $V_{CC}$  and GND Pins Minimize High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Latch-Up Performance Exceeds 500 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

SN54LVTH162374 . . . WD PACKAGE  
 SN74LVTH162374 . . . DGG OR DL PACKAGE  
 (TOP VIEW)



## description

The 'LVTH162374 devices are 16-bit edge-triggered D-type flip-flops with 3-state outputs designed for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK), the Q outputs of the flip-flop take on the logic levels set up at the D inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$  does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The outputs, which are designed to source or sink up to 12 mA, include equivalent 22- $\Omega$  series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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 On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

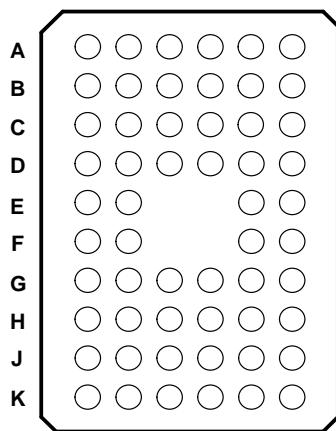
**description (continued)**

When  $V_{CC}$  is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

**GQL PACKAGE  
(TOP VIEW)**

1 2 3 4 5 6

**terminal assignments**

	1	2	3	4	5	6
A	1 $\overline{OE}$	NC	NC	NC	NC	1CLK
B	1Q2	1Q1	GND	GND	1D1	1D2
C	1Q4	1Q3	$V_{CC}$	$V_{CC}$	1D3	1D4
D	1Q6	1Q5	GND	GND	1D5	1D6
E	1Q8	1Q7			1D7	1D8
F	2Q1	2Q2			2D2	2D1
G	2Q3	2Q4	GND	GND	2D4	2D3
H	2Q5	2Q6	$V_{CC}$	$V_{CC}$	2D6	2D5
J	2Q7	2Q8	GND	GND	2D8	2D7
K	2 $\overline{OE}$	NC	NC	NC	NC	2CLK

NC – No internal connection

**ORDERING INFORMATION**

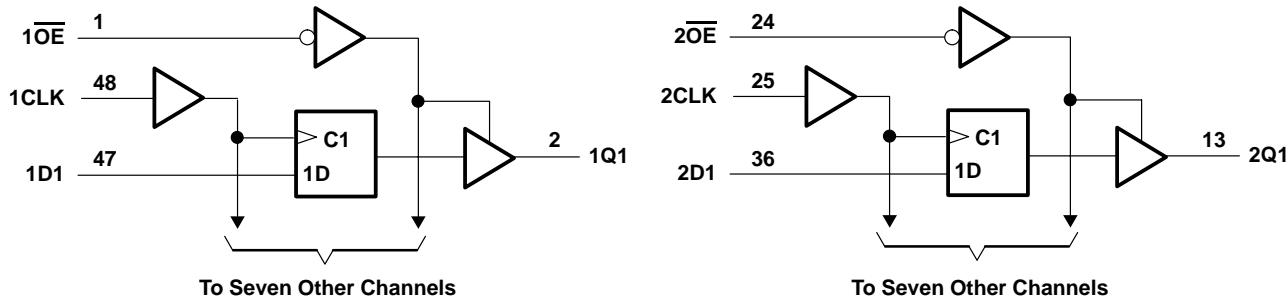
TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74LVTH162374DL	LVTH162374
		Tape and reel	SN74LVTH162374DLR	
	TSSOP – DGG	Tape and reel	SN74LVTH162374DGGR	LVTH162374
	VFBGA – GQL	Tape and reel	SN74LVTH162374KR	LL2374
–55°C to 125°C	CFP – WD	Tube	SNJ54LVTH162374WD	SNJ54LVTH162374WD

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

**FUNCTION TABLE  
(each flip-flop)**

INPUTS			OUTPUT Q
OE	CLK	D	
L	↑	H	H
L	↑	L	L
L	H or L	X	$Q_0$
H	X	X	Z

## logic diagram (positive logic)



Pin numbers shown are for the DGG, DL, and WD packages.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .  
 3. The package thermal impedance is calculated in accordance with JEDEC 51-7.

#### **recommended operating conditions (see Note 4)**

		SN54LVTH162374		SN74LVTH162374		UNIT	
		MIN	MAX	MIN	MAX		
V <sub>CC</sub>	Supply voltage	2.7	3.6	2.7	3.6	V	
V <sub>IH</sub>	High-level input voltage	2		2		V	
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	V	
V <sub>I</sub>	Input voltage		5.5		5.5	V	
I <sub>OH</sub>	High-level output current		-12		-12	mA	
I <sub>OL</sub>	Low-level output current		12		12	mA	
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10	10	ns/V	
Δt/ΔV <sub>CC</sub>	Power-up ramp rate		200	200		μs/V	
T <sub>A</sub>	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**SN54LVTH162374, SN74LVTH162374****3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS****WITH 3-STATE OUTPUTS**

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	SN54LVTH162374			SN74LVTH162374			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 2.7 V, I <sub>I</sub> = -18 mA			-1.2			-1.2	V
V <sub>OH</sub>	V <sub>CC</sub> = 3 V, I <sub>OH</sub> = -12 mA		2		2			V
V <sub>OL</sub>	V <sub>CC</sub> = 3 V, I <sub>OL</sub> = 12 mA			0.8			0.8	V
I <sub>I</sub>	V <sub>CC</sub> = 0 or 3.6 V, V <sub>I</sub> = 5.5 V			10			10	μA
	Control inputs V <sub>CC</sub> = 3.6 V, V <sub>I</sub> = V <sub>CC</sub> or GND			±1			±1	
	Data inputs V <sub>CC</sub> = 3.6 V	V <sub>I</sub> = V <sub>CC</sub>		1			1	
		V <sub>I</sub> = 0		-5			-5	
I <sub>off</sub>	V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> = 0 to 4.5 V						±100	μA
I <sub>I(hold)</sub>	V <sub>CC</sub> = 3 V	V <sub>I</sub> = 0.8 V		75			75	μA
		V <sub>I</sub> = 2 V		-75			-75	
	V <sub>CC</sub> = 3.6 V‡, V <sub>I</sub> = 0 to 3.6 V						500 -750	
I <sub>OZH</sub>	V <sub>CC</sub> = 3.6 V, V <sub>O</sub> = 3 V			5			5	μA
I <sub>OZL</sub>	V <sub>CC</sub> = 3.6 V, V <sub>O</sub> = 0.5 V			-5			-5	μA
I <sub>OZPU</sub>	V <sub>CC</sub> = 0 to 1.5 V, V <sub>O</sub> = 0.5 V to 3 V, OE = don't care			±100*			±100	μA
I <sub>OZPD</sub>	V <sub>CC</sub> = 1.5 V to 0, V <sub>O</sub> = 0.5 V to 3 V, OE = don't care			±100*			±100	μA
I <sub>CC</sub>	V <sub>CC</sub> = 3.6 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND	Outputs high		0.19			0.19	mA
		Outputs low		5			5	
		Outputs disabled		0.19			0.19	
ΔI <sub>CC</sub> §	V <sub>CC</sub> = 3 V to 3.6 V, One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND			0.2			0.2	mA
C <sub>i</sub>	V <sub>I</sub> = 3 V or 0			3			3	pF
C <sub>o</sub>	V <sub>O</sub> = 3 V or 0			9			9	pF

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

		SN54LVTH162374		SN74LVTH162374		UNIT	
		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V			
		MIN	MAX	MIN	MAX		
f <sub>clock</sub>	Clock frequency	160		160		160	MHz
t <sub>w</sub>	Pulse duration, CLK high or low	3		3.3		3	ns
t <sub>su</sub>	Setup time, data before CLK↑	2.8		3.2		1.8	2
t <sub>h</sub>	Hold time, data after CLK↑	High or low	1.2	0.5	0.8	0.1	ns

**SN54LVTH162374, SN74LVTH162374  
3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS  
WITH 3-STATE OUTPUTS**

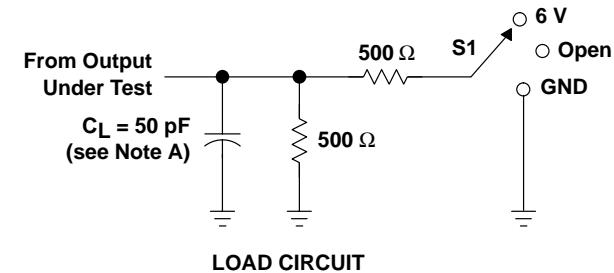
SCBS262J – JULY 1993 – REVISED DECEMBER 2001

**switching characteristics over recommended operating free-air temperature range,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 1)**

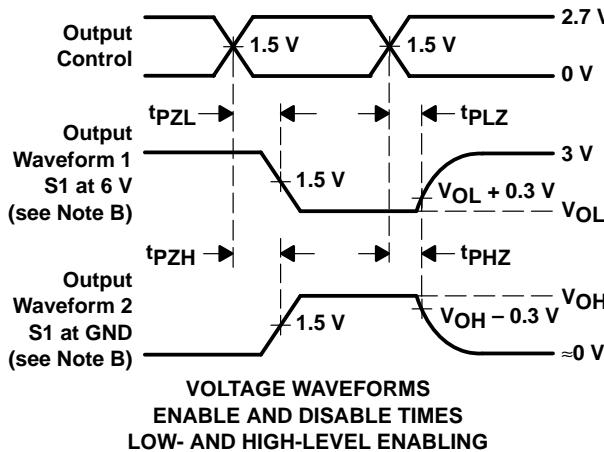
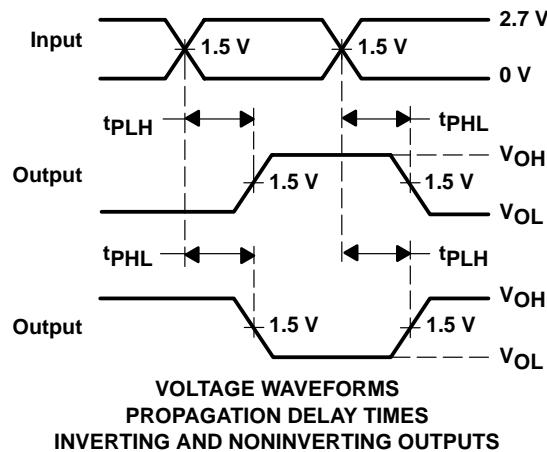
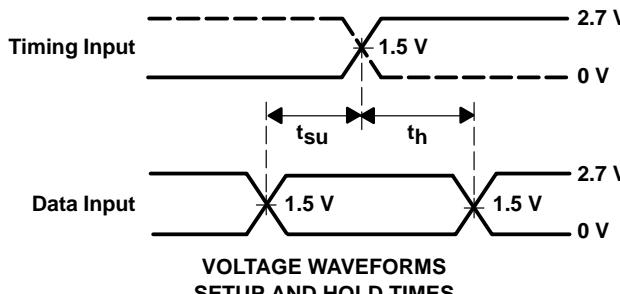
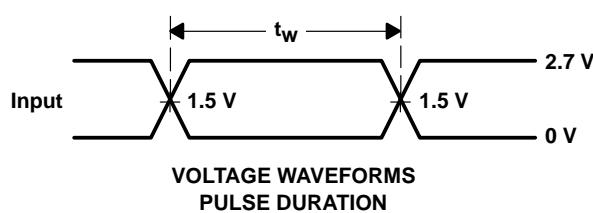
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH162374				SN74LVTH162374				UNIT
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 2.7 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 2.7 \text{ V}$		
			MIN	MAX	MIN	MAX	MIN	TYPE <sup>†</sup>	MAX	MIN	MAX
$f_{max}$			160		160		160		160		MHz
$t_{PLH}$	CLK	Q	1.4	6.6		7.4	2	3.4	5.3	6.2	ns
$t_{PHL}$			1.4	5.8		6	2.2	3.3	4.9	5.1	
$t_{PZH}$	$\overline{OE}$	Q	1	6.6		7.4	1.8	3.5	5.6	6.9	ns
$t_{PZL}$			1.4	6		6.8	1.8	3.5	4.9	6	
$t_{PHZ}$	$\overline{OE}$	Q	1	6.6		7.4	2.4	4.2	5.4	5.7	ns
$t_{PLZ}$			1.4	6		6	2	3.8	5	5.1	
$t_{sk(o)}$									0.5		ns

<sup>†</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

## PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



NOTES: A.  $C_L$  includes probe and jig capacitance.

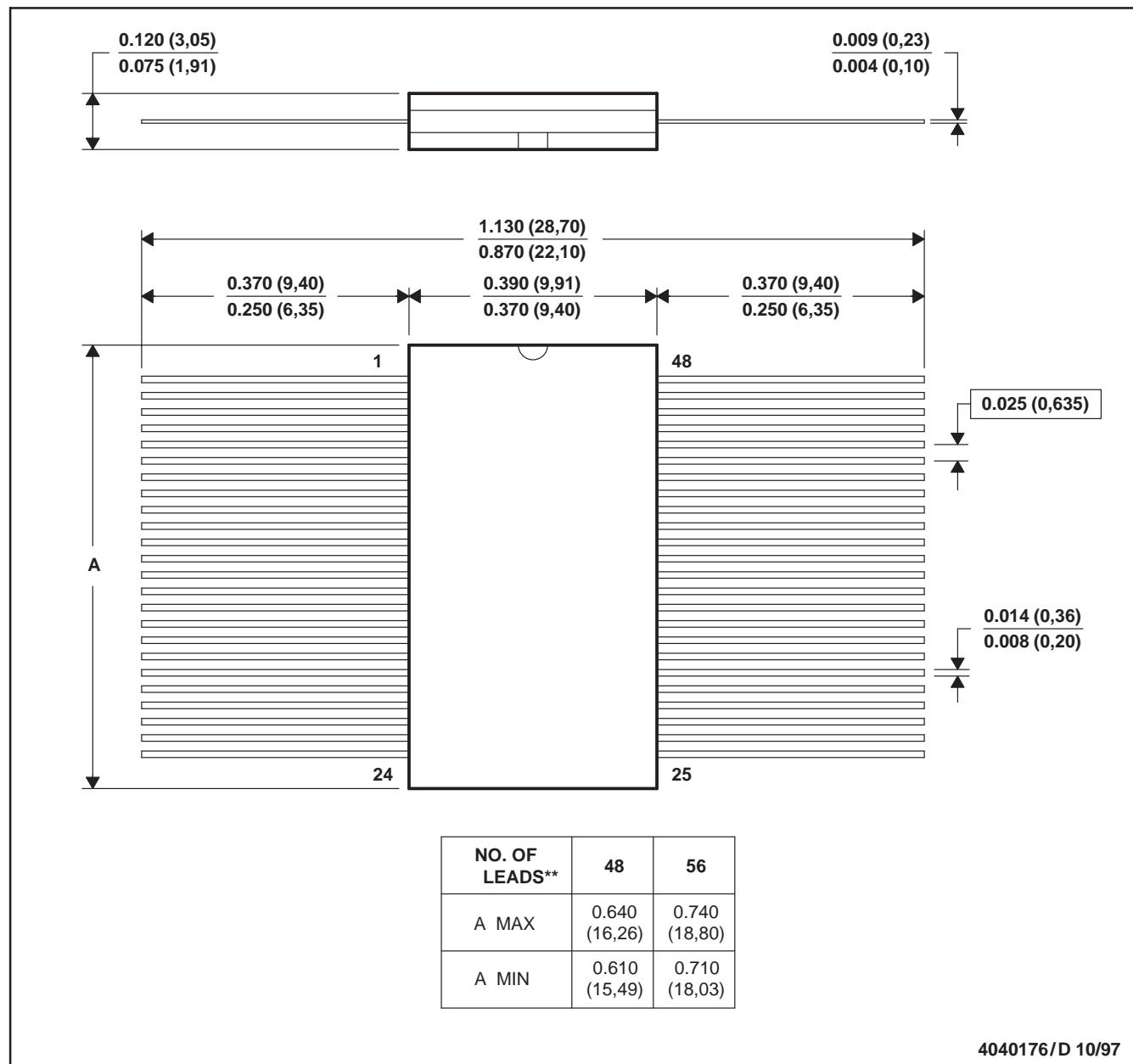
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

WD (R-GDFP-F\*\*)

CERAMIC DUAL FLATPACK

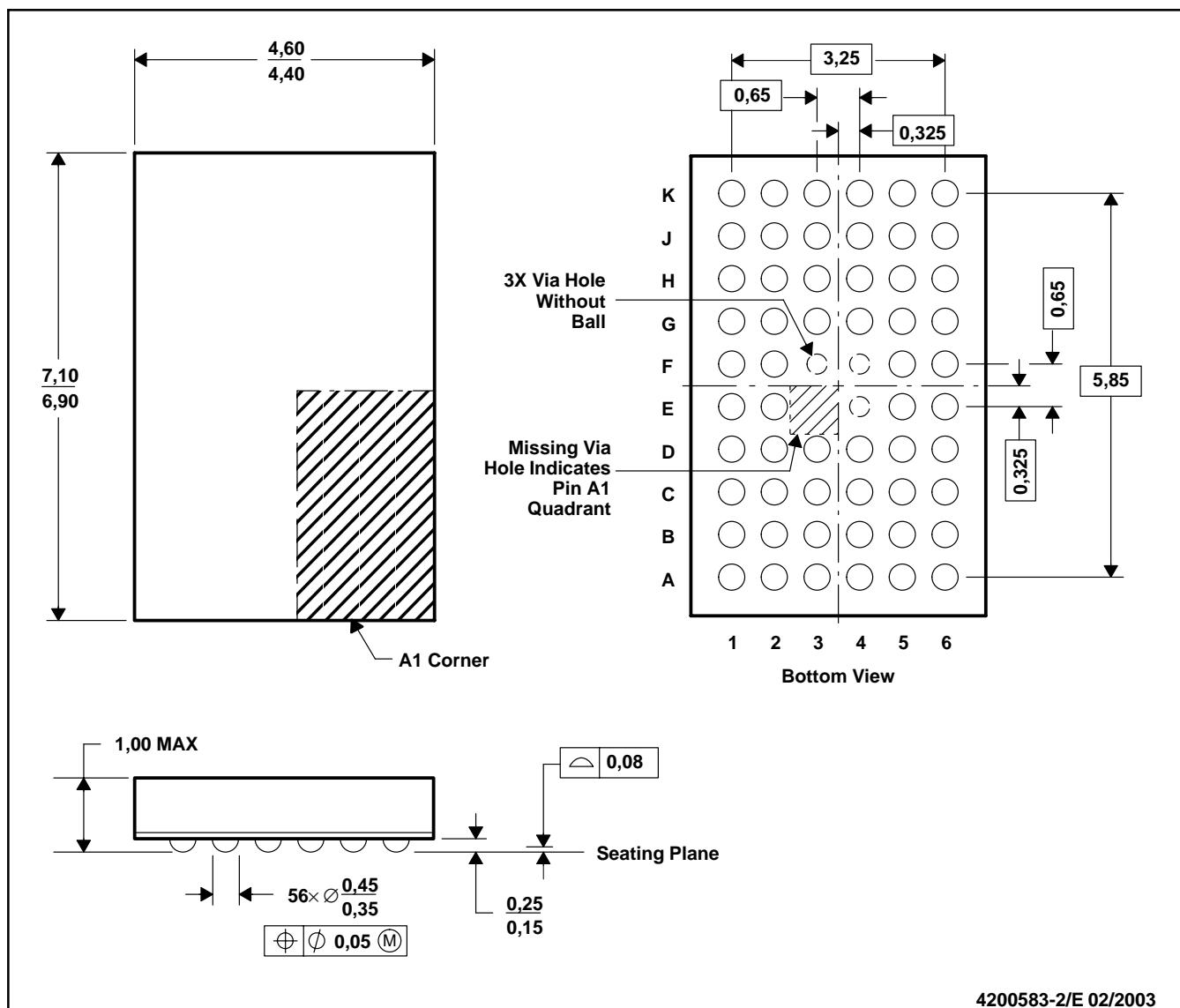
48 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification only.  
 E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA  
 GDFP1-F56 and JEDEC MO-146AB

## GQL (R-PBGA-N56)

## PLASTIC BALL GRID ARRAY



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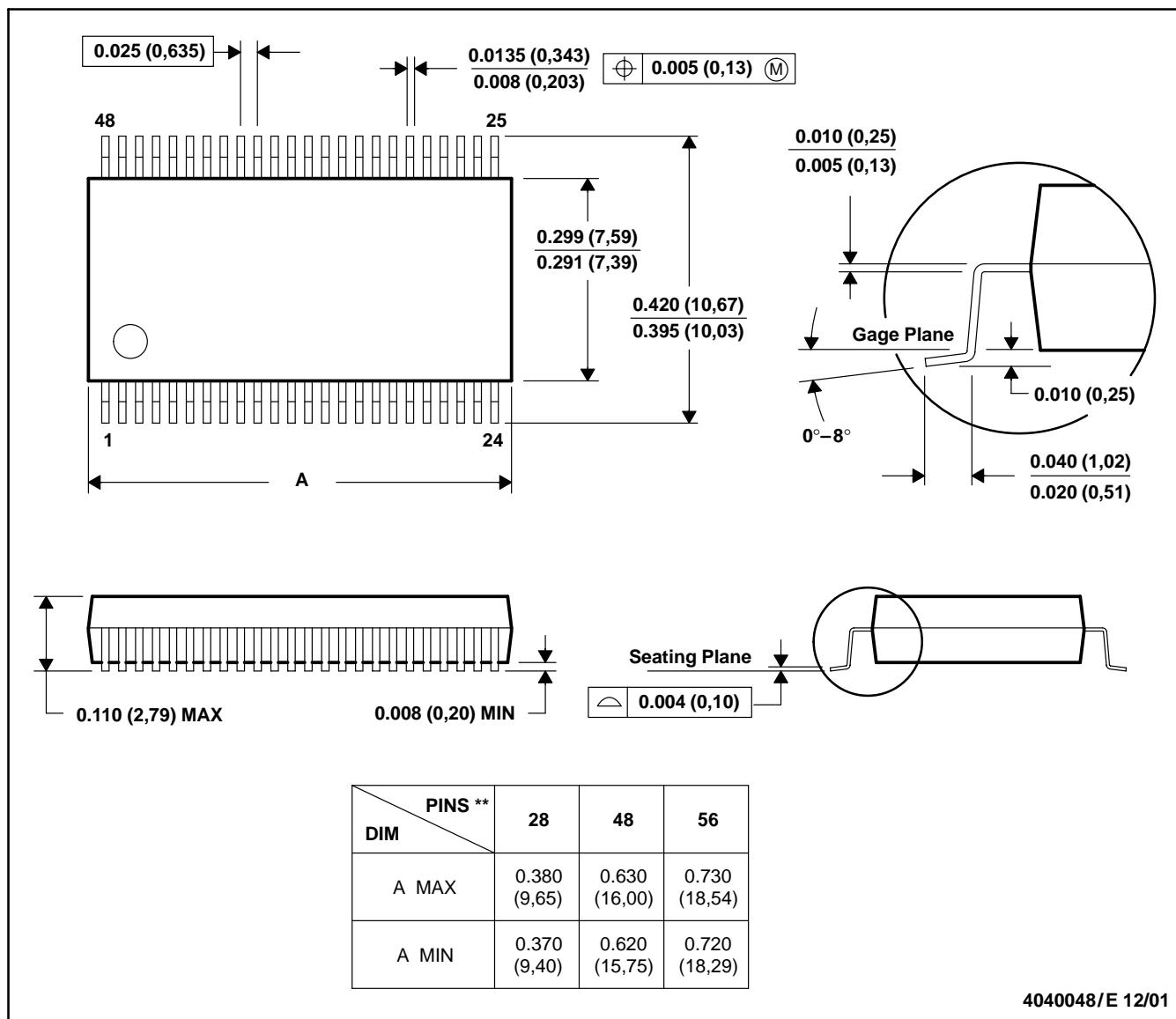
- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - MicroStar Junior™ BGA configuration
  - Falls within JEDEC MO-225 variation BA.
  - This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

MicroStar Junior is a trademark of Texas Instruments.

## DL (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



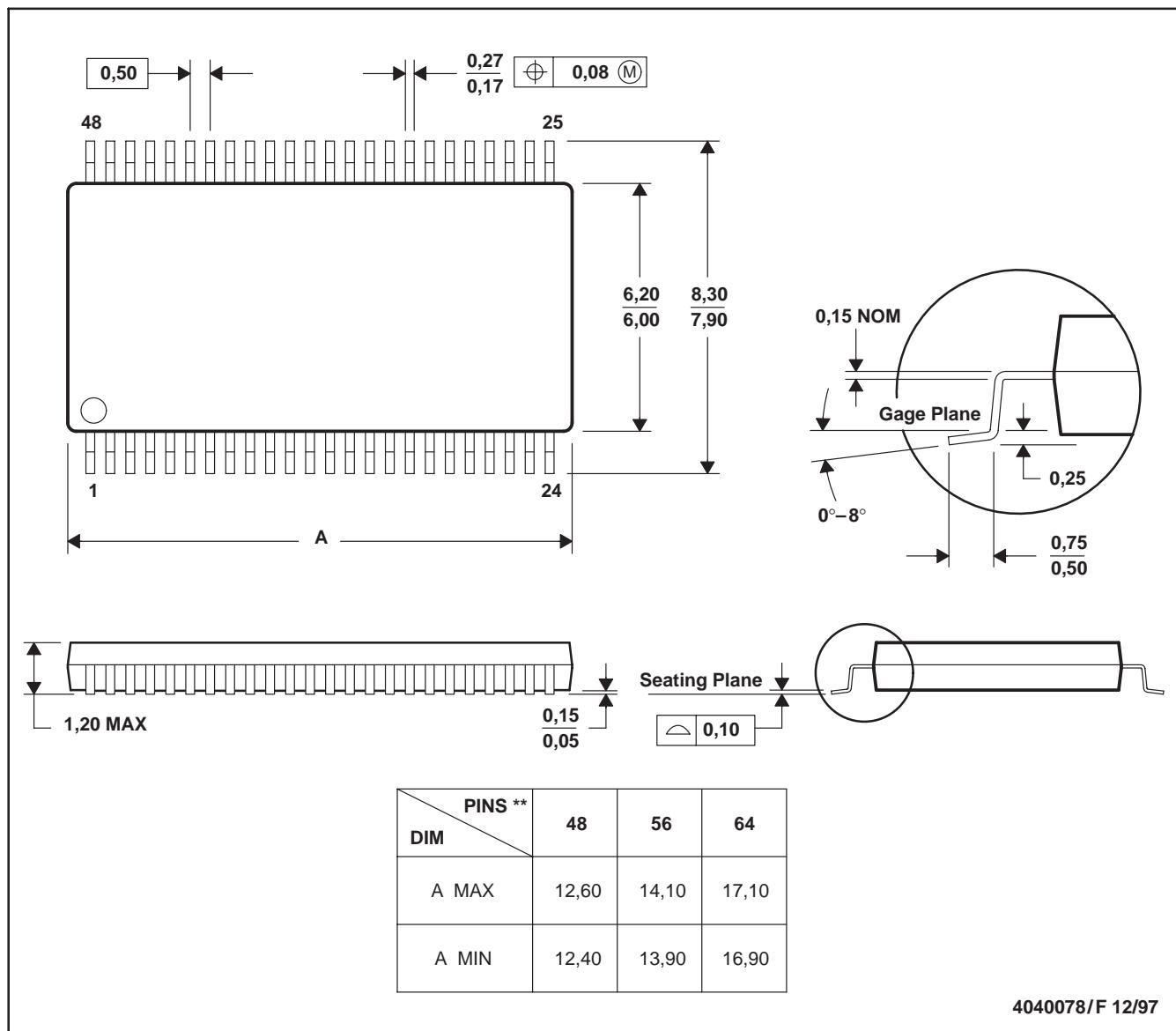
4040048/E 12/01

- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MO-118

## DGG (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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