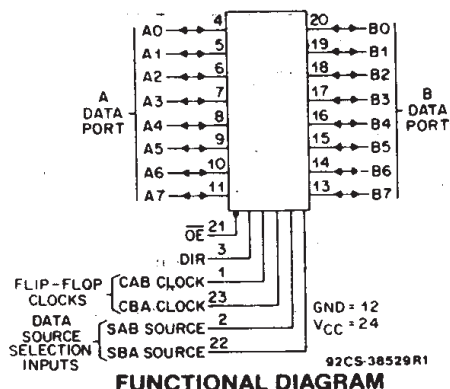


CD54/74AC646, CD54/74AC648 CD54/74ACT646, CD54/74ACT648



Data sheet acquired from Harris Semiconductor
SCHS293



Octal-Bus Transceiver/Registers, 3-State

CD54/74AC/ACT646 - Non-Inverting

CD54/74AC/ACT648 - Inverting

Type Features:

- Buffered inputs
- Typical propagation delay:
5.3 ns @ $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$

Family Features:

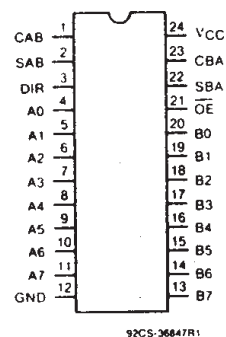
- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST[®]/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24\text{-mA}$ output drive current
 - Fanout to 15 FAST[®] ICs
 - Drives 50-ohm transmission lines

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

The RCA CD54/74AC646 and CD54/74AC648 and the CD54/74ACT646 and CD54/74ACT648 3-state, octal-bus transceiver/registers use the RCA ADVANCED CMOS technology. The CD54/74AC648 and CD54/74ACT648 have inverting outputs. The CD54/74AC646 and CD54/74ACT646 have non-inverting outputs. These devices are bus transceivers with D-type flip-flops which act as internal storage registers on the LOW-to-HIGH transition of either CAB or CBA clock inputs. Output Enable (OE) and Direction (DIR) inputs control the transceiver functions. Data present at the high-impedance output can be stored in either register or both but only one of the two buses can be enabled as outputs at any one time. The Select controls (SAB and SBA) can multiplex stored and transparent (real time) data. The Direction control determines which data bus will receive data when the Output Enable (OE) is LOW. In the high-impedance mode (Output Enable HIGH), A data can be stored in one register and B data can be stored in the other register. The clocks are not gated with the Direction (DIR) and Output Enable (OE) terminals; data at the A or B terminals can be clocked into the storage flip-flops at any time.

The CD74AC/ACT646 and CD74AC/ACT648 are supplied in 24-lead dual-in-line narrow-body plastic packages (EN suffix) and in 24-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to $+85^\circ\text{C}$); and Extended Industrial/Military (-55 to $+125^\circ\text{C}$).

The CD54AC/ACT646 and CD54AC/ACT648, available in chip form (H suffix), are operable over the -55 to $+125^\circ\text{C}$ temperature range.



TERMINAL ASSIGNMENT

CD54/74AC646, CD54/74AC648

CD54/74ACT646, CD54/74ACT648

FUNCTION TABLE

INPUTS						DATA I/O#		OPERATION OR FUNCTION	
OE	DIR	CAB	CBA	SAB	SBA	A0 THRU A7	B0 THRU B7	646	648
X	X		X	X	X	Input	Not specified	Store A, B unspecified	Store A, B unspecified
X	X	X		X	X	Not specified	Input	Store B, A unspecified	Store B, A unspecified
H	X			X	X	Input	Input	Store A and B Data	Store A and B Data
H	X	H or L	H or L	X	X			Isolation, hold storage	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time $\bar{B}$ Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus	Stored $\bar{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time $\bar{A}$ Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Stored $\bar{A}$ Data to B Bus

#The data output functions may be enabled or disabled by various signals at the OE and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

To prevent excess currents in the High-Z modes, all I/O terminals should be terminated with 10 kΩ resistors.

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE (V_{CC})	-0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V)	±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V)	±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V)	±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND})	±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -55$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE (T_A)	-55 to $+125^\circ\text{C}$
STORAGE TEMPERATURE (T_{stg})	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum	+265 $^\circ\text{C}$
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only	+300 $^\circ\text{C}$

*For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC} *: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I , V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	$^\circ\text{C}$
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

CD54/74AC646, CD54/74AC648

CD54/74ACT646, CD54/74ACT648

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS		TEST CONDITIONS		V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C						UNITS
					+25		-40 to +85		-55 to +125		
		V _I (V)	I _O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V _{IH}			1.5 3 5.5	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	V
Low-Level Input Voltage	V _{IL}			1.5 3 5.5	— — —	0.3 0.9 1.65	— — —	0.3 0.9 1.65	— — —	0.3 0.9 1.65	V
High-Level Output Voltage	V _{OH}	V _{IH} or V _{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
			-0.05	3	2.9	—	2.9	—	2.9	—	
			-0.05	4.5	4.4	—	4.4	—	4.4	—	
			-4	3	2.58	—	2.48	—	2.4	—	
			-24	4.5	3.94	—	3.8	—	3.7	—	
		#, * {	-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V _{OL}	V _{IH} or V _{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
			0.05	3	—	0.1	—	0.1	—	0.1	
			0.05	4.5	—	0.1	—	0.1	—	0.1	
			12	3	—	0.36	—	0.44	—	0.5	
			24	4.5	—	0.36	—	0.44	—	0.5	
		#, * {	75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I _I	V _{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current	I _{OZ}	V _{IH} or V _{IL} V _O = V _{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI	I _{CC}	V _{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

Technical Data

CD54/74AC646, CD54/74AC648 CD54/74ACT646, CD54/74ACT648

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS		TEST CONDITIONS		V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C						UNITS
					+25		-40 to +85		-55 to +125		
		V _I (V)	I _O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V _{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage	V _{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage	V _{OH}	V _{IH} or V _{IL} # , * {	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V _{OL}	V _{IH} or V _{IL} # , * {	0.05	4.5	—	0.1	—	0.1	—	0.1	V
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I _i	V _{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current	I _{OZ}	V _{IH} or V _{IL} V _O = V _{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI	I _{CC}	V _{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI _{CC}	V _{CC} -2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C. 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
CAB, CBA	1.25
SAB, SBA	1.2
DIR	0.67
OE	1.17
An, Bn	0.4

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

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CD54/74AC646, CD54/74AC648

CD54/74ACT646, CD54/74ACT648

PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V _{cc} (V)	AMBIENT TEMPERATURE (T _A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Max. Frequency	f _{max}	1.5	11	—	10	—	MHz
		3.3*	101	—	89	—	
		5†	143	—	125	—	
Setup Time Data to Clock	t _{su}	1.5	27	—	31	—	ns
		3.3	3.1	—	3.5	—	
		5	2.2	—	2.5	—	
Hold Time Data to Clock	t _h	1.5	2	—	2	—	ns
		3.3	2	—	2	—	
		5	2	—	2	—	
Clock Pulse Width	t _w	1.5	44	—	50	—	ns
		3.3	4.9	—	5.6	—	
		5	3.5	—	4	—	

*3.3 V: min. is @ 3 V

†5 V: min is @ 4.5 V

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays:							
Store A Data to B Bus	t _{PLH}	1.5	—	154	—	169	ns
Store B Data to A Bus	t _{PHL}	3.3*	4.8	17.1	4.7	18.9	
646		5†	3.5	12.3	3.4	13.5	
Store $\bar{A}$ Data to B Bus	t _{PLH}	1.5	—	154	—	169	ns
Store $\bar{B}$ Data to A Bus	t _{PHL}	3.3	4.8	17.1	4.7	18.9	
648		5	3.5	12.3	3.4	13.5	
A Data to B Bus	t _{PLH}	1.5	—	125	—	138	ns
B Data to A Bus	t _{PHL}	3.3	4	14	3.9	15.4	
646		5	2.8	10	2.8	11	
$\bar{A}$ Data to B Bus	t _{PLH}	1.5	—	125	—	138	ns
$\bar{B}$ Data to A Bus	t _{PHL}	3.3	4	14	3.9	15.4	
648		5	2.8	10	2.8	11	
Select to Data	t _{PLH}	1.5	—	136	—	150	ns
646	t _{PHL}	3.3	4.3	15.3	4.2	16.8	
		5	3.1	10.9	3	12	
Select to Data	t _{PLH}	1.5	—	136	—	150	ns
648	t _{PHL}	3.3	4.3	15.3	4.2	16.8	
		5	3.1	10.9	3	12	
3-State Enabling/ Disabling Time	t _{PZL}	1.5	—	154	—	169	ns
Bus to Output or	t _{PZH}	3.3	5.2	18.4	5.1	20.2	
Register to Output	t _{PLZ}	5	3.5	12.3	3.4	13.5	
	t _{PHZ}						
Power Dissipation Capacitance	C _{PD} §	—	150 Typ.		150 Typ.		pF
Min. (Valley) During Switching of Other Outputs (Output Under Test Not Switching)	V _{OH} V _{OHV} See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) During Switching of Other Outputs (Output Under Test Not Switching)	V _{OL} V _{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C _I	—	—	10	—	10	pF
3-State Output Capacitance	C _O	—	—	15	—	15	pF

*3.3 V: min. is @ 3.6 V

max. is @ 3 V

†5 V: min. is @ 5.5 V

max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per package.P_D = V_{CC}² C_{PD} f_i + Σ (V_{CC}² C_L f_o) where f_i = input frequencyf_o = output frequencyC_L = output load capacitanceV_{CC} = supply voltage.

CD54/74AC646, CD54/74AC648

CD54/74ACT646, CD54/74ACT648

PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Max. Frequency	f _{max}	5*	125	—	110	—	MHz
Setup Time Data to Clock	t _{su}	5	2.2	—	2.5	—	ns
Hold Time Data to Clock	t _h	5	2	—	2	—	ns
Clock Pulse Width	t _w	5	3.9	—	4.5	—	ns

*5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Store A Data to B Bus Store B Data to A Bus 646	t _{PLH} t _{PHL}	5*	4	14.1	3.9	15.5	ns
Store $\bar{A}$ Data to B Bus Store $\bar{B}$ Data to A Bus 648	t _{PLH} t _{PHL}	5	4	14.1	3.9	15.5	ns
A Data to B Bus B Data to A Bus 646	t _{PLH} t _{PHL}	5	3.2	11.4	3.1	12.5	ns
$\bar{A}$ Data to B Bus $\bar{B}$ Data to A Bus 648	t _{PLH} t _{PHL}	5	3.2	11.4	3.1	12.5	ns
Select to Data 646	t _{PLH} t _{PHL}	5	3.7	13.2	3.6	14.5	ns
Select to Data 648	t _{PLH} t _{PHL}	5	4	14.1	3.9	15.5	ns
3-State Enabling/ Disabling Time Bus to Output or Register to Output	t _{PZL} t _{PZH} t _{PLZ} t _{PHZ}	5	4	14.1	3.9	15.5	ns
Power Dissipation Capacitance	C _{PD} §	—	150 Typ.		150 Typ.		pF
Min. (Valley) During Switching of Other Outputs (Output Under Test Not Switching)	V _{OH} V _{OHV} See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) During Switching of Other Outputs (Output Under Test Not Switching)	V _{OL} V _{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C _I	—	—	10	—	10	pF
3-State Output Capacitance	C _O	—	—	15	—	15	pF

*5 V: min. is @ 5.5 V
max. is @ 4.5 V§C_{PD} is used to determine the dynamic power consumption, per package.

$$P_D = C_{PD} V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_o) + V_{CC} \Delta I_{CC} \text{ where } f_i = \text{input frequency}$$

$$f_o = \text{output frequency}$$

$$C_L = \text{output load capacitance}$$

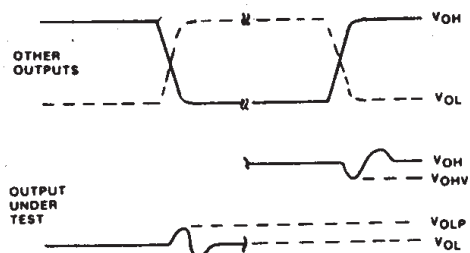
$$V_{CC} = \text{supply voltage.}$$

Technical Data

CD54/74AC646, CD54/74AC648

CD54/74ACT646, CD54/74ACT648

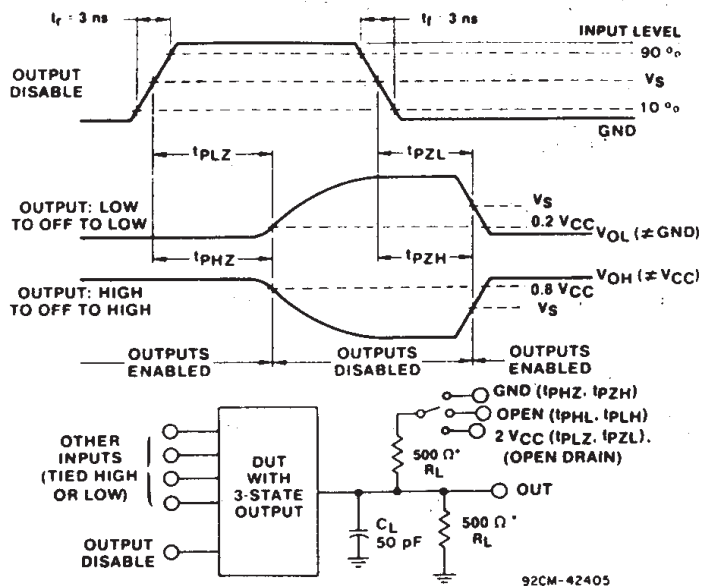
PARAMETER MEASUREMENT INFORMATION



- NOTES:
1. V_{OHV} and V_{OLP} are measured with respect to a ground reference near the output under test.
 2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS:
 $PRR \leq 1 \text{ MHz}$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$, SKEW 1 ns .
 3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED.
 IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH $0.1 \mu\text{F}$ CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

92CS-42406

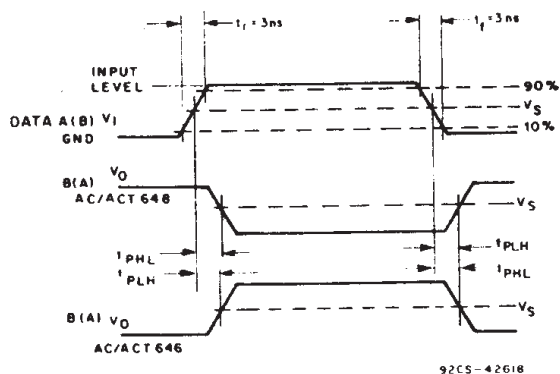
Fig. 1 - Simultaneous switching transient waveforms.



*FOR AC SERIES ONLY: WHEN $V_{CC} = 1.5 \text{ V}$, $R_L = 1 \text{ k}\Omega$

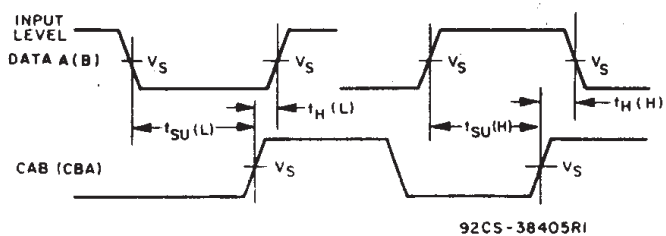
92CM-42405

Fig. 2 - Three-state propagation delay waveforms and test circuit.



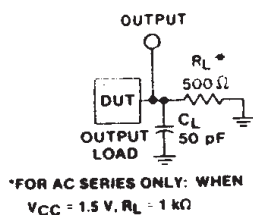
92CS-42618

Fig. 3 - Propagation delay times.



92CS-38405RI

Fig. 4 - Data setup and hold times.



92CS-42389

Fig. 5 - Test circuit.

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	$0.5 V_{CC}$	1.5 V
Output Switching Voltage, V_S	$0.5 V_{CC}$	$0.5 V_{CC}$

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD74AC646M	Obsolete	Production	SOIC (DW) 24	-	-	Call TI	Call TI	-55 to 125	AC646M
CD74AC646M96	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC646M
CD74AC646M96.A	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC646M
CD74ACT646M	Obsolete	Production	SOIC (DW) 24	-	-	Call TI	Call TI	-55 to 125	ACT646M
CD74ACT646M96	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT646M
CD74ACT646M96.A	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT646M

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

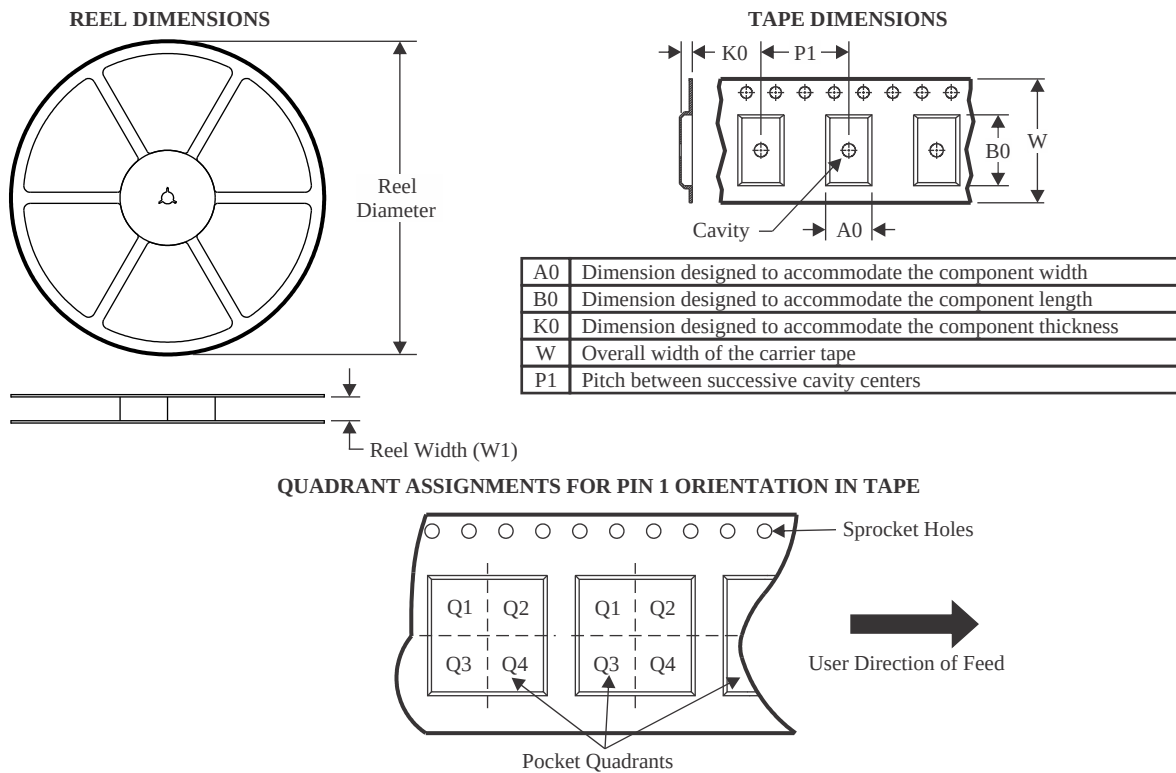
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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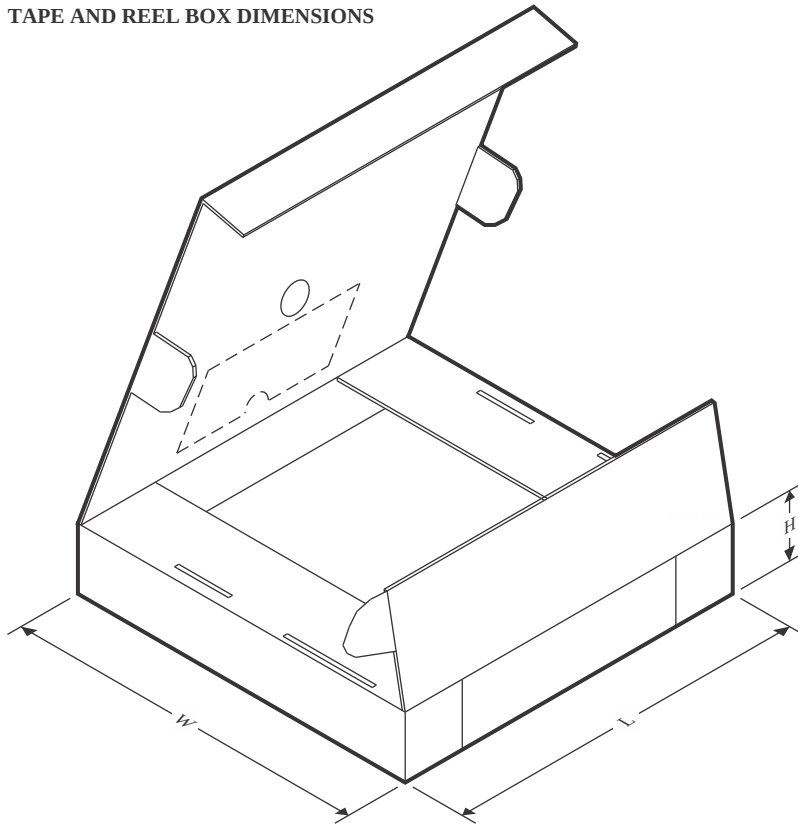
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC646M96	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
CD74ACT646M96	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

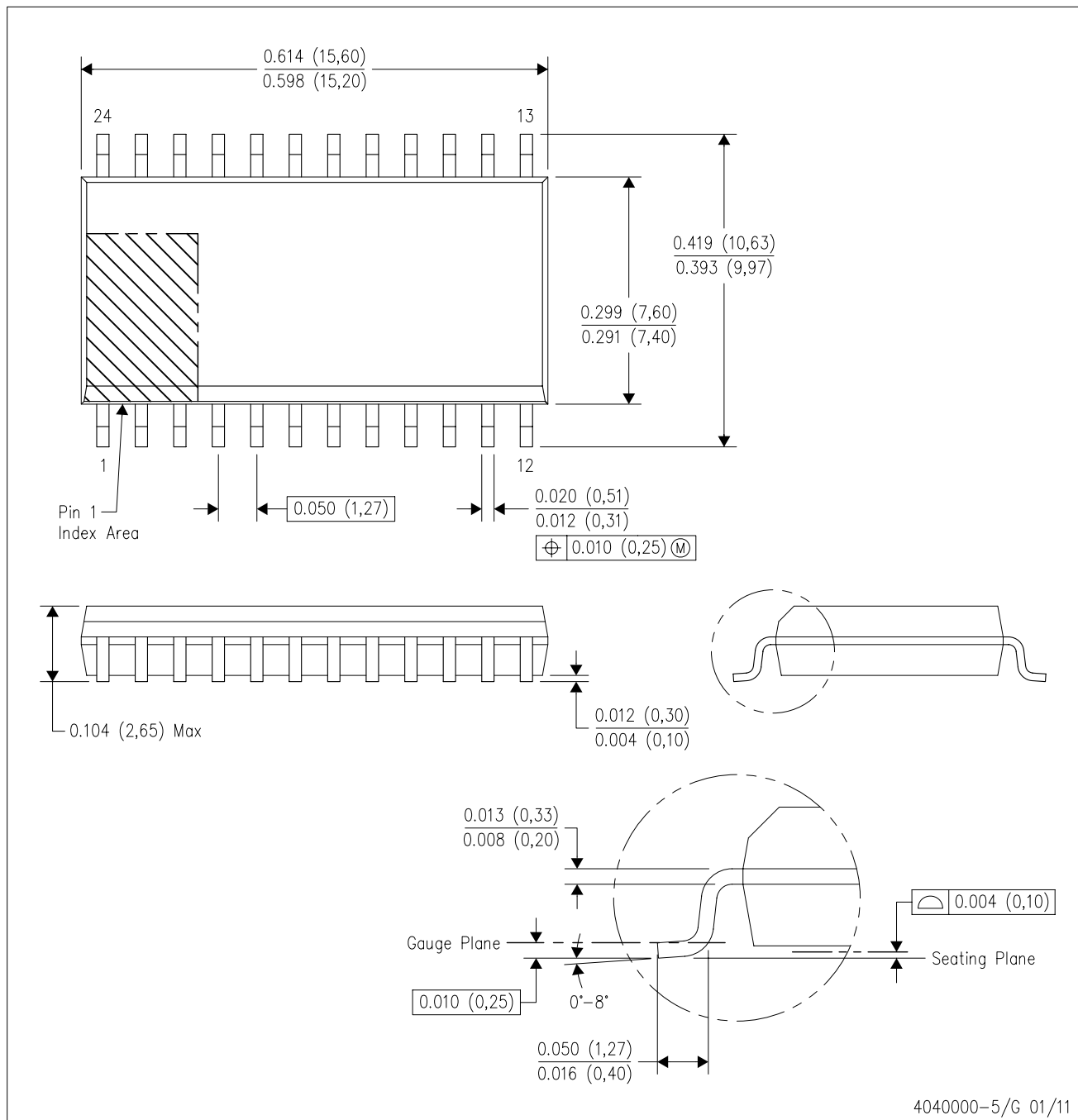


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC646M96	SOIC	DW	24	2000	350.0	350.0	43.0
CD74ACT646M96	SOIC	DW	24	2000	350.0	350.0	43.0

DW (R-PDSO-G24)

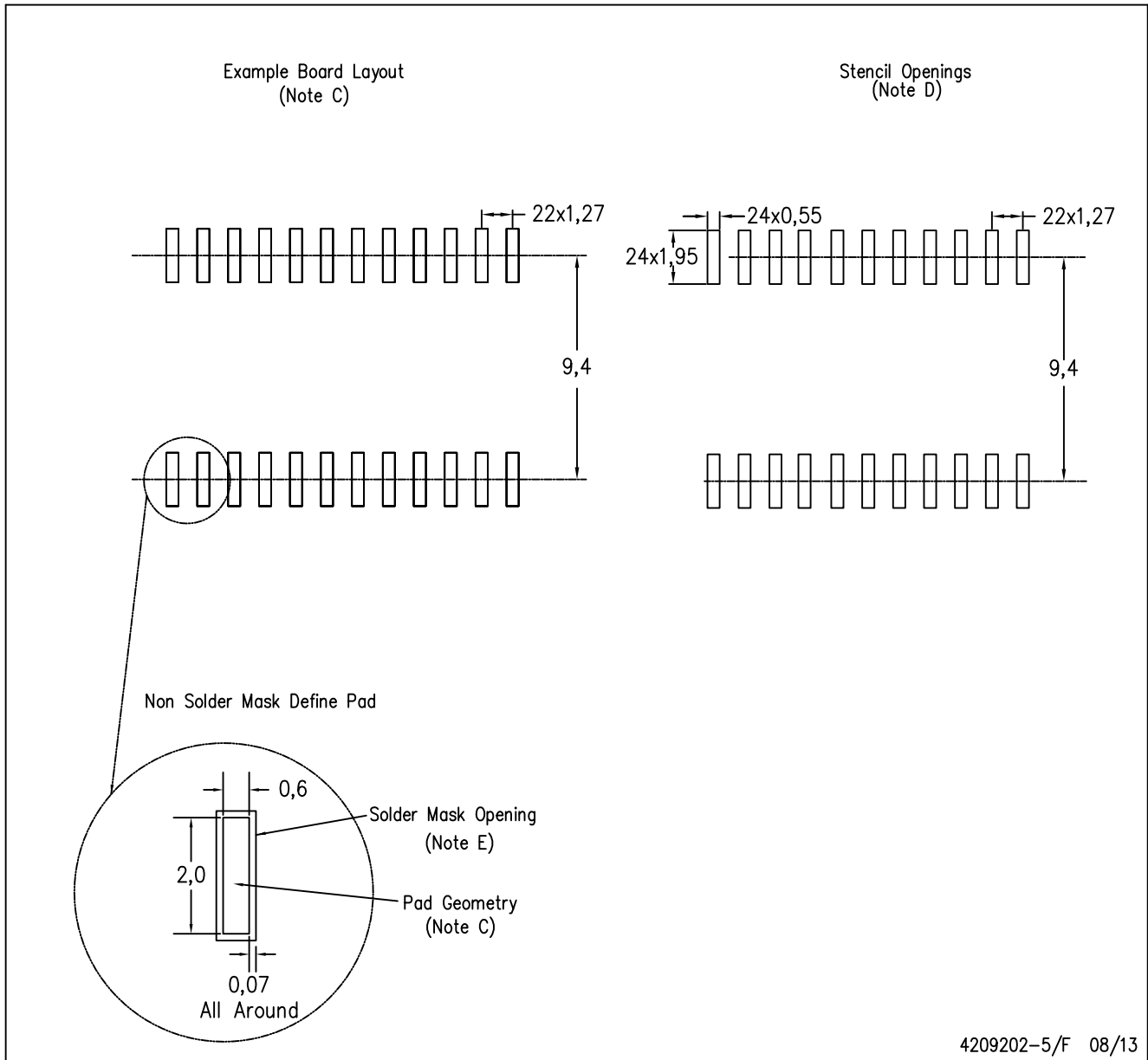
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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