



L3234
L3235N

HIGHLY INTEGRATED SLIC KIT TARGETED TO PABX AND KEY SYSTEM APPLICATIONS

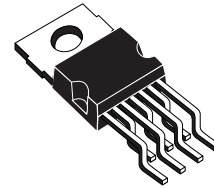
- HIGHLY INTEGRATED SUBSCRIBER LINE INTERFACE KIT FOR PABX AND KEY SYSTEM APPLICATIONS
- IMPLEMENTS ALL KEY ELEMENTS OF THE BORSCHT FUNCTION
- INTEGRATED ZERO CROSSING BALANCED RINGING INJECTION ELIMINATES EXTERNAL RELAY AND CENTRALISED RINGING GENERATOR
- ZERO NOISE INJECTED ON ADJACENT LINES DURING RINGING SEQUENCE
- LOW POWER IN STANDBY AND ACTIVE MODES
- BATTERY FEED WITH PROGRAMMABLE LIMITING CURRENT
- PARALLEL LATCHED DIGITAL INTERFACE
- SIGNALLING FUNCTIONS (OFF HOOK, GND-KEY)
- LOW NUMBER OF EXTERNAL COMPONENTS
- INTEGRATED THERMAL PROTECTION
- INTEGRATED OVER CURRENT PROTECTION
- 0°C TO 70°C: L3234/L3235N
- -40°C TO 85°C: L3234T/L3235NT

DESCRIPTION

The L3234/L3235N is a highly integrated SLIC KIT targeted to PABX and key system applications

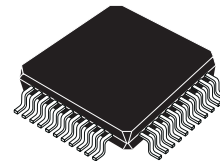
The kit integrates the majority of functions required to interface a telephone line. The L3234/L3235N implements the main features of the broths function:

- Battery Feed (Balanced Mode)
- Ringing Injection
- Signalling Detection
- Hybrid Function



HEPTAWATT

ORDERING NUMBER: L3234



TQFP44

ORDERING NUMBER: L3235N

The Kit comprises 2 devices, the L3234 ringing injector fabricated in Bipolar in 140V Technology.

Its function is to amplify and inject in balanced mode with zero crossing the ringing signal. The device requires an external positive supply of 100V and a low level sinusoid of approx. 950mVrms. The L3235N Line Feeder is integrated in 60V Bipolar Technology. The L3235N provides battery feed to the line with programmable current limitation. The two to four wire voice frequency signal conversion is implemented by the L3235N and line terminating and balance impedances are externally programmable. The L3234/L3235N kit is designed for low power dissipation. In a short loop condition the extra power is dissipated on an external transistor. The Kit is controlled by five wire parallel bus and interfaces easily to all the STLC5046 and STLC5048 CODECs. In Kit with STLC5048 (see fig 1) the line impedance synthesis and echo canceling are performed inside the CODEC.



L3234

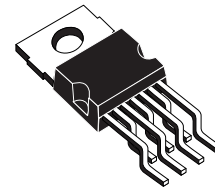
Solid State Ringing Injector

DESCRIPTION

The L3234 is a monolithic integrated circuit which is part of a kit of solid state devices for the subscriber line interface. The L3234 sends a ringing signal into a two wires analog telephone line in balanced mode. The AC ringing signal amplitude is up to 60Vrms, and for that purpose a positive supply voltage of +100V shall be available on the subscriber card.

The L3234 receives a low amplitude ringing signal (950mVrms) and provide the voltage/current amplification (60Vrms/70mA) when the enable input is active ($CS \geq 2V$). In disable mode ($CS \leq 0.8V$) the power consumption of the chip is very low (<14mW).

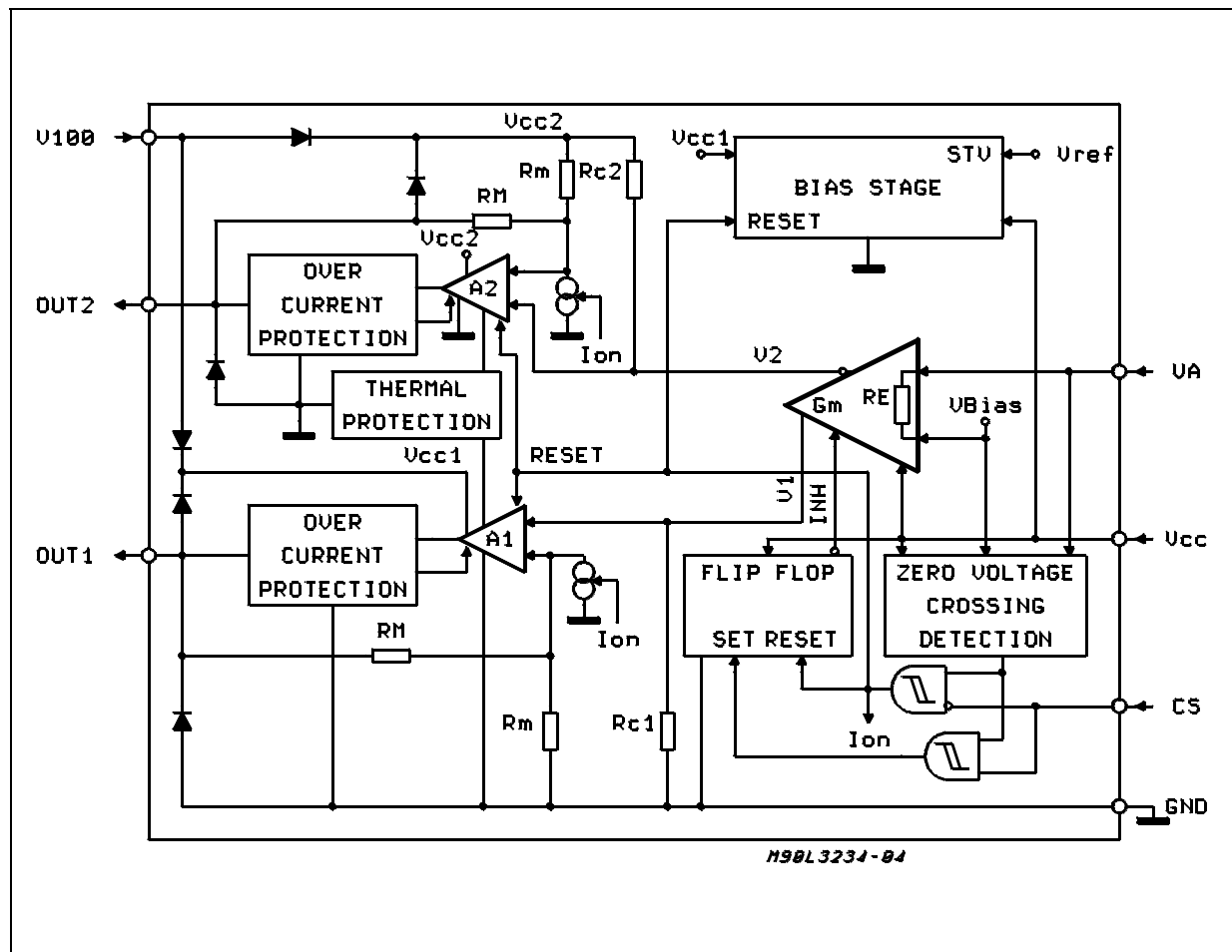
The circuit is designed with a high voltage bipolar technology ($V_{CE0} > 140V$ / $V_{CBO} > 250V$).



HEPTAWATT

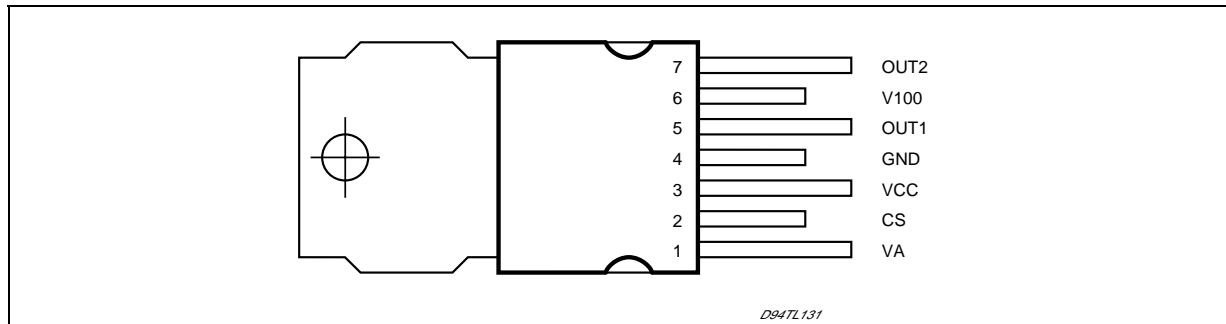
The package is a moulded plastic power package (Heptawatt) suitable also for surface mounting.

BLOCK DIAGRAM



L3234 - L3235N

PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|------------------|---|-----------------|------------------|
| V100 | Positive Power Supply Voltage | +120 | V |
| V _{CC} | 5V Power Supply Voltage | 5.5 | V |
| V _A | Low Voltage Ringing Signal (with V100 = 120Vdc) | 1.4 | V _{rms} |
| CS | Logical Ring Drive Input | V _{CC} | |
| T _j | Max. Junction Temperature | 150 | °C |
| T _{stg} | Storage Temperature | -55 to +150 | °C |

OPERATING RANGE

| Symbol | Parameter | Value | Unit |
|------------------|---|-----------------------------------|------------------|
| V100 | High Power Supply Voltage | 95 to 105 | V |
| V _{CC} | Low Power Supply Voltage | 5 ±5% | V |
| V _A | Low Voltage Ringing Signal | 600 to 950 within 10Hz - 100Hz | V _{rms} |
| T _{op} | Operating Temperature for L3234 | 0 to 70 | °C |
| T _{jop} | Max. Junction Operating Temperature (due to thermal protection) | 130 | °C |

Note: Operating ranges define those limits between which the functionality of the device is guaranteed.

THERMAL DATA

| Symbol | Description | Value | Unit |
|------------------------|-------------------------------------|---------|------|
| R _{th j-case} | Thermal Resistance Junction-case | Max. 4 | °C/W |
| R _{th j-amb} | Thermal Resistance Junction-ambient | Max. 50 | °C/W |

PIN DESCRIPTION

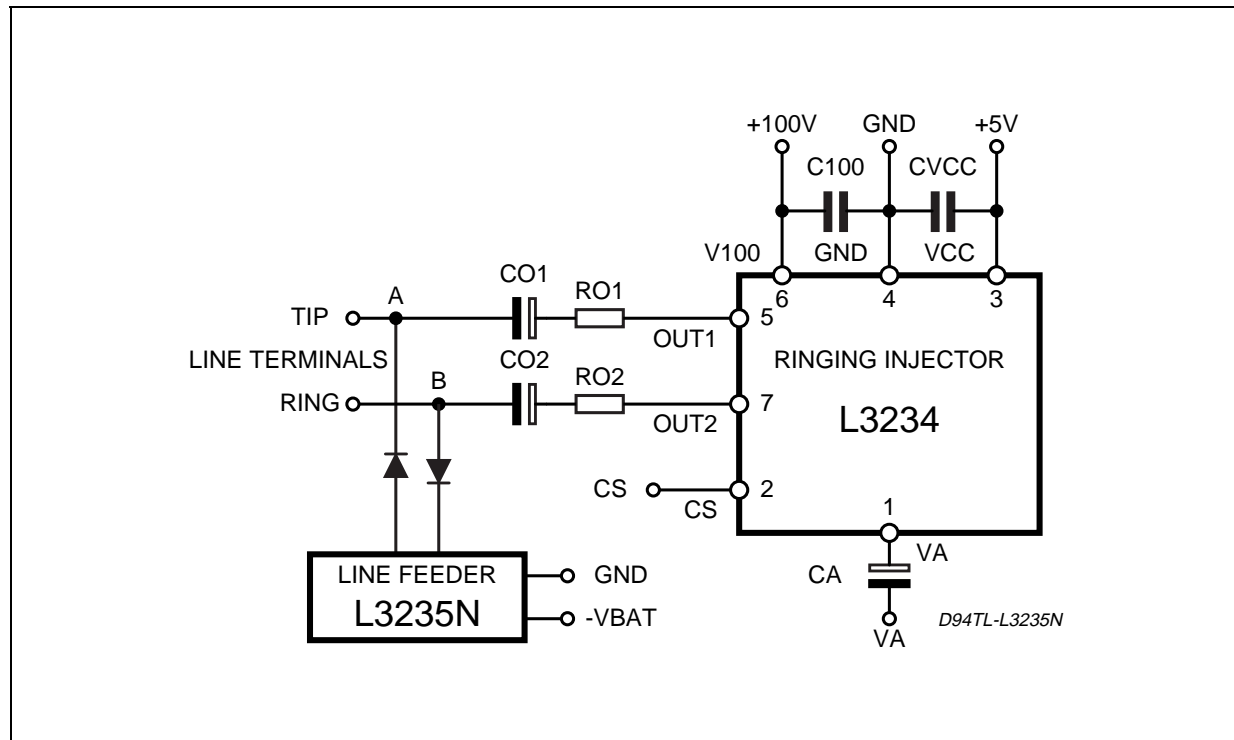
| Pin | Name | Description |
|-----|-----------------|---|
| 1 | VA | Low Voltage Ringing Signal Input |
| 2 | CS | Logical Ring Drive Input |
| 3 | V _{CC} | +5V Low Power Supply |
| 4 | GND | Common Analog-Digital Ground |
| 5 | OUT1 | Ringing Signal Output |
| 6 | V100 | +100V High Power Supply |
| 7 | OUT2 | Ringing Signal Output in Opposite Phase with Out1 |

OPERATION DESCRIPTION

The Fig. 1 show the simplified circuit configuration

of the L3234 Solid State Ringing injector when used with the L3235N Line Feeder.

Figure 1: L3234/L3235N Circuit Configuration



EXTERNAL COMPONENTS LIST

In the following table are shown the recommended external components values for L3234.

| Ref. | Value | Involved Parameter or Function |
|------------------|--------------|--|
| R01, R02 | 82Ω | Ringin ^g Feedin ^g Series Resistors |
| C01, C02 | 10μF - 160V | Ringin ^g Feedin ^g De couplin ^g Capacitors |
| CA | 4.7μF - 10V | Low Level Ringin ^g Signal De couplin ^g Capacitor |
| C100 | 100nF - 100V | Positive Battery Filter |
| CV _{CC} | 100nF | +5V Supply Filter |

When the ringing function is selected by the subscriber card, a low level signal is continuously applied to pin 1 through a de coupling capacitor. Then the logical ring drive signal CS provided by L3235N is applied to pin 2 with a cadenced mode.

The ringing cycles are synchronised by the L3234 in such a way that the ringing starts and stops always when the analog input signal crosses zero.

When the ringing injection is enabled (CS = "1"), an AC ringing signal is injected in a balanced

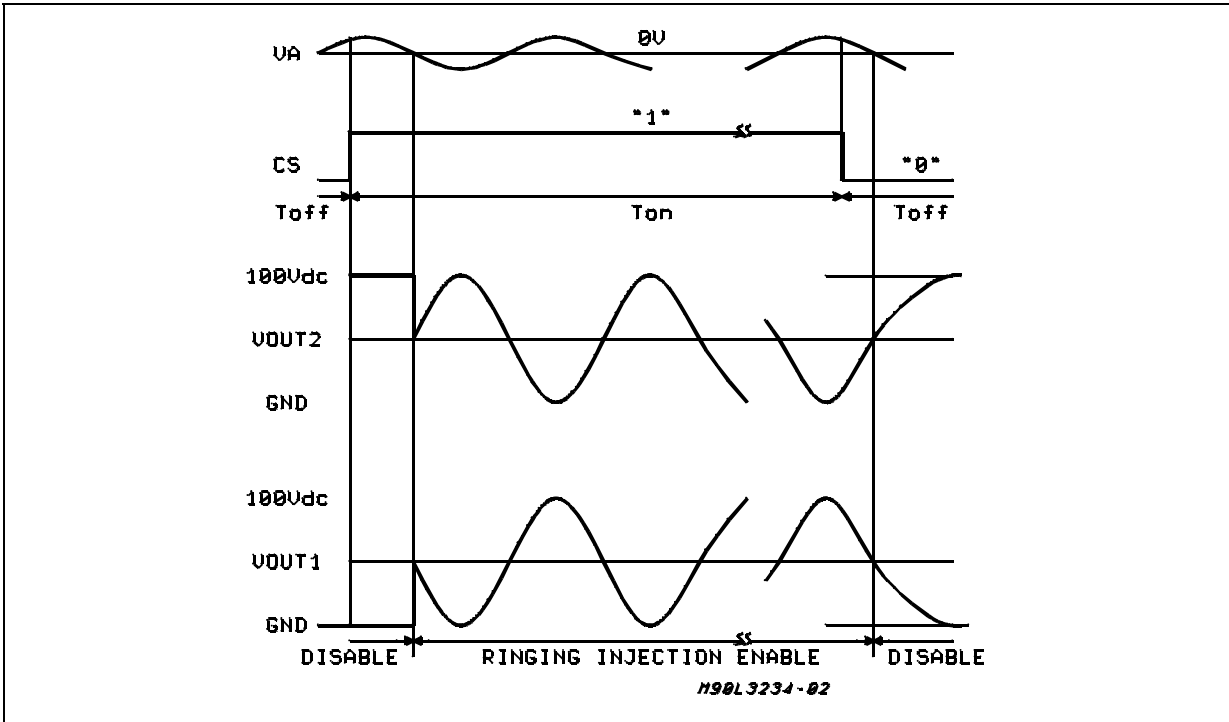
mode into the telephone line.

When the ringing injection is disabled (CS = "0"), the output voltage on OUT2 raises to the high power supply, whereas on OUT1, it falls down to ground.

The L3234 has a low output impedance when sending the signal, and high output impedance when the ringing signal is disabled

In fig. 2 the dynamic features of L3234 are shown.

Figure 2: Dynamic Features of L3234



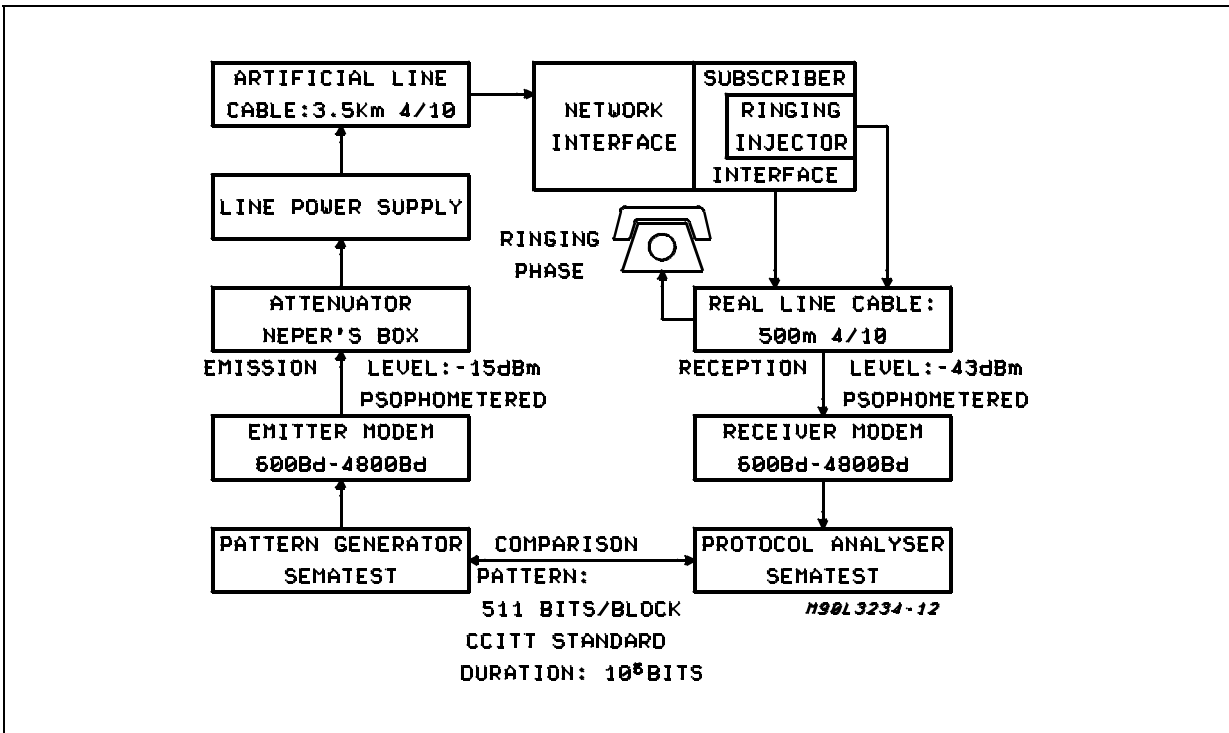
DATA TRANSMISSION INTERFERENCE TEST

The L3234 meet the requirements of the technical specification ST/PAA/TPA/STP/1063 from the CNET. The test circuit used is indicated below.

The measured error rate for data transmission is lower than 10^{-6} during the ringing phase.

This test measures if during the ringing phase the circuit induce any noise to the closer lines.

Figure 3: Test Circuit Data Transmission Interference Test



ELECTRICAL CHARACTERISTICS (Test conditions: $V_{I00} = +100V$, $V_{CC} = +5V$, $T_{amb} = 25^{\circ}C$, unless otherwise specified)

Note: Testing of all parameter is performed at $25^{\circ}C$. Characterisation, as well as the design rule used allow correlation of tested performance with actual performances at other temperatures. All parameters listed here are met in the range $0^{\circ}C$ to $+70^{\circ}C$.

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit | Fig |
|-----------------------------------|-------------------------------------|--------------------------------|----------|-----------|------------|------------------------|-----|
| STAND BY MODE: CS = "0" | | | | | | | |
| $I_S (V_{I00})$ $I_S (V_{CC})$ | Consumption | $V_A = 950mV_{rms}; 50Hz$ | | 45 560 | 100 800 | μA μA | |
| V_{SOUT1} V_{SOUT2} | DC Output Voltage | $V_A = 950mV_{rms}; 50Hz$ | 92 | | 6 | V V | |
| Z_{SOUT1} Z_{SOUT2} | Output Impedance | | 70 70 | | | $k\Omega$ $k\Omega$ | 4 |
| | Z_{OUT} Matching | | | | 15 | % | |
| THD | Harmonic Distortion During Emission | $V_{LINE} \leq 6dBm; f = 1kHz$ | | -46 | -40 | dB | 5 |

RINGING PHASE: CS = "1"

DC OPERATION

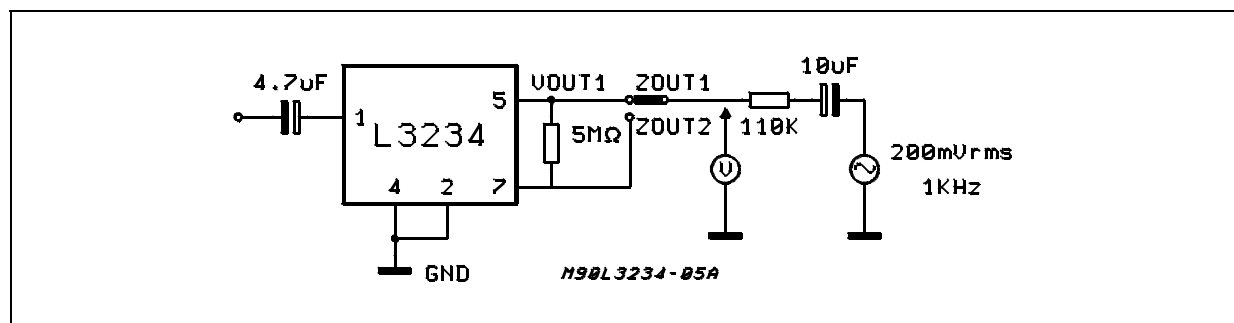
| | | | | | | | |
|-----------------------------------|---|--|----------|------------|----------|--------------|----|
| $I_R (V_{I00})$ $I_R (V_{CC})$ | Consumption | $Z_{LINE} = \infty$ $V_A = 950mV_{rms}; 50Hz$ | | 2.5 2.2 | 5 3 | mA mA | |
| V_{ROUT1} V_{ROUT2} | DC Output Voltage | $V_A = 0V$ | 44 44 | | 56 56 | V V | |
| V_{IH} $I_{IH} (CS = 0)$ | Threshold Voltage on the Logical Input CS | $V_A = 950mV_{rms}; 50Hz$ | 2.0 | | 1 | V μA | 6 |
| V_{IL} $I_{IL} (CS = 0)$ | | | | | 0.8 1 | V μA | |
| I_{lim} | DC Line Current Limitation | $V_A = 0V$ | 70 | | 150 | mA | 12 |

AC OPERATION

| | | | | | | | |
|----------------------------------|-------------------------------|---|--------------|----------|----|-----------|---|
| V_{OUT1}/V_A V_{OUT2}/V_A | Ring Gain | $Z_{LINE} = 2.2\mu F + 1k\Omega$ $V_A = 0dBm$ | 29.5 29.5 | 30 30 | | dB dB | 7 |
| $V_{OUT1} - V_{OUT1}$ | Ring Signal | $Z_{LINE} = 2.2\mu F + 1k\Omega$ $V_A = 950mV_{rms}; 50Hz$ | 57 | 60 | | Vrms | 7 |
| THD V_{LINE} | Harmonic Distortion | $V_A = 950mV_{rms}; 50Hz$ | | | 5 | % | |
| $Z_{IN} (V_A)$ | Input Impedance | $V_A = 950mV_{rms}; 50Hz$ | 40 | | | $k\Omega$ | 8 |
| Z_{OUT} | Differential Output Impedance | $I_{LINE} < 50mA_{rms}$ | | | 20 | Ω | 9 |

TEST CIRCUITS

Figure 4.



TEST CIRCUITS (continued)
Figure 5.

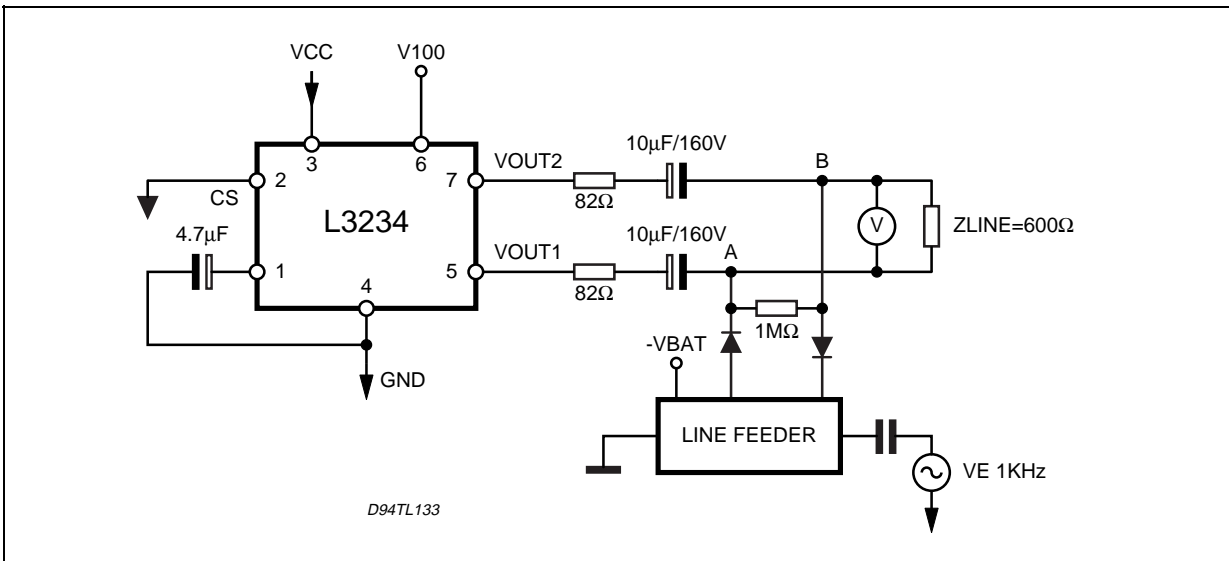


Figure 6.

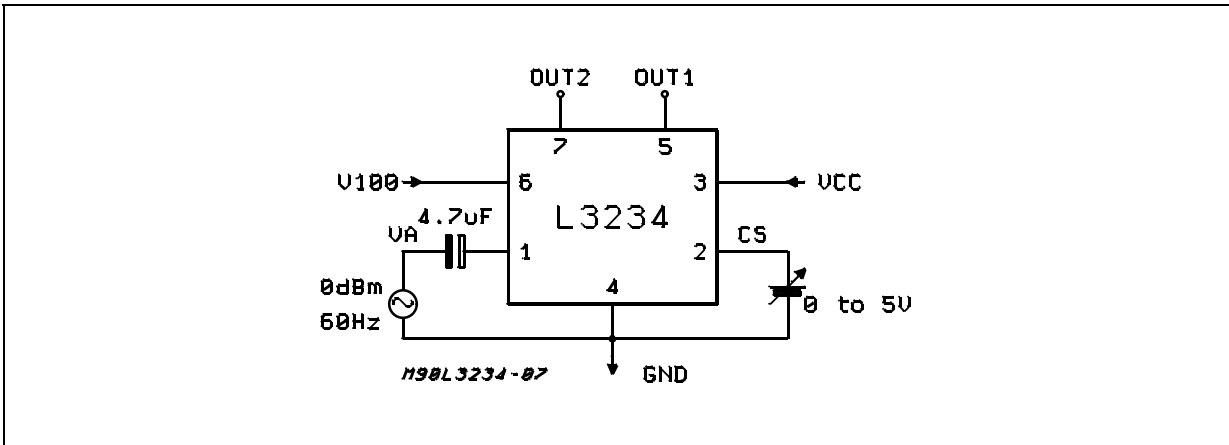
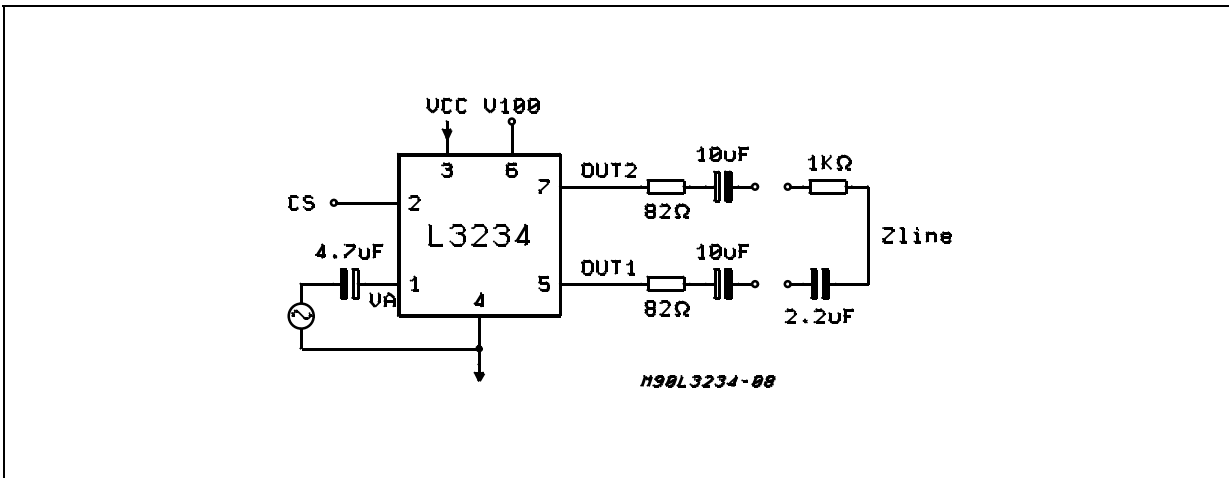


Figure 7.



TEST CIRCUITS (continued)
Figure 8.

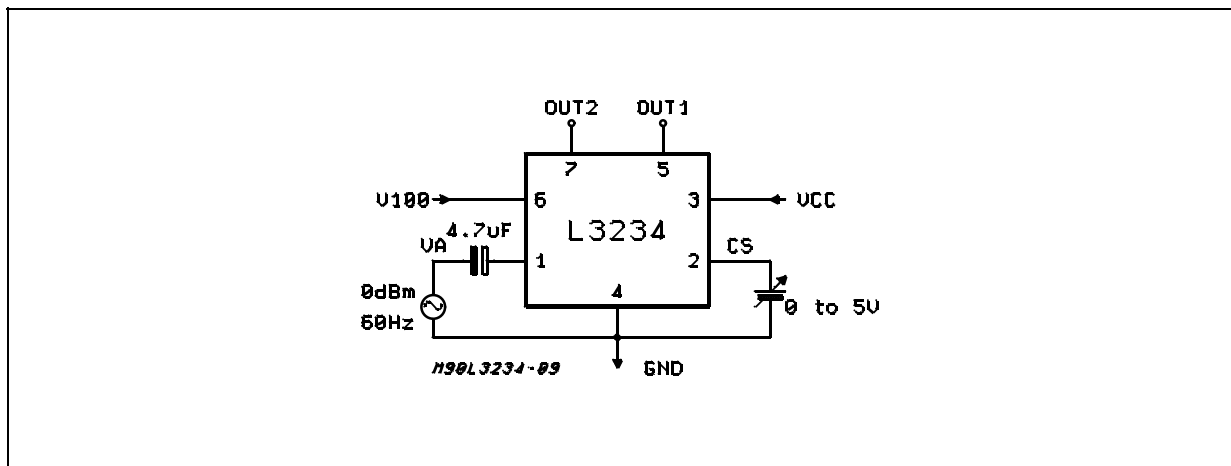


Figure 9.

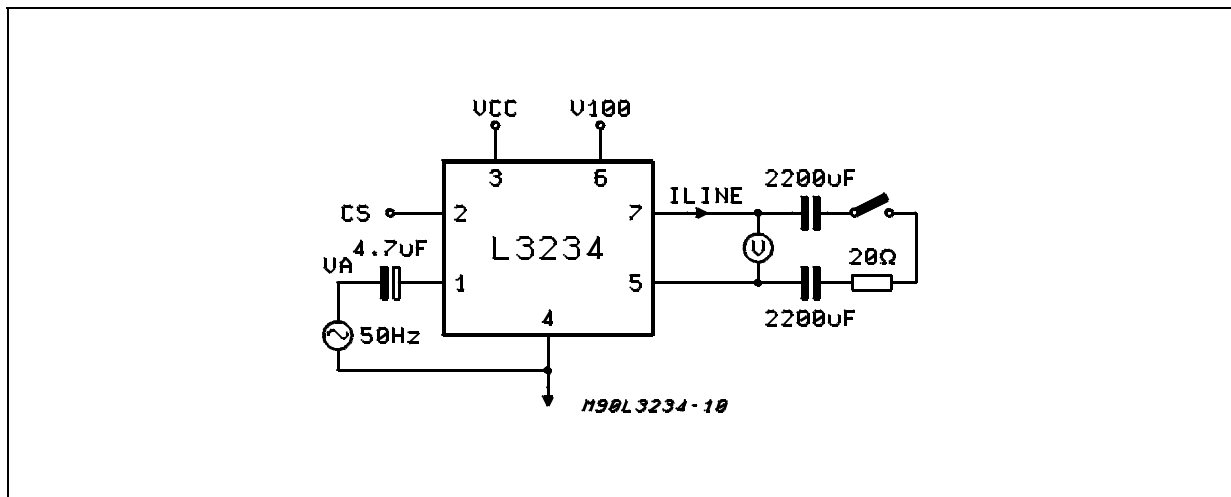
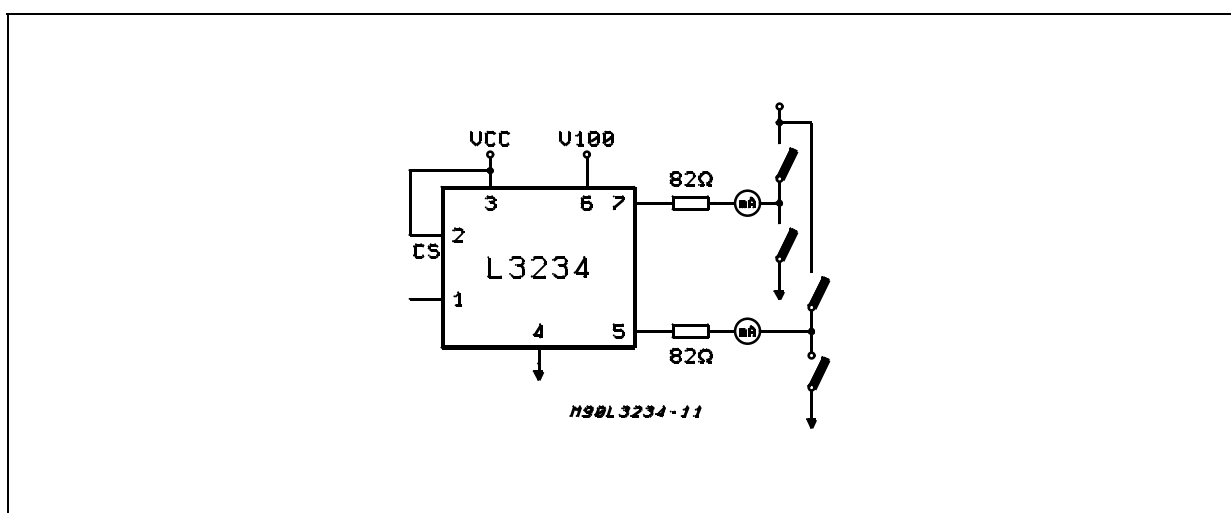


Figure 10.



L3235N

Subscriber Line Interface Circuit

DESCRIPTION

Circuit description

The L3235N Subscriber Line Interface Circuit (SLIC) is a bipolar integrated circuit in 60V technology optimized for PABX application.

The L3235N supplies a line feed voltage with a current limitation which can be modified by an external resistor (RLIM).

The SLIC incorporates loop currents, ground key detection functions with an externally programmable constant time.

The two to four wires and four to two wires voice frequency signal conversion is performed by the L3235N and the line terminating and the balancing impedances are externally programmable.

The device integrates an automatic power limitation circuit. In short loop condition the extra power is dissipated on one external transistor (Text).

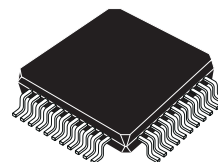
This approach allows to assembly the L3235N in a low cost standard plastic TQFP44 package.

The chip is protected by thermal protection at $T_j = 150^{\circ}\text{C}$.

The SLIC is able to give a power up command for Combo in off hook condition and an enable logic for solid state ringing injector L3234.

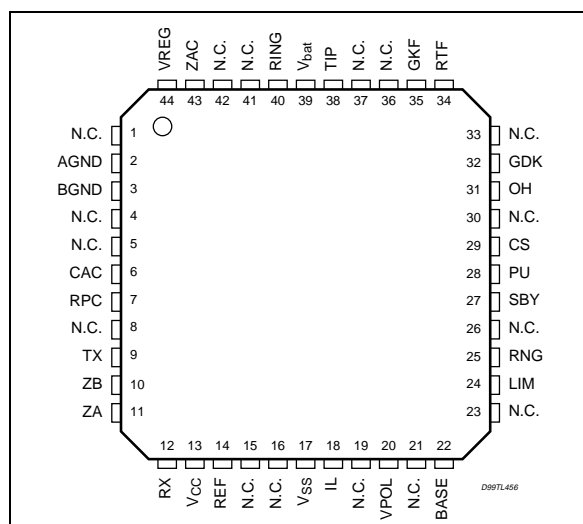
The L3235N package is 44 pin plastic TQFP.

The L3235N has been designed to operate together with L3234 performing complete BORSHT function without any electromechanical ringing relay (see the application circuit fig. 16).



TQFP44

PIN CONNECTION



ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|-----------|---------------------------|-------------|--------------------|
| V_{BAT} | Battery Voltage | -54 | V |
| V_{CC} | Positive Supply Voltage | 5.5 | V |
| V_{SS} | Negative Supply Voltage | -5.5 | V |
| T_j | Max. Junction Temperature | 150 | $^{\circ}\text{C}$ |
| T_{stg} | Storage Temperature | -55 to +150 | $^{\circ}\text{C}$ |

OPERATING RANGE

| Symbol | Parameter | Min. | Max. | Unit |
|-----------|------------------------------------|-------|-------|--------------------|
| V_{BAT} | Battery Voltage | -52 | -24 | V |
| V_{CC} | Positive Supply Voltage | 4.75 | 5.25 | V |
| V_{SS} | Negative Supply Voltage | -5.25 | -4.75 | V |
| T_{op} | Operating Temperature for L3235N | 0 | 70 | $^{\circ}\text{C}$ |
| T_j | Max Junction Operating Temperature | | 130 | $^{\circ}\text{C}$ |

Note: Operating ranges define those limits between which the functionality of the device is guaranteed.

THERMAL DATA

| Symbol | Description | Value | Unit |
|-----------------|-------------------------------------|-------|---------|
| $R_{th\ j-amb}$ | Thermal Resistance Junction-ambient | Max | 60 °C/W |

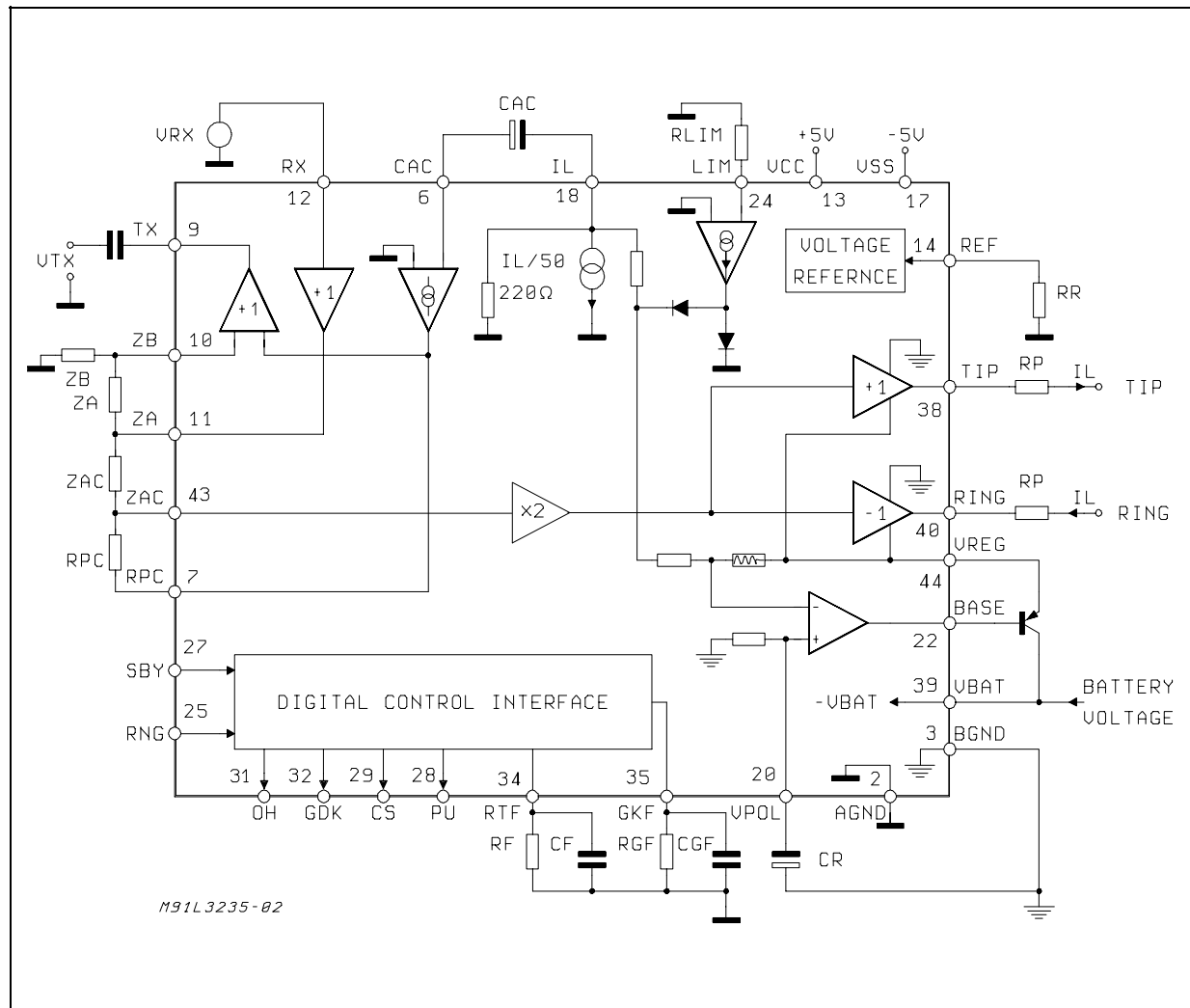
PIN DESCRIPTION

| N° | Name | Description |
|---|------------------|--|
| 1,4,5,8, 15,16,19 ,21,23, 26,30,33 ,36,37, 41,42 | NC | Not Connected |
| 2 | AGND | Analog/Digital Ground. |
| 3 | BGND | Battery Ground. This is the Reference for the Battery Voltage (note 1). |
| 6 | CAC | AC Current Feedback Input. |
| 7 | RPC | External Protection Resistors AC Transmission Compensation. |
| 9 | TX | Four Wire Transmitting Amplifier Output. |
| 10 | ZB | Non Inverting Operational Input Inserted in the Hybrid Circuit for 2W to 4W Conversion. The Network Connected from this Pin to Ground shall be a copy of the Line Impedance. |
| 11 | ZA | VRX Output Buffer 2W to 4W Conversion. |
| 12 | RX | High Impedance Four Wire Receiving Input. |
| 13 | V _{CC} | Positive 5V Supply Voltage. |
| 14 | REF | Voltage Reference Output; a Resistor Connected to this pin sets the Internal Bias Current. |
| 17 | V _{SS} | Negative 5V Supply Voltage. |
| 18 | IL | Transversal Line Current Feedback Divided by 50. |
| 20 | VPOL | Non Inverting Operational Input to Implement DC Character. |
| 22 | BASE | Driver for External Transistor Base. |
| 24 | LIM | Voltage Reference Output; a Resistor Connected to this Pin Sets the Value of Line Current Limitation. |
| 25 | RNG | Ringing Logic Input from Line Card Controller. |
| 27 | SBY | Stand by Logic Input (SBY = 1 Set Line Current Limitation at 3mA). |
| 28 | PU | Power u.p Logic Output for the Codec Filter. (PU = 0 means Codec Filter Activated) |
| 29 | CS | Ring Injector Enable for L3234 Output. (CS = 1 means L3234 Ringing Injection Enable). |
| 31 | OH | Hook Status Logic Output (OH = 0 means off hook). |
| 32 | GDK | Ground Key Status Logic Output (GDK = 0 means Ground Key on). |
| 34 | RTF | Time Constant Hook Detector Filter Input. |
| 35 | GKF | Time Constant GK Detector Filter Input. |
| 38 | TIP | Tip Wire of 2 Wire Line Interface. |
| 39 | V _{bat} | Negative Battery Supply Input. |
| 40 | RING | RING wire of 2 Wire Line Interface. |
| 43 | ZAC | Non Inverting Input of the AC Impedance Synthesis Circuit. |
| 44 | VREG | Emitter Connection for the External Transistor. |

Note 1:

AGND and BGND pins must be tied together at a low impedance point (e.g. at card connector level).

L3235N FUNCTIONAL DIAGRAM



FUNCTIONAL DESCRIPTION

DIGITAL INTERFACE

The different operating modes of the L3235N are programmed through a digital interface based on two input pins:

- 1) SBY input programs the stand-by or Active/Ringing modes.
- 2) RNG input programs the ringing ON/OFF activation condition for the L3234.

The L3235N digital interface has four output pins :

- 1) OH provides the on hook/off hook or ring trip informations (active low).
- 2) GDK provides the ground key on/off information (active low).
- 3) PU must be connected to the enable input pin of CODEC/FILTER devices like ETC 5054/57

and automatically activates this device when in active mode off-hook is detected or when ringing mode is selected.

- 4) CS output must be connected to the CS enable input of the solid state ringing injector L3234.

In this way the L3234 will be enabled when ringing mode is programmed and will be automatically disabled when the ring trip condition will be detected reducing the ringing signal disconnection time after ring trip.

The table 1 here below resumes the different operation modes and the relative logic output signals.

The two current detection (hook and GND key) have internal fixed threshold. Externally it is possible to program their time constant through two R-C components connected respectively to pin 26 (RTF) and pin 27 (GKF).

Table 1.

| OPERATING MODE | INPUT PIN | | LINE STATUS | | OUTPUT PIN | | | |
|----------------|-----------|-----|---------------------------|--------------------------------|------------|-----|----|------|
| | SBY | RNG | 0: ON HOOK 1: OFF HOOK | 0: NO GND KEY 1: GND KEY ON | OH | GDK | PU | CS |
| ACTIVE | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| RINGING | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0(*) |
| | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0(*) |
| | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0(*) |
| STAND-BY | 1 | 0 | X | X | 1 | 1 | 1 | 0 |
| | 1 | 1 | X | X | 1 | 1 | 0 | 1 |

(*)This status is latched and doesn't change until RNG turn to 0

OPERATING MODES

Stand-By (SBY = 1 and RNG = 0)

In Stand-By mode the L3235N limits the DC Loop current to 3 mA.

In this mode all the AC circuits are active and all the AC characteristics are the same as in Active Mode.

Also the two Line Current detectors (hook and GND key) are active but due to the loop current limited to 3 mA they will not be activated.

This mode is useful in emergency condition when it is very important to limits the system power dissipation.

Ring Mode (SBY = 0 and RNG = 1)

When ringing mode is selected "CS" pin is set to 1 in order to activate the L3234 ringing injector.

See L3234 for detailed description.

Ring trip is detected by means of the same internal circuitry used for off-hook detection.

An off-hook delay time lower than $\frac{1}{2} F_{RING}$ should be selected. (see ext. components list).

When ring trip is detected "CS" is automatically set to "0" allowing in this way a quick ringing disconnection.

After Ring trip detection the Card Controller must set the L3235N in active mode to remove the internal latching of the "CS" information.

Active mode (SBY = 0 and CS1 = 0)

In Active mode the L3235N has the DC characteristic show in Fig.13

The DC characteristics of L3235N has two different feeding conditions:

1)Current Limiting Region : (short loop) the DC impedance of the SLIC is very high (>20 Kohm) therefore the system works as a current generator. By the ext. resistor RLIM connected at pin 19 it is possible to program limiting current values from 20 mA to 70 mA.

2) Voltage source region (long loop).

The DC impedance of the L3235N is almost equal to zero therefore the system works like a voltage generator with in series the two external protection resistors Rp.

When a limiting current value higher than 40 mA is programmed the device will automatically reduce to 40 mA the loop current for very short loop.

This is done in order to limit the maximum power dissipation in very short loop to values lower than 2W for the external transistor and lower than 0.5W for the L3235N itself.

This improve the system reliability reducing the L3235N power dissipation and therefore the internal junction temperature.

Figure 11: DC characteristic in Active Mode with two different values of limiting current (30mA and 70 mA).

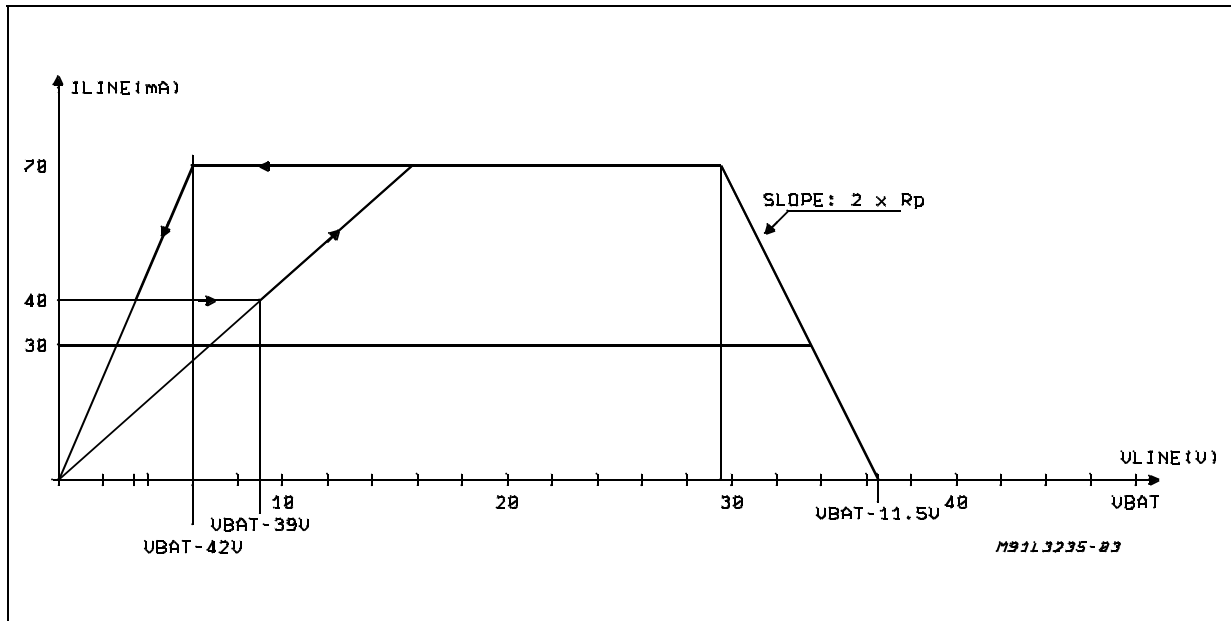
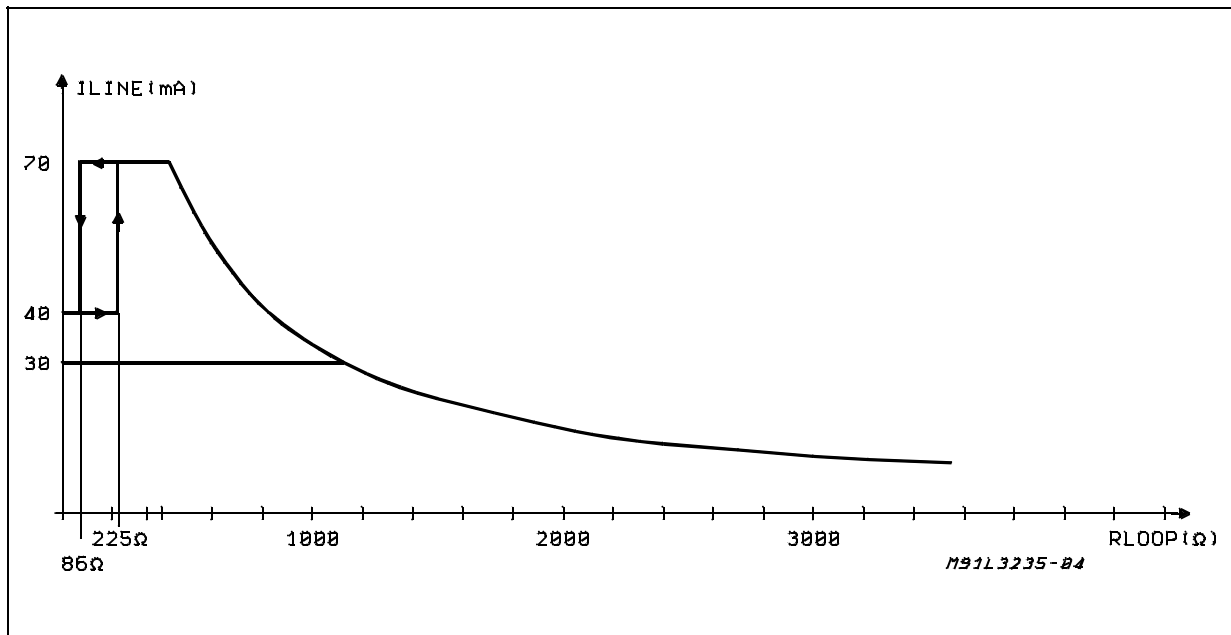


Figure 12: Line current versus loop resistance with two different values of limiting current (30mA and 70mA)



AC transmission circuit stability

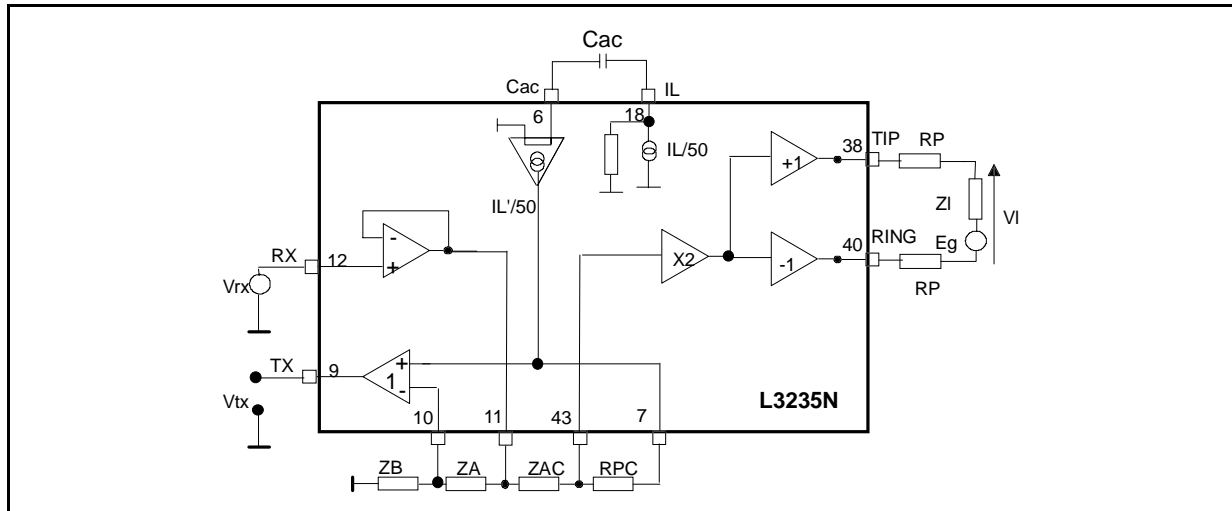
To ensure stability of the feedback loop shown in block diagram form in figure 13 two capacitors are required. Figure 14 includes these capacitors Cc and Ch.

AC - DC separation

The high pass filter capacitor C_{AC} provides the separation between DC circuits and AC circuits. A C_{AC} value of 100mF will position the low end frequency response 3dB break point at 7Hz,

$$f_{sp} = \frac{1}{2\pi \cdot 220\Omega \cdot C_{AC}}$$

Figure 13.



AC Characteristic

A simplified AC model of the transmission circuits is shown in figure 13

Where:

- V_{rx} is the received signal
- V_{tx} is the transmitted signal
- V_l is the AC transversal voltage in line
- E_g is the line open circuit AC voltage
- Z_l is the line impedance
- R_P are the protection resistors
- Z_B is the line impedance balancing network
- Z_A is the SLIC impedance balancing network
- Z_{AC} programmable AC line termination impedance
- R_{PC} used for external protection resistors insertion loss compensation
- $I/50$ is the AC transversal current divided by 50
- CAC AC feedback current decoupling

AC behavior

The AC path simplified formulas, that are valid when $I/50'$ is equal to $I/50$, are the following :

- Two wire impedance
The impedance presented to the two wire by the SLIC including the protection resistors R_P and defined as Z_s is equal to :
$$Z_s = Z_{AC}/12.5 + 2R_P$$

i.e. with $Z_{AC} = 6250 \text{ W}$ and $R_P = 50 \text{ W}$
 $Z_s = 600 \text{ W}$
- Two wire to four wire gain
The transmission gain , G_{tx} , of the SLIC is

equal to :

$$G_{TX} = V_{tx} / V_l$$

$$G_{TX} = 0.25 * (R_{PC} + Z_{AC}) / (25R_P + Z_{AC})$$

using $R_{PC} = 25R_P$, as recommended to compensate the protection resistor R_P ,
 $G_{TX} = 0.25$ (-12 dB)

- Four wire to two wire gain
The receiver gain , G_{rx} , of the SLIC is equal to:

$$G_{RX} = V_l / V_{rx}$$

$$G_{RX} = 50Z_l / (Z_{AC} + 12.5(Z_l + 2R_P))$$

using $Z_{AC} = 12.5(Z_s - 2R_P)$ and assuming
 $Z_l = Z_s$ we have the following gain:

$$G_{RX} = 2 \quad (+6 \text{ dB})$$

- Hybrid function
The transybrid loss, Th_l , is equal to:

$$Th_l = V_{tx} / V_{rx}$$

$$Th_l = Z_B / (Z_A + Z_B) - (Z_{AC} + R_{PC}) / (Z_{AC} + 12.5(2R_P + Z_l))$$

using $Z_{AC} = 12.5(Z_s - 2R_P)$ and $R_{PC} = 25R_P$
we have the following relation:

$$Th_l = Z_B / (Z_A + Z_B) - Z_l / (Z_l + Z_s)$$

To maximize the hybrid attenuation the impedance must be matched, $Z_A / Z_B = Z_s / Z_l$, to guarantee $Th_l = 0$.

From the above relation it is evident that if Z_s is equal to the Z_l in Th_l test the impedance Z_A and Z_B can be substituted by two equal resistors.

External components list for L3235N

To set the SLIC into operation the following parameters have to be defined:

- The AC SLIC impedance at line terminals "Zs" to which the return loss measurements is referred. It can be real (typ. 600Ω) or complex.
- The equivalent AC impedance of the line "Zl" used for evaluation of the trans-hybrid loss performance (2/4 wire conversion). It is usually a complex impedance.
- The value of the two protection resistors Rp in series with the line termination.

Once, the above parameters are defined, it is possible to calculate all the external components using the following table. The typical values has been obtained supposing: Zs = 600Ω; Zl = 600Ω; Rp = 50Ω

| Name | Suggested Value | Function | Formula |
|-------------------------------------|--------------------|---|---|
| R _F C _F | 39KΩ 390nF | Delay Time On-hook Off-hook | $\tau = 0.69 \cdot C_F \cdot 39K\Omega$ (1) |
| R _{GF} C _{GF} | 39KΩ 390nF | Delay Time GK Detector | $\tau = 0.69 \cdot C_{GF} \cdot 39K\Omega$ |
| R _R | 51KΩ | Bias Set | |
| R _{LIM} | 8.4KΩ to 33KΩ | Ext. Current Limit. Progr. | $R_{LIM} = \frac{564}{I_{LIM} - 3mA}$ |
| CR | 4.7μF 6.3 V 30% | Negative Battery Filter | $C_{AC} = \frac{1}{2\pi \cdot 16K\Omega \cdot f_p}$ |
| R _P | 50 | Protection Resistors | $47 \leq R_P \leq 100\Omega$ (2) |
| R _T | 1MΩ 20% | Termination Resistor | |
| C _{AC} | 100μF 6.3V 20% | DC/AC current feedback splitting | $C_{AC} = \frac{1}{2\pi \cdot 220\Omega \cdot f_{sp}}$ |
| R _{PC} | 1250Ω 1% | R _P insertion loss compensation | $R_{PC} = 12.5 \cdot (2R_P)$ |
| Z _{AC} | 6250Ω 1% | 2W AC Impedance programming | $Z_{AC} = 12.5 \cdot (Z_S - 2R_P)$ |
| C _C | 470pF 20% | AC Feedback compensation | $f_1 = 300KHz \quad C_C = \frac{1}{2\pi f_1 \cdot 25R_P}$ |
| Z _{AS} | 12500Ω 1% | Slic Impedance Balancing Net. | $Z_{AS} = 25 \cdot (Z_S - 2R_P)$ |
| R _{AS} | 2500Ω 1% | | $R_{AS} = 25 \cdot (2R_P)$ |
| Z _B | 15KΩ 1% | Line impedance Balancing Net. | $Z_B = 25 \cdot Z_l$ |
| C _H | 220pF 20% | C _C Transybrid loss Compensation | $C_H = C_C \cdot \frac{Z_{AC}}{Z_{AS}}$ |
| C _{TX} | 4.7μF 30% | DC Decoupling Tx Output | $C_{TX} = \frac{1}{6.28 \cdot f_p \cdot Z_{load}}$ |
| D1, D2 | 1N4007 | Line Rectifier | |
| Text | (3) | External Transistor | $P_{Diss} \geq 2W, V_{CEO} \geq 60V$ $H_{FE} \geq 40, I_C \geq 100mA$ $V_{BE} < 0.8V @ 100mA$ |
| CV _{SS} ; CV _{DD} | 100nF | ±5V supply filter | |
| C _{VB} | 100nF/100V | V _{BAT} supply filter | |

Notes:

1) For proper operation Cf should be selected in order to verify the following conditions:

A) $cf > 150nF$

B) $\tau < 1/2 \cdot f_{RING}$

f_{RING} : Ringing signal frequency

2) For protection purposes the RP resistor is usually splitted in two part R_{P1} and R_{P2}, with R_{P1} ≥ 30Ω.

3) ex: BD140; MJE172; MJE350.... (SOT32 or SOT82 package available also for surface mount). For low power application (reduced battery voltage) BCP53 (SOT223 surface mount package) can be used. Depending on application enviroment an heatsink could be necessary.

L3234 - L3235N

ELECTRICAL CHARACTERISTICS (Test condition: refer to the test circuit of the fig. 16; $V_{CC} = 5V$, $V_{SS} = -5V$, $V_{bat} = -48V$, $T_{amb} = 25^{\circ}C$, unless otherwise specified)

Note: Testing of all parameters is performed at $25^{\circ}C$. Characterization, as well as the design rules used allow correlation of tested performance with actual performance at other temperatures. All parameters listed here are met in the range $0^{\circ}C$ to $+70^{\circ}C$.

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit | Fig. |
|--------|-----------|----------------|------|------|------|------|------|
|--------|-----------|----------------|------|------|------|------|------|

STAND-BY

| | | | | | | | |
|-----------|---------------------------------|-------------------|------|---|----|----|--|
| V_{IS} | Output Voltage at TIP/RING pins | $I_{LINE} = 0$ | 35.7 | | 39 | V | |
| I_{LCC} | Short Circuit Current | Stand-by, SBY = 1 | 2 | 3 | 4 | mA | |

DC OPERATION

| | | | | | | | |
|------------|---------------------------------|-------------------------------------|--------------|-----|----------|--------|--|
| V_{IP} | Output Voltage at TIP/RING pins | $I_{LINE} = 0$ $I_{LINE} = 50mA$ | 35.7 35.2 | | 39 39 | V V | |
| I_{lim} | Current Progr. | $I_{lim} \text{ Prog.} = 70mA$ | 63 | 70 | 77 | mA | |
| I_{lim} | Current Progr. | $8.4K\Omega < R_{LIM} < 33K\Omega$ | 20 | | 70 | mA | |
| I_O | On-hook Threshold | | | | 5 | mA | |
| I_f | Off-hook Threshold | | 10 | | | mA | |
| I_{gk} | GK Detector Threshold | | 10 | | 17 | mA | |
| Gklim | Ground Key Current Limitation | RING to BGND | 13 | | 22 | mA | |
| Gkov | Ground Key Threshold Overlap | Gklim-Ilgk | 1 | | | mA | |
| I_{max} | Max. Output Current at TIP/RING | $I_{lim} = 70mA$ | 90 | | 140 | mA | |
| I_{VCC} | Supply Current from V_{CC} | $I_{line} = 0$ | | 6.2 | 8 | mA | |
| I_{VSS} | Supply Current from V_{SS} | $I_{line} = 0$ | | 1.6 | 2.1 | mA | |
| I_{Vbat} | Supply Current from V_{bat} | $I_{line} = 0$ | | 2.8 | 3.6 | mA | |

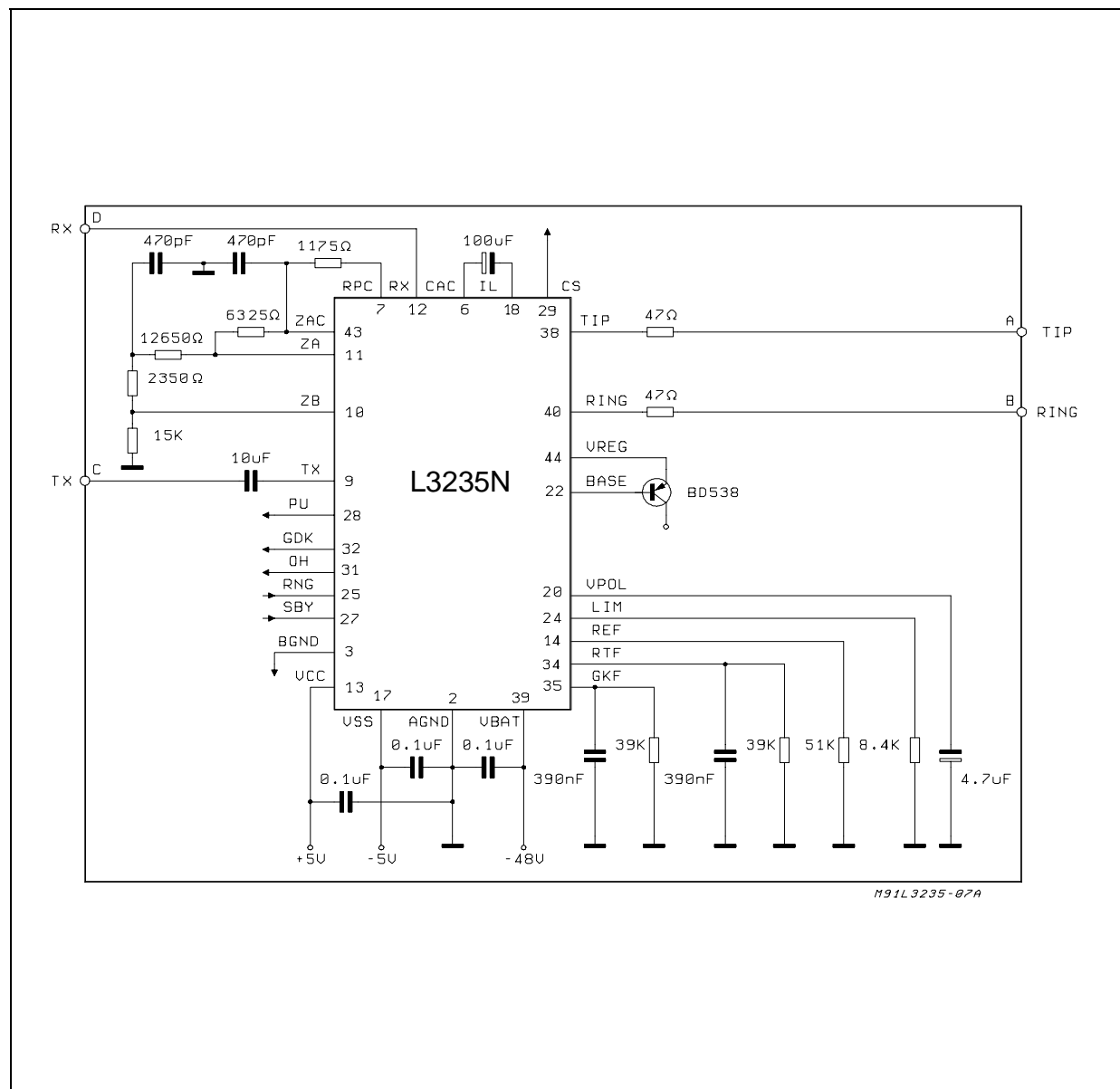
AC OPERATION

| | | | | | | | |
|-----------|---|--|-------------|------------|-------|------------|----|
| Z_{Tx} | Sending Output Impedance | pin 9 (Tx) | | | 10 | Ω | |
| Z_{Rx} | Receiving Input Impedance | pin 12 (Rx) | 1 | | | M Ω | |
| R_l | 2W Return Loss | $f = 300$ to $3400Hz$ | 22 | 36 | | dB | A1 |
| Thl | Trans Hybrid Loos | $f = 300$ to $3400Hz$ | 22 | 36 | | dB | A2 |
| G_s | Sending Gain | $f = 1020Hz$ $I_l = 20mA$ | -11.9 | -12.1 | -12.3 | dB | A3 |
| G_{sf} | Flatness | $f = 300$ to $3400Hz$ | -0.2 | | 0.2 | dB | |
| G_{sl} | Linearity | -20dB to 10dBm | -0.2 | | 0.2 | dB | |
| G_r | Receiving Gain | $f = 1020Hz$ $I_l = 20mA$ | 5.8 | 6 | 6.2 | dB | A4 |
| G_{rf} | Flatness | $f = 300$ to $3400Hz$ | -0.2 | | 0.2 | dB | |
| G_{rl} | Linearity | -20dBm to +4dBm | -0.2 | | 0.2 | dB | |
| Np4W | Psoph. Noise at Tx | | | -90 | -78 | dBmp | |
| Np2W | Psoph. Noise at Line | | | -82 | -70 | dBmp | |
| S_{vrr} | Relative to V_{bat} versus Line Terminal versus Tx Terminal | $f = 1020Hz$ $V_S = 100mV_{pp}$ | | -30 -24 | | dB dB | A5 |
| S_{vrr} | Relative to V_{CC} and V_{SS} versus Line Terminal versus Tx Terminal | $f = 1020Hz$ $V_S = 100mV_{pp}$ | | -20 -14 | | dB dB | |
| L_{tc} | L/T Conversion measured at line Terminals | $f = 300$ to 3400 $I_{line} = 20mA$ | 49 53(*) | | | dB dB | A6 |
| T_{lc} | T/L Conversion Measured at Line Terminals | $f = 300$ to 3400 $I_{line} = 20mA$ | 46(*) | | | dB | A7 |

(*) Selected parts L3235NC

ELECTRICAL CHARACTERISTICS (continued)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit | Fig. |
|----------|-------------------------------|---|----------|------|------------|---------------|------|
| V_{il} | Input Voltage at Logical "0" | Input SBY, CS1 | 0 | | 0.8 | V | |
| V_{ih} | Input Voltage at Logical "1" | Input SBY, CS1 | 2 | | 5 | V | |
| I_{il} | Input Current at Logical "0" | Input SBY, CS1 | | | 10 | μA | |
| I_{ih} | Input Current at Logical "1" | Input SBY, CS1 | | | 10 | μA | |
| V_{ol} | Output Voltage at Logical "0" | $I_{out} = 1\text{mA}$ $I_{out} = 10\mu\text{A}$ | | | 0.5 0.4 | V | |
| V_{oh} | Output Voltage at Logical "1" | $I_{out} = 10\mu\text{A}$ $I_{out} = 1\text{mA}$ | 4 2.7 | | | V | |

Figure 14: Test Circuit

APPENDIX A

L3235N TEST CIRCUITS

Referring to the test circuit reported in fig 16 you can find the proper configuration for the main measurements.

In particular:

A-B: Line terminals

C: Tx sending output on 4W side

D: Rx receiving input on 4W Side

Figure A1: 2W Return Loss

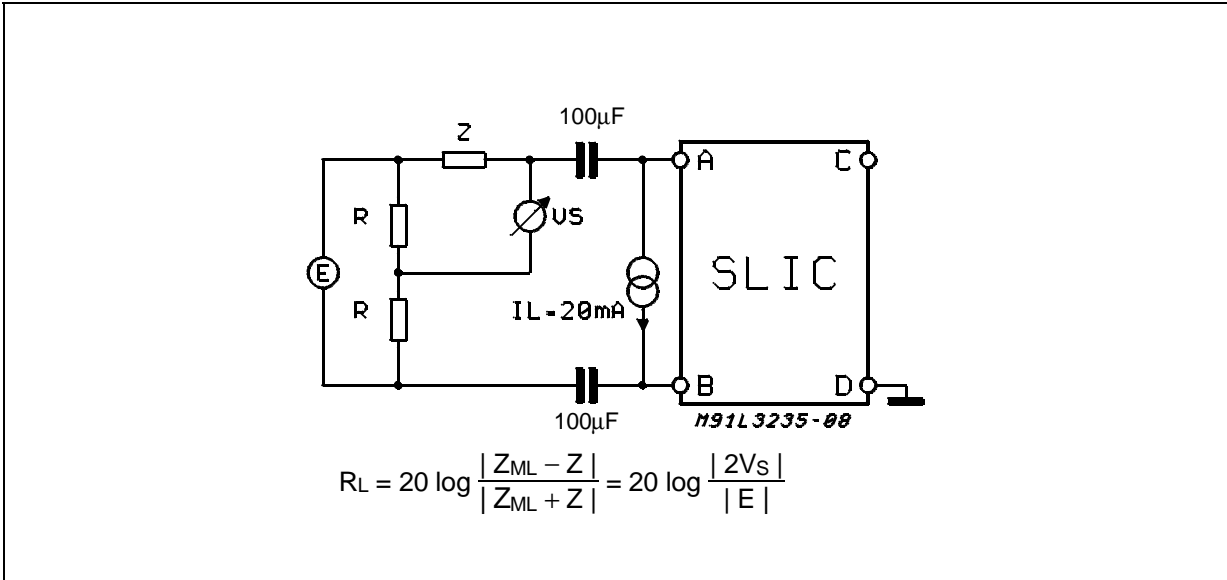


Figure A2: Trans-hybrid Loss

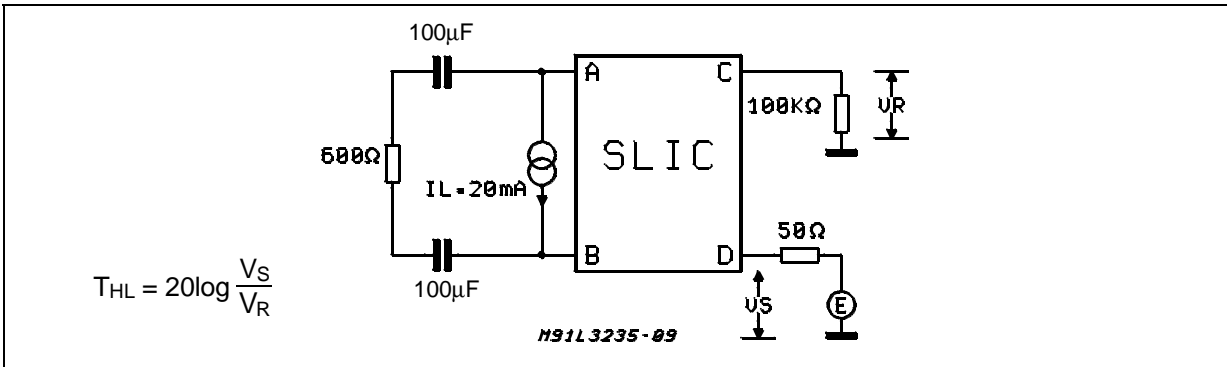
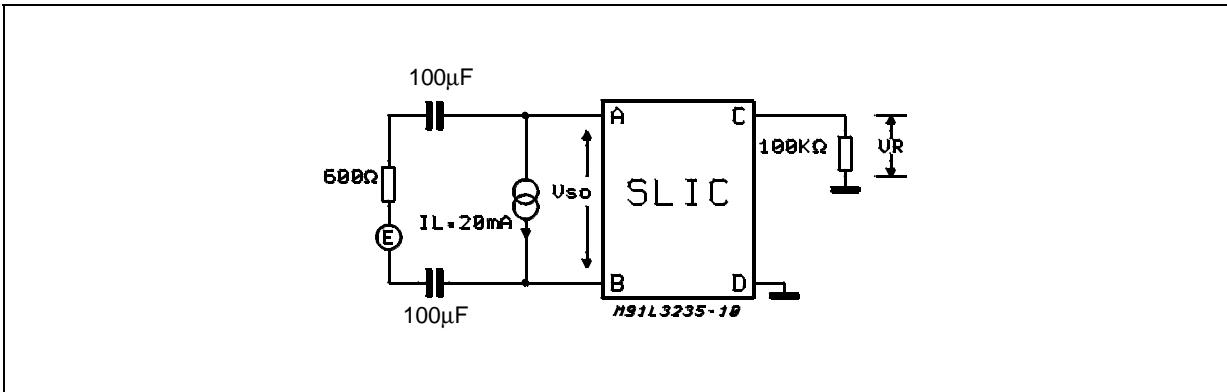


Figure A3: Sending Gain



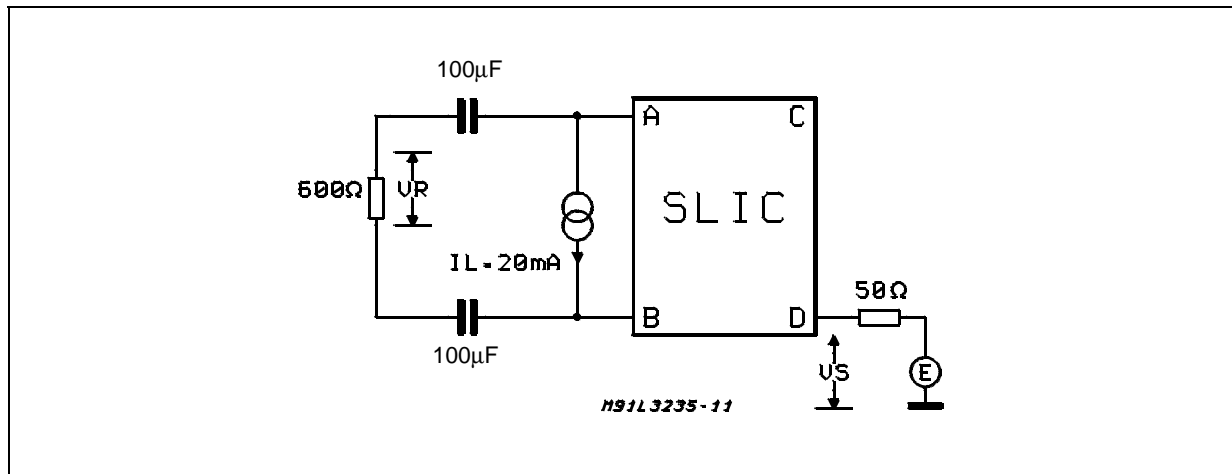
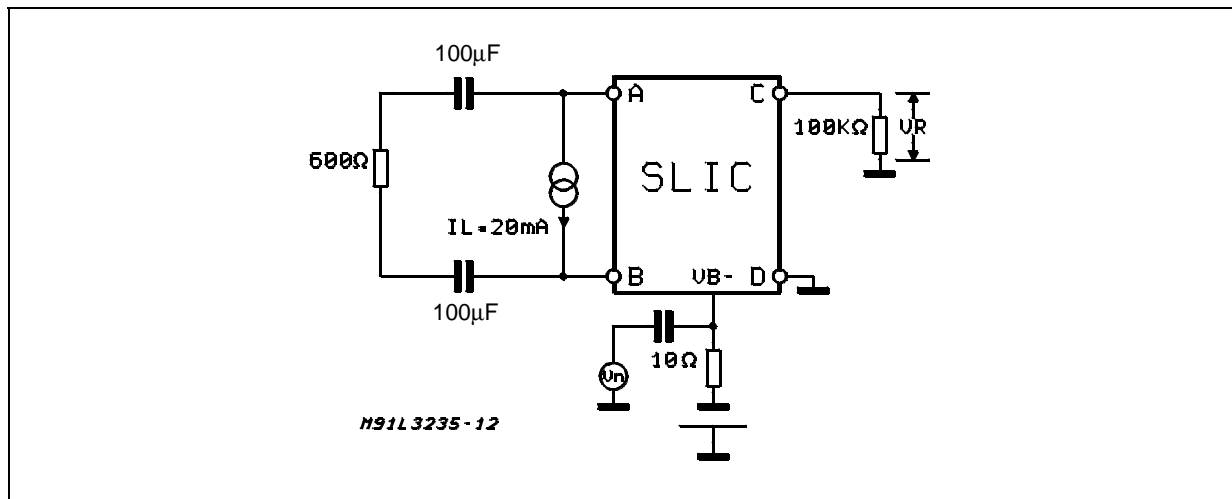
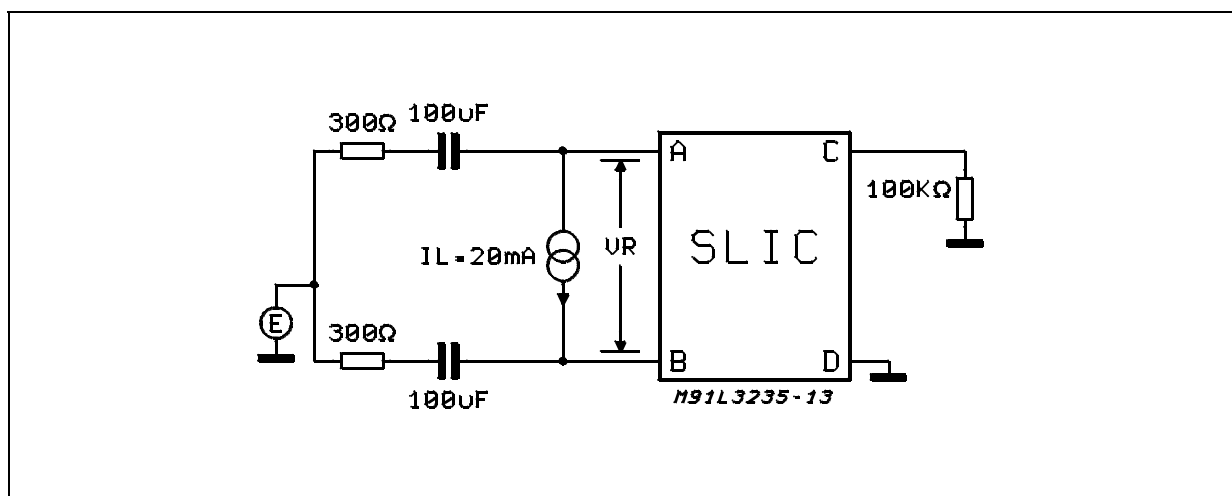
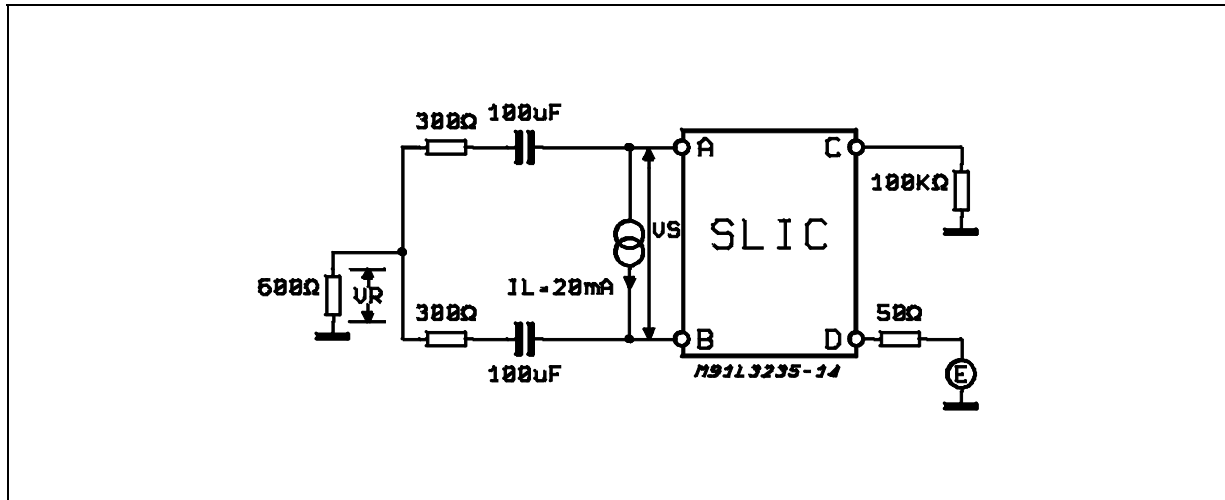
TEST CIRCUITS (continued)**Figure A4:** Receiving Gain**Figure A5:** SVRR Relative to Battery Voltage V_B **Figure A6:** Longitudinal to Transversal Conversion

Figure A7: Transversal to Longitudinal Conversion



APPENDIX B

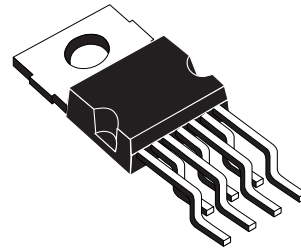
LAYOUT SUGGESTIONS

Standard layout rules should be followed in order to get the best system performances:

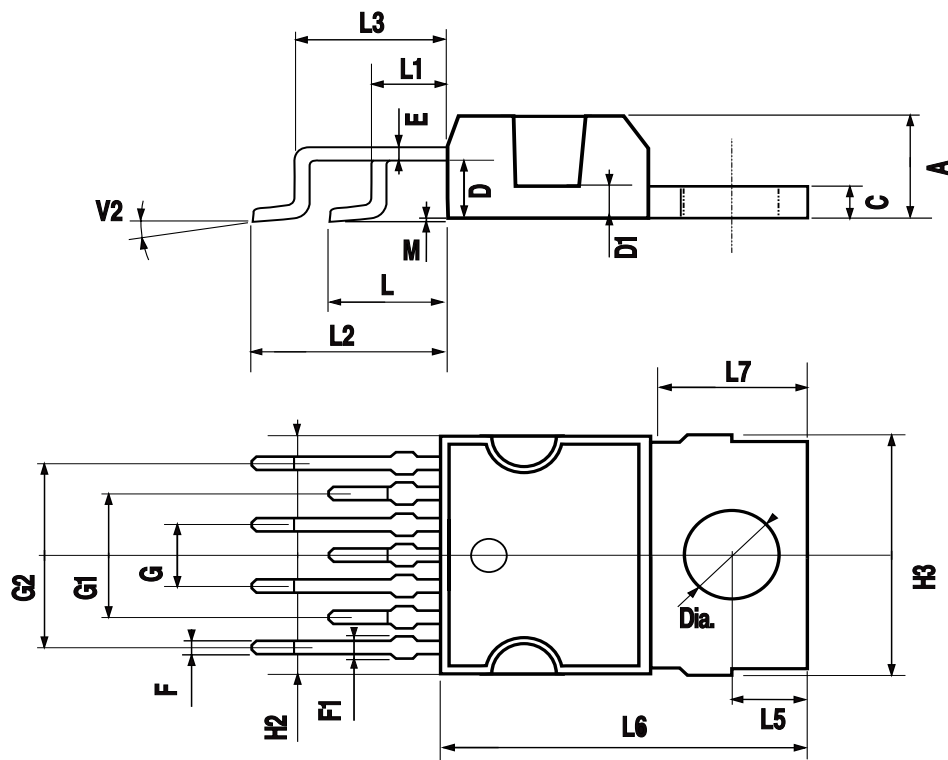
- 1) Use always 100nF filtering capacitor close to the supply pins of each IC.
- 2) The L3235N bias resistor (RR) should be connected close to the corresponding pins of L3235N (REF and AGND).

| DIM. | mm | | | inch | | |
|------|---------|------|------|-------|-------|-------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 4.8 | | | 0.189 |
| C | | | 1.37 | | | 0.054 |
| D | 2.4 | | 2.8 | 0.094 | | 0.110 |
| D1 | 1.2 | | 1.35 | 0.047 | | 0.053 |
| E | 0.35 | | 0.55 | 0.014 | | 0.022 |
| F | 0.6 | | 0.8 | 0.024 | | 0.031 |
| F1 | | | 0.9 | | | 0.035 |
| G | 2.41 | 2.54 | 2.67 | 0.095 | 0.100 | 0.105 |
| G1 | 4.91 | 5.08 | 5.21 | 0.193 | 0.200 | 0.205 |
| G2 | 7.49 | 7.62 | 7.8 | 0.295 | 0.300 | 0.307 |
| H2 | 9.2 | | 10.4 | 0.362 | | 0.409 |
| H3 | 10.05 | | 10.4 | 0.396 | | 0.409 |
| L | 4.6 | | 5.05 | 0.181 | | 0.198 |
| L1 | 3.9 | 4.1 | 4.3 | 0.153 | 0.161 | 0.170 |
| L2 | 6.55 | 6.75 | 6.95 | 0.253 | 0.265 | 0.273 |
| L3 | 5.9 | 6.1 | 6.3 | 0.232 | 0.240 | 0.248 |
| L5 | 2.6 | 2.8 | 3 | 0.102 | 0.110 | 0.118 |
| L6 | 15.1 | | 15.8 | 0.594 | | 0.622 |
| L7 | 6 | | 6.6 | 0.236 | | 0.260 |
| M | 0.17 | | 0.32 | 0.007 | | 0.012 |
| V2 | 8°(max) | | | | | |
| Dia | 3.65 | | 3.85 | 0.144 | | 0.152 |

OUTLINE AND MECHANICAL DATA



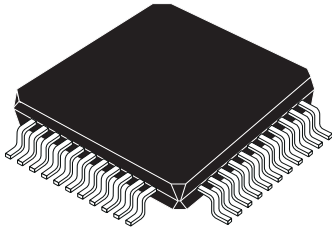
Heptawatt (Surface Mount)



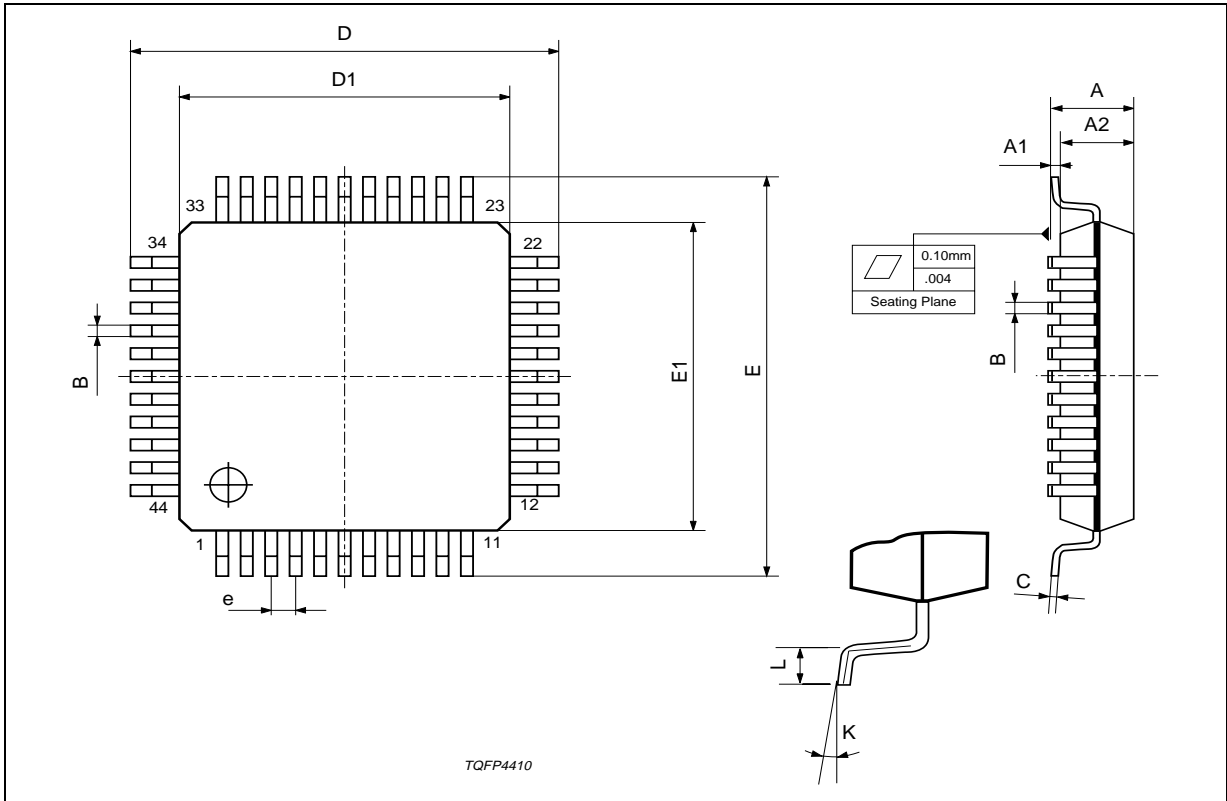
April 1999

| DIM. | mm | | | inch | | |
|------|--------------------------------|-------|------|-------|-------|-------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.60 | | | 0.063 |
| A1 | 0.05 | | 0.15 | 0.002 | | 0.006 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| B | 0.30 | 0.37 | 0.45 | 0.012 | 0.014 | 0.018 |
| C | 0.09 | | 0.20 | 0.004 | | 0.008 |
| D | | 12.00 | | | 0.472 | |
| D1 | | 10.00 | | | 0.394 | |
| D3 | | 8.00 | | | 0.315 | |
| e | | 0.80 | | | 0.031 | |
| E | | 12.00 | | | 0.472 | |
| E1 | | 10.00 | | | 0.394 | |
| E3 | | 8.00 | | | 0.315 | |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | | 1.00 | | | 0.039 | |
| K | 0°(min.), 3.5°(typ.), 7°(max.) | | | | | |

**OUTLINE AND
MECHANICAL DATA**



TQFP44 (10 x 10)



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