

64M X 72 Bits (512MB) 200-Pin DDR SDRAM SO-DIMM with ECC (PC2100)

FEATURES

- PC2100 Compliant
(DDR266A 133MHz-7.5ns@CL = 2)
(DDR266B 133MHz-7.5ns@CL = 2.5)
- 200-Pin SO-DIMM form factor
- Auto and self refresh capability
(8192 cycles/64ms refresh)
- SSTL_2 compatible inputs and outputs
- +2.5V $\pm$ 0.2V V_{DD}
- DDR architecture: Two data accesses per clock cycle, differential clock inputs (CK0 and /CK0), and bi-directional data strobe (DQS)
- Four internal banks for concurrent operation
- Auto Precharge option for each burst access
- Burst lengths: 2, 4, 8
- All inputs are sampled at the positive going edge of the system clock; data referenced to both edges of DQS
- Serial Presence Detect with EEPROM
- ECC
- RoHS Compliant, lead-free version available

GENERAL DESCRIPTION

The SL72A8M64M8M-C75xW(U) is a 64M x 72 bit Double Data Rate (DDR) Synchronous Dynamic RAM (SDRAM) Small-Outline Dual In-line Memory Module (SO-DIMM).

The module consists of nine CMOS 16M x 8 bit x 4 bank DDR SDRAMs in 66-pin 400-mil TSOP II packages mounted on a 200-pin glass epoxy substrate.

A serial EEPROM using the two pin I²C protocol is also mounted to provide for the Serial Presence Detects (SPD). Decoupling capacitors of 0.22 μ F are mounted. Damping resistors are mounted for DQ, DQS, and DM signals. A PLL supplies clocks to the SDRAMs from one clock input.

The module has gold edge connections and is intended for mounting into 200-pin SO-DIMM edge connector sockets keyed for 2.5V.

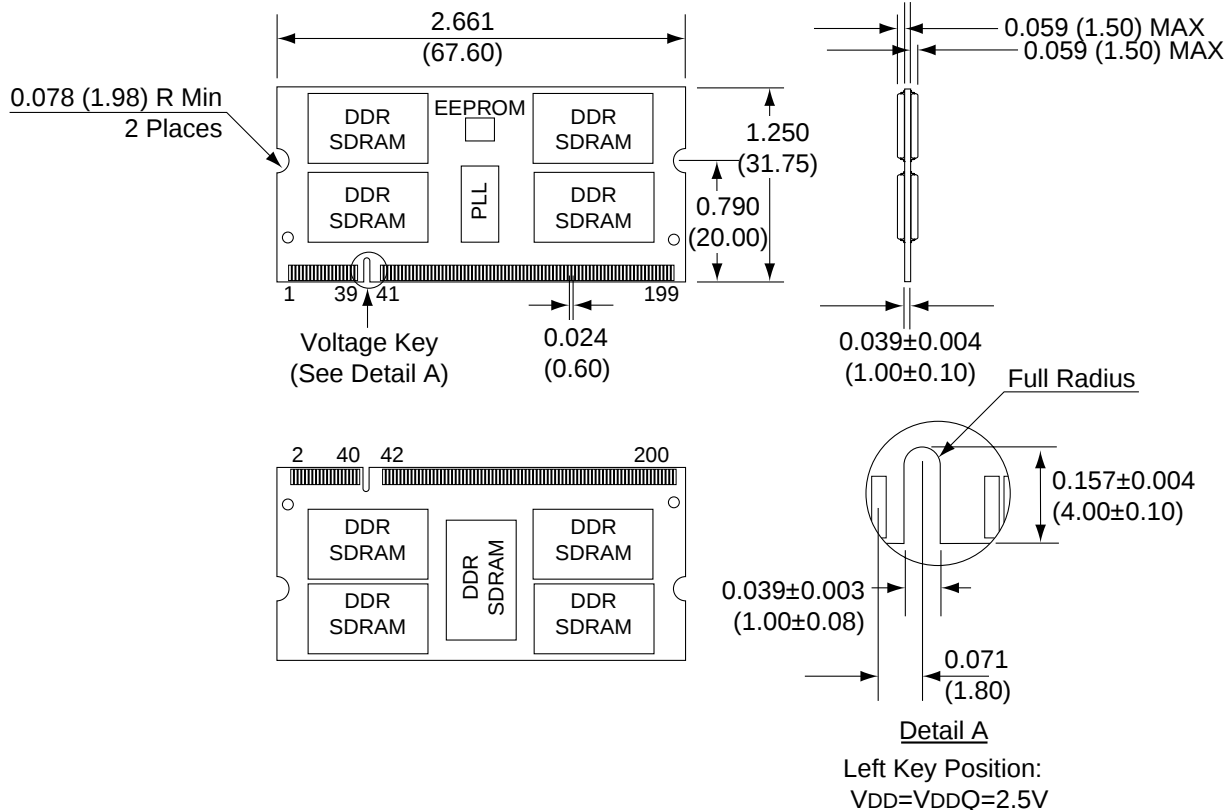
ORDERING INFORMATION

Part Number	CL	MHz	Bandwidth
SL72A8M64M8M-C75DW(U)	2	133	2.1 GB/s
SL72A8M64M8M-C75EW(U)	2.5	133	2.1 GB/s

Note: The "U" suffix added to the part number selects the RoHS Compliant, lead-free module.

PACKAGE DIMENSIONS

Units are in inches (millimeters). Tolerances are ± 0.005 (± 0.127) unless otherwise specified.



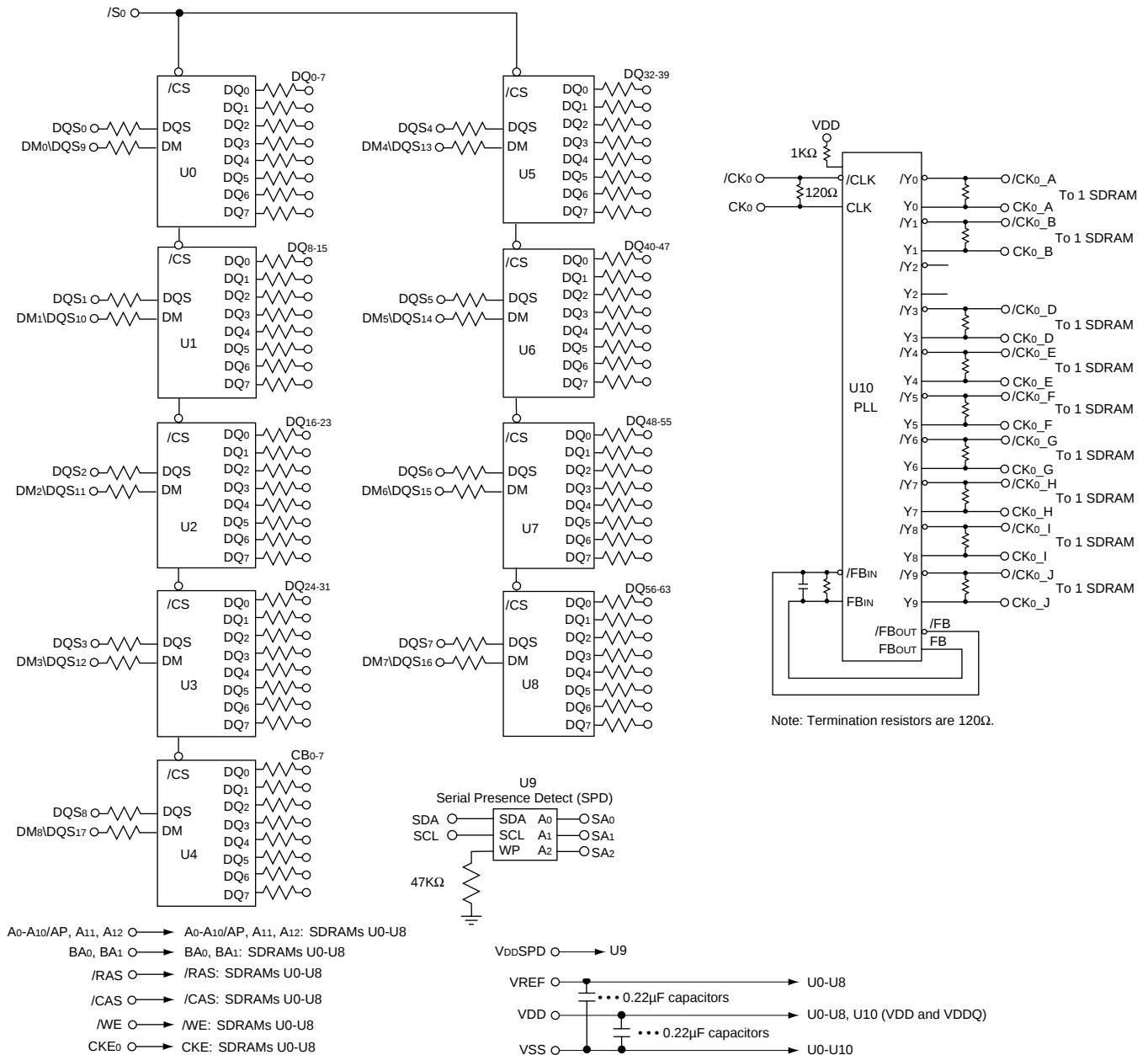
PIN CONFIGURATION (* = Not Used; / = Active Low)**Pinout**

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VREF	2	VREF	51	VSS	52	VSS	101	A ₉	102	A ₈	151	DQ ₄₂	152	DQ ₄₆
3	VSS	4	VSS	53	DQ ₁₉	54	DQ ₂₃	103	VSS	104	VSS	153	DQ ₄₃	154	DQ ₄₇
5	DQ ₀	6	DQ ₄	55	DQ ₂₄	56	DQ ₂₈	105	A ₇	106	A ₆	155	VDD	156	VDD
7	DQ ₁	8	DQ ₅	57	VDD	58	VDD	107	A ₅	108	A ₄	157	VDD	158	/CK ₁ *
9	VDD	10	VDD	59	DQ ₂₅	60	DQ ₂₉	109	A ₃	110	A ₂	159	VSS	160	CK ₁ *
11	DQS ₀	12	DM ₀ \DQS ₉	61	DQS ₃	62	DM ₃ \DQS ₁₂	111	A ₁	112	A ₀	161	VSS	162	VSS
13	DQ ₂	14	DQ ₆	63	VSS	64	VSS	113	VDD	114	VDD	163	DQ ₄₈	164	DQ ₅₂
15	VSS	16	VSS	65	DQ ₂₆	66	DQ ₃₀	115	A ₁₀ \AP	116	BA ₁	165	DQ ₄₉	166	DQ ₅₃
17	DQ ₃	18	DQ ₇	67	DQ ₂₇	68	DQ ₃₁	117	BA ₀	118	/RAS	167	VDD	168	VDD
19	DQ ₈	20	DQ ₁₂	69	VDD	70	VDD	119	/WE	120	/CAS	169	DQS ₆	170	DM ₆ \DQS ₁₅
21	VDD	22	VDD	71	CB ₀	72	CB ₄	121	/S ₀	122	/S ₁ *	171	DQ ₅₀	172	DQ ₅₄
23	DQ ₉	24	DQ ₁₃	73	CB ₁	74	CB ₅	123	DU(A ₁₃)*	124	DU(BA ₂)*	173	VSS	174	VSS
25	DQS ₁	26	DM ₁ \DQS ₁₀	75	VSS	76	VSS	125	VSS	126	VSS	175	DQ ₅₁	176	DQ ₅₅
27	VSS	28	VSS	77	DQS ₈	78	DM ₈ \DQS ₁₇	127	DQ ₃₂	128	DQ ₃₆	177	DQ ₅₆	178	DQ ₆₀
29	DQ ₁₀	30	DQ ₁₄	79	CB ₂	80	CB ₆	129	DQ ₃₃	130	DQ ₃₇	179	VDD	180	VDD
31	DQ ₁₁	32	DQ ₁₅	81	VDD	82	VDD	131	VDD	132	VDD	181	DQ ₅₇	182	DQ ₆₁
33	VDD	34	VDD	83	CB ₃	84	CB ₇	133	DQS ₄	134	DM ₄ \DQS ₁₃	183	DQS ₇	184	DM ₇ \DQS ₁₆
35	CK ₀	36	VDD	85	DU	86	DU(/RESET)*	135	DQ ₃₄	136	DQ ₃₈	185	VSS	186	VSS
37	/CK ₀	38	VSS	87	VSS	88	VSS	137	VSS	138	VSS	187	DQ ₅₈	188	DQ ₆₂
39	VSS	40	VSS	89	CK ₂ *	90	VSS	139	DQ ₃₅	140	DQ ₃₉	189	DQ ₅₉	190	DQ ₆₃
41	DQ ₁₆	42	DQ ₂₀	91	/CK ₂ *	92	VDD	141	DQ ₄₀	142	DQ ₄₄	191	VDD	192	VDD
43	DQ ₁₇	44	DQ ₂₁	93	VDD	94	VDD	143	VDD	144	VDD	193	SDA	194	SA ₀
45	VDD	46	VDD	95	CKE ₁ *	96	CKE ₀	145	DQ ₄₁	146	DQ ₄₅	195	SCL	196	SA ₁
47	DQS ₂	48	DM ₂ \DQS ₁₁	97	DU	98	DU	147	DQS ₅	148	DM ₅ \DQS ₁₄	197	VDDSPD	198	SA ₂
49	DQ ₁₈	50	DQ ₂₂	99	A ₁₂	100	A ₁₁	149	VSS	150	VSS	199	VDDID*	200	DU

Pin Description

Pin Symbol	Pin Function	Pin Symbol	Pin Function
CK(0:2)	Clock inputs, positive line	DQ(0:63)	Data input/output
/CK(0:2)	Clock inputs, negative line	CB(0:7)	Data check bits input/output
CKE(0:1)	Clock enables	DM(0:8)\DQS(9:17)	Low data masks/high data strobes
/RAS	Row address strobe	DQS(0:8)	Low data strobes
/CAS	Column address strobe	/RESET	Register initialization
/WE	Write enable	VDD	Core power
/S(0:1)	Chip selects	VSS	Ground
A(0:9,11:13)	Address inputs	VREF	Input/output reference
A ₁₀ /AP	Address input/Autoprecharge	VDDSPD	SPD power (2.2V to 5.5V)
BA(0:2)	SDRAM bank address	VDDID	VDD identification flag
SCL	SPD clock input		
SDA	SPD data input/output	DU	Don't Use
SA(0:2)	SPD address		

FUNCTIONAL BLOCK DIAGRAM



- Notes: 1. Unless otherwise noted, all series resistors are 22Ω .
 2. DQ wiring may differ from that described in this drawing; however DQ, DQS, DM, CKE, and /S relationships are maintained as shown.

SERIAL PRESENCE DETECT INFORMATION

Serial PD Interface Protocol: I²C; Current sink capability of SDA driver <=3mA; Maximum clock frequency: 100 KHz

Byte #	Function Described	Function Supported	Hex Value
0	# of bytes written into serial memory at module manufacturer	128 bytes	80h
1	Total # of bytes of SPD memory device	256Bytes (2K-bit)	08h
2	Fundamental memory type	DDR SDRAM	07h
3	# of row addresses on this assembly	13	0Dh
4	# of column addresses on this assembly	11	0Bh
5	# of physical banks on this assembly	1 bank	01h
6	Data width of this assembly	72 bits	48h
7	...Data width of this assembly (continued)	—	00h
8	Voltage interface level of this assembly	SSTL 2.5V	04h
9	SDRAM cycle time at CL=2.5 (tCYC)	7.5ns	75h
10	SDRAM access time from clock at CL=2.5 (tAC)	0.75ns	75h
11	DIMM configuration type	ECC	02h
12	Refresh rate/type	7.8μs, Self -refresh	82h
13	SDRAM width	8 bits	08h
14	Error Checking SDRAM data width	8 bits	08h
15	Min. CLK delay for back-to-back rand. col. addr.	tCCD=1 CLK	01h
16	SDRAM device attributes: burst lengths supported	2,4,8	0Eh
17	SDRAM device attributes: # of banks on SDRAM device	4 banks	04h
18	SDRAM device attributes: CAS latency	CAS latency = 2.0, 2.5	0Ch
19	SDRAM device attributes: CS latency	CS latency = 0	01h
20	SDRAM device attributes: Write latency	Write Latency = 1	02h
21	SDRAM module attributes	Differential clock, PLL	24h
22	SDRAM device attributes: general	VDD±0.2V	00h
23	Minimum clock cycle time at CL=2 (tCYC)	7.5ns (DDR266A) 10ns (DDR266B)	75h A0h
24	Max. data access time form clock at CL=2 (tAC)	0.75ns	75h
25	Minimum clock cycle time at CL=1.5 (tCYC)	N/A	00h
26	Max. data access time from clock at CL=1.5 (tAC)	N/A	00h
27	Minimum row precharge time (tRP)	20.0ns	50h
28	Minimum row active to row active delay (tRRD)	15.0ns	3Ch
29	Minumum RAS to CAS (tRCD)	20.0ns	50h
30	Minumum RAS pulse width (tRAS)	45ns	2Dh
31	Module bank density	512MB	80h
32	Min. command and address signal setup time (tAS)	0.9ns	90h
33	Min. command and address signal hold time (tAH)	0.9ns	90h
34	Min. data/data mask signal input setup time (tDS)	0.5ns	50h
35	Min. data/data mask signal input hold time (tDH)	0.5ns	50h

continued on the next page

SERIAL PRESENCE DETECT INFORMATION *(continued)*

Byte #	Function Described	Function Supported	Hex Value
36-40	Superset information (may be used in future)	no superset	00h
41	Row cycle time (trc)	65ns	41h
42	Auto refresh cycle time (trfc)	75ns	4Bh
43	Maximum SDRAM device cycle time (tCK_MAX)	13ns	34h
44	DQS-DQ skew (tdQSQ)	0.50ns	32h
45	SDRAM device data hold skew factor (tQHS)	0.75ns	75h
46-61	Reserved		00h
62	SPD revision	JEDEC 1.0	10h
63	Checksum for bytes 0-62	JEDEC calculation	xxh
64	Manufacturer's JEDEC ID code per JEP-106E	Continuation code	7Fh
65	Man. JEDEC ID code (continued)	STEC's ID	A8h
66-71			00h
72	Manufacturing location	STEC USA or STEC Malaysia	01h (USA) or 02h
73-90	Manufacturer's part number		xxh
91	Revision code of PCB	RevA(01),RevB(02)	00h
92			00h
93	Manufacturing date	Year (BCD)	yy
94		Calender Week (BCD)	w w
95	Assembly serial number	Tester number	ss
96		Serial number (bits 7-0)	ss
97		Serial number (bits 15-8)	ss
98		Serial number (bits 23-16)	ss
99-127	Manufacture's specific data		xxh
128-255		Undefined	00h

ABSOLUTE MAXIMUM RATINGS

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional Operation should be restricted to recommended operating condition. Exposure to higher than recommended voltage for extended periods of time may affect device reliability.

Parameter	Symbol	Value	Unit
Voltage on any pin relative to VSS	V _{IN} , V _{OUT}	−0.5 to +3.6	V
Voltage on VDD supply relative to VSS	VDD	−1.0 to +3.6	V
Voltage on VDDQ supply relative to VSS	VDDQ	−1.0 to 3.6	V
Storage temperature	T _{STG}	−55 to +150	°C
Power Dissipation	P _D	13.5	W
Short circuit current	I _{OS}	50	mA

POWER and DC OPERATING CONDITIONS (SSTL_2 IN/OUT)

Recommended operating conditions (Voltage referenced to VSS=0V. T_A=0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage (for device with a nominal VDD of 2.5V)	VDD	2.3	2.7	V	
I/O Supply voltage	VDDQ	2.3	2.7	V	
I/O Reference voltage	VREF	VDDQ/2-50mV	VDDQ/2+50mV	V	1
I/O Termination voltage (system)	VTT	VREF−0.04	VREF+0.04	V	2
Input logic high voltage	V _{IH} (DC)	VREF+0.15	VDDQ+0.3	V	4
Input logic low voltage	V _{IL} (DC)	−0.3	VREF−0.15	V	4
Input voltage level, CK and /CK	V _{IN} (DC)	−0.3	VDDQ+0.3	V	
Input differential voltage, CK and /CK	V _{ID} (DC)	0.3	VDDQ+0.6	V	3
Input crossing point voltage, CK and /CK	V _{IX} (DC)	1.15	1.35	V	5
Input leakage current	I _L	−18	18	μA	
Output leakage current	I _{OZ}	−5	5	μA	
Output high current (V _{OUT} =VTT+0.84V) (Normal strength driver)	I _{OH}	−16.8		mA	
Output low current (V _{OUT} =VTT−0.84V) (Normal strength driver)	I _{OL}	16.8		mA	
Output high current (V _{OUT} =VTT+0.45V) (Half strength driver)	I _{OH}	−9		mA	
Output low current (V _{OUT} =VTT−0.45V) (Half strength driver)	I _{OL}	9		mA	

- Includes ± 25mV margin for DC offset on VREF, and a combined total of ± 50mV margin for all AC noise and DC offset on VREF, bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on VREF and internal DRAM noise coupled to VREF, both of which may result in VREF noise. VREF should be de-coupled with an inductance of ≤ 3nH.
- VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF
- V_{ID} is the magnitude of the difference between the input level on CK and the input level on /CK.
- These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a VREF envelop that has been bandwidth limited to 200MHZ.
- The value of V_{IX} is expected to equal 0.5*VDDQ of the transmitting device and must track variations in the dc level of the same.
- These characteristics obey the SSTL-2 class II standards.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted; Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.)

Parameter/Condition	Symbol	Max	Units
OPERATING CURRENT: One bank; Active-Precharge; $t_{RC} = t_{RC}(\text{MIN})$; $t_{CK} = t_{CK}(\text{MIN})$; DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles;	IDD0	990	mA
OPERATING CURRENT: One bank; Active-Read-Precharge; Burst = 4; $t_{RC} = t_{RC}(\text{MIN})$; $t_{CK} = t_{CK}(\text{MIN})$; IOU = 0mA; Address and control inputs changing once per clock cycle	IDD1	1215	mA
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; Power-down mode; $t_{CK} = t_{CK}(\text{MIN})$; CKE = (LOW)	IDD2P	45	mA
IDLE STANDBY CURRENT: /CS = HIGH; All banks idle; $t_{CK} = t_{CK}(\text{MIN})$; CKE = HIGH; Address and other control inputs changing once per clock cycle. VIN = VREF for DQ, DQS, and DM	IDD2F	270	mA
ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; Power-down mode; $t_{CK} = t_{CK}(\text{MIN})$; CKE = LOW	IDD3P	270	mA
ACTIVE STANDBY CURRENT: /CS = HIGH; CKE = HIGH; One bank; Active-Precharge; $t_{RC} = t_{RAS}(\text{MAX})$; $t_{CK} = t_{CK}(\text{MIN})$; DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	IDD3N	450	mA
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}(\text{MIN})$; IOU = 0mA	IDD4R	1350	mA
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}(\text{MIN})$; DQ, DM, and DQS inputs changing twice per clock cycle	IDD4W	1395	mA
AUTO REFRESH CURRENT: $t_{RC} = t_{RC}(\text{MIN})$	IDD5	2160	mA
SELF REFRESH CURRENT: CKE ≤ 0.2V	IDD6	45	mA
OPERATING CURRENT: Four bank interleaving READs (BL=4) with auto precharge, $t_{RC} = t_{RC}(\text{MIN})$; $t_{CK} = t_{CK}(\text{MIN})$; Address and control inputs change only during Active READ, or WRITE commands.	IDD7A	3060	mA

AC OPERATING CONDITIONS0

(VDD=VDDQ=2.5V, TA=25°C, f=1MHz)

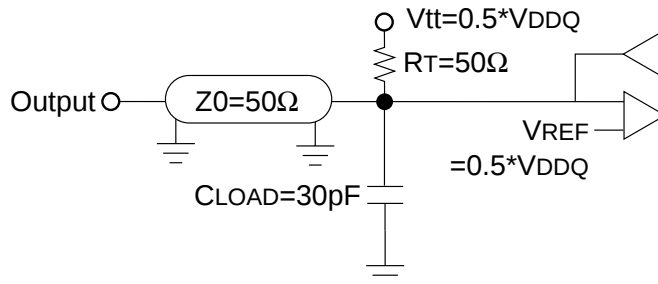
Parameter/Condition	Symbol	Min	Max	Units	Note
Input High (Logic 1) Voltage, DQ, DQS, and DM signals	VIH(AC)	VREF+0.31		V	3
Input Low (Logic 0) Voltage, DQ, DQS, and DM signals	VIL(AC)		VREF-0.31	V	3
Input Differential Voltage, CK and /CK inputs	VID(AC)	0.7	VDDQ+0.6	V	1
Input Crossing Point Voltage, CK and /CK inputs	VIX(AC)	0.5*VDDQ-0.2	0.5*VDDQ+0.2	V	2

- VID is the magnitude of the difference between the input level on CK and the input on /CK.
- The value of V IX is expected to equal 0.5*V DDQ of the transmitting device and must track variations in the DC level of the same.
- These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relation to a Vref envelope that has been bandwidth limited 20MHz.

AC OPERATING TEST CONDITIONS

($V_{DD}=V_{DDQ}=2.5V$, $T_A=0^{\circ}C$ to $70^{\circ}C$)

Parameter	Value	Unit
Input reference voltage for Clock	$0.5 \cdot V_{DDQ}$	V
Input signal maximum peak swing	1.5	V
Input signal minimum slew rate	0.5	V/ns
Input levels (V_{IH}/V_{IL})	$V_{REF}+0.31/V_{REF}-0.31$	V
Input timing measurement ref. level	V_{REF}	V
Output timing measurement ref. level	V_{TT}	V
Output load condition	See Load Circuit	



Output Load Circuit (SSTL_2)

INPUT/OUTPUT CAPACITANCE

($V_{DD}=V_{DDQ}=2.5V$, $T_A=25^{\circ}C$, $f=1MHz$)

Parameter	Symbol	Max	Units
Input Capacitance (A_0 - A_{12} , BA_0 , BA_1 , $/RAS$, $/CAS$, $/WE$)	C_{IN1}	47	pF
Input Capacitance (CKE_0)	C_{IN2}	47	pF
Input Capacitance ($/S_0$)	C_{IN3}	47	pF
Input Capacitance (CK_0 , $/CK_0$)	C_{IN4}	15	pF
Data and DQS I/O Capacitance (DQ_0 - DQ_{63} , CB_0 - CB_7 , DQS_0 - DQS_{17})	C_{OUT}	10	pF
Input Capacitance (DM_0 - DM_8)	C_{IN5}	10	pF

AC TIMING PARAMETERS (These AC characteristics were tested on the component.)

Symbol	Parameter	Min	Max	Unit	Note
tRC	Row cycle time	65		ns	
tRFC	Refresh row cycle time	75		ns	
tRAS	Row active time	45	120K	ns	
tRCD	/RAS to /CAS delay	20		ns	
tRP	Row precharge time	20		ns	
tRRD	Row active to Row active delay	15		ns	
tWR	Write recovery time	2		tCK	
tCDLR	Last data in to Read command	1		tCK	
tCCD	Col. address to Col. address delay	1		tCK	
tCK	Clock cycle time CL=2.0 (DDR266A/DDR266B)	7.5/10	13	ns	5
	Clock cycle time CL=2.5	7.5	13	ns	5
tCH	Clock high level width	0.45	0.55	tCK	
tCL	Clock low level width	0.45	0.55	tCK	
tDQSCK	DQS-out access time from CK, /CK	-0.75	+0.75	ns	
tAC	Output data access time from CK, /CK	-0.75	+0.75	ns	
tDQSQ	Data strobe edge to output data edge		+0.5	ns	5
tRPRE	Read Preamble	0.9	1.1	tCK	
tRPST	Read Postamble	0.4	0.6	tCK	
tDQSS	CK to valid DQS-in	0.75	1.25	tCK	
tWPRES	DQS-in setup time	0		ns	2
tWPREH	DQS-in hold time	0.25		tCK	
tDSS	DQS falling edge to CK rising-setup time	0.2		tCK	
tDSH	DQS falling edge from CK rising-hold time	0.2		tCK	
tDQSH	DQS-in high level width	0.35		tCK	
tDQSL	DQS-in low level width	0.35		tCK	
tDSC	DQS-in cycle time	0.9	1.1	tCK	
tIS	Address and Control Input setup time	0.9		ns	6
tIH	Address and Control Input hold time	0.9		ns	6
tHZ	Data-out high impedance time from CK,/CK	tACmin -400ps		ps	
tLZ	Data-out low impedance time from CK,/CK	tACmin -400ps		ps	
tSL(I)	Input Slew Rate (for input only pins)	0.5		V/ns	6
tSL(IO)	Input Slew Rate (for I/O pins)	0.5		V/ns	7
tSL(O)	Output Slew Rate	1.0	4.5	V/ns	10
tSLMR	Output Slew Rate Matching Ratio (rise to fall)	0.67	1.5	Ratio	
tMRD	Mode register set cycle time	15		ns	
tDS	DQ and DM setup time to DQS	0.5		ns	7,8,9
tDH	DQ and DM hold time to DQS	0.5		ns	7,8,9
tDIPW	DQ and DM input pulse width	1.75		ns	
tPDEX	Power down exit time	7.5		ns	
tXSNR	Exit self refresh to non-read command	75		ns	
tXSA	Exit self refresh to bank active command	75		ns	4
tXSR	Exit self refresh to read command	200		Cycle	
tREF	Refresh interval time	7.8		µs	1
tQH	Output DQS valid window	tHPmin -tQHS		ns	
tHP	Clock half period	tCLmin or tCHmin		ns	
tQHS	Data hold skew factor		0.75	ns	
tWPST	DQS write postamble time	0.4	0.6	tCK	3

Notes:

1. Maximum burst refresh of 8.
2. The specific requirement is that DQS be valid(High or Low) on or before this CK edge. The case shown(DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on tDQSS.
3. The maximum limit for this parameter is not a device limit. The device will operate with a great value for this parameter, but system performance (bus turnaround) will degrade accordingly.
4. A write command can be applied with tRCD satisfied after this command.
5. For registered DIMMs, tCL and tCH are $\geq 45\%$ of the period including both the half period jitter (tJIT(HP)) of the PLL and the half period jitter due to crosstalk (tJIT(crosstalk)) on the DIMM.

6. Input Setup/Hold Slew Rate Derating

Input Setup/Hold Slew Rate	Δt_{IS}	Δt_{IH}
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+50	+50
0.3	+100	+100

This derating table is used to increase t_{IS} / t_{IH} in the case where the input slew rate is below 0.5V/ns. Input setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

7. I/O Setup/Hold Slew Rate Derating

I/O Setup/Hold Slew Rate	Δt_{DS}	Δt_{DH}
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+75	+75
0.3	+150	+150

This derating table is used to increase t_{DS} / t_{DH} in the case where the I/O slew rate is below 0.5V/ns. I/O setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

8. I/O Setup/Hold Plateau Derating

I/O Input Level	Δt_{DS}	Δt_{DH}
(mV)	(ps)	(ps)
± 280	+50	+50

This derating table is used to increase t_{DS}/t_{DH} in the case where the input level is flat below VREF $\pm$ 310mV for a duration of up to 2ns.

9. I/O Delta Rise/Fall Rate(1/slew-rate) Derating

Delta Rise/Fall Rate	Δt_{DS}	Δt_{DH}
(ns/V)	(ps)	(ps)
0	0	0
± 0.25	+50	+50
± 0.5	+100	+100

This derating table is used to increase t_{DS}/t_{DH} in the case where the DQ and DQS slew rates differ. The Delta Rise/Fall Rate is calated as 1/SlewRate1-1/SlewRate2. For example, if slew rate 1 = 5V/ns and slew rate 2 = .4V/ns then the Delta Rise/Fall Rate = -0/5ns/V. Input S/H slew rate based on larger of AC-AC delta rise/fall rate and DC-DC delta rise/fall rate.

10. This parameter is for system simulation purpose. It is guaranteed by design.

REVISION HISTORY

Rev. Change Description from Previous Revision

- 103 03/24/2004. Component-based specs added.
- 104 03/25/2004. Board updated from PCB 955 (1.400") to PCB 1195 (1.250").
- 105 04/12/2004. CK1 and CK2 termination removed from block. SPD bytes 62, 72, and 91 corrected.
- 106 10/13/2006. U option added.
- 107 07/30/2007. Logo updated. Byte 72 of SPD updated to include Malaysia.

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