

General Description

The AO4478 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. This device is suitable for use as general purpose, PWM and a load switch applications.

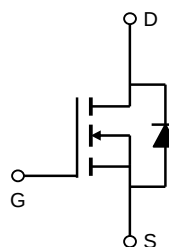
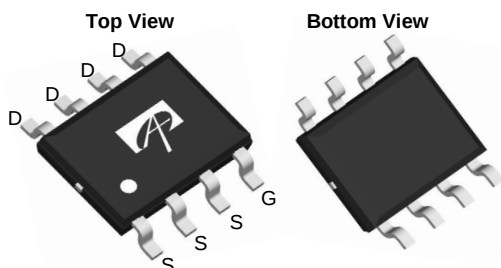
Product Summary

V_{DS} (V) = 30V
 I_D = 9A (V_{GS} = 10V)
 $R_{DS(ON)}$ <19m Ω (V_{GS} = 10V)
 $R_{DS(ON)}$ <26m Ω (V_{GS} = 4.5V)

100% UIS Tested
 100% Rg Tested



SOIC-8



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 25	V
Continuous Drain Current	I_D	9.0	A
$T_A=25^\circ\text{C}$		7.0	
Pulsed Drain Current ^C	I_{DM}	60	
Avalanche Current ^C	I_{AR}	17	
Repetitive avalanche energy $L=0.1\text{mH}^C$	E_{AR}	14	mJ
Power Dissipation ^B	P_D	3.1	W
$T_A=25^\circ\text{C}$		2.0	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	31	40	$^\circ\text{C/W}$
$t \leq 10\text{s}$		59	75	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^{AD}	$R_{\theta JA}$	16	24	$^\circ\text{C/W}$
Steady-State				
Maximum Junction-to-Lead ^C	$R_{\theta JL}$			$^\circ\text{C/W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±25V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =250μA	1	1.6	2	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	60			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =9A T _J =125°C		16 25	19 30	mΩ
		V _{GS} =4.5V, I _D =8A		21	26	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =10A		24		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.70	1	V
I _S	Maximum Body-Diode Continuous Current				4	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz		466	560	pF
C _{oss}	Output Capacitance			90		pF
C _{rss}	Reverse Transfer Capacitance			61		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		3.7	5.6	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =9A		9.3	11	nC
Q _{g(4.5V)}	Total Gate Charge			4.3	5.2	nC
Q _{gs}	Gate Source Charge			1		nC
Q _{gd}	Gate Drain Charge			2.3		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =1.65Ω, R _{GEN} =3Ω		5		ns
t _r	Turn-On Rise Time			8		ns
t _{D(off)}	Turn-Off DelayTime			20		ns
t _f	Turn-Off Fall Time			5		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =9A, dI/dt=500A/μs		7.5	9	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =9A, dI/dt=500A/μs		9.8		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150°C, using ≤ 10s junction-to-ambient thermal resistance.

C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.

D. The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

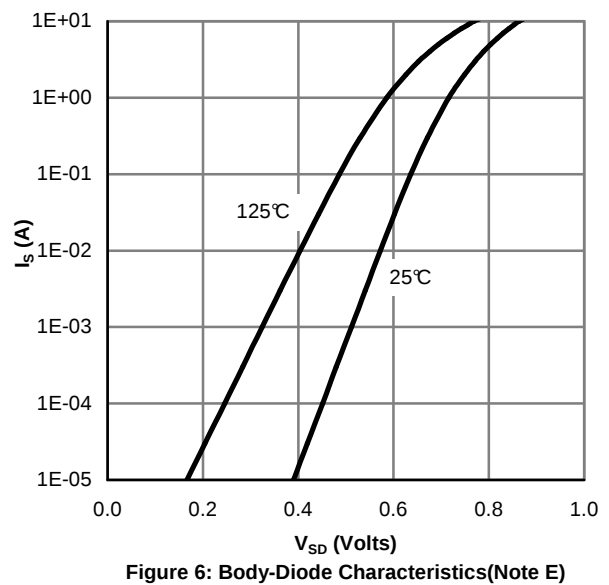
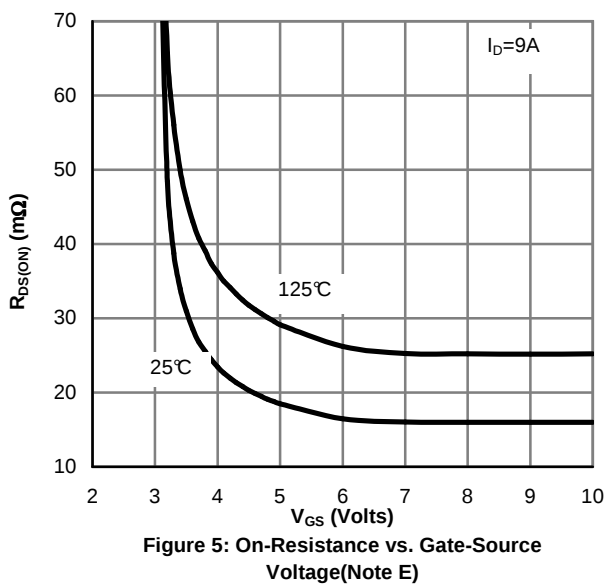
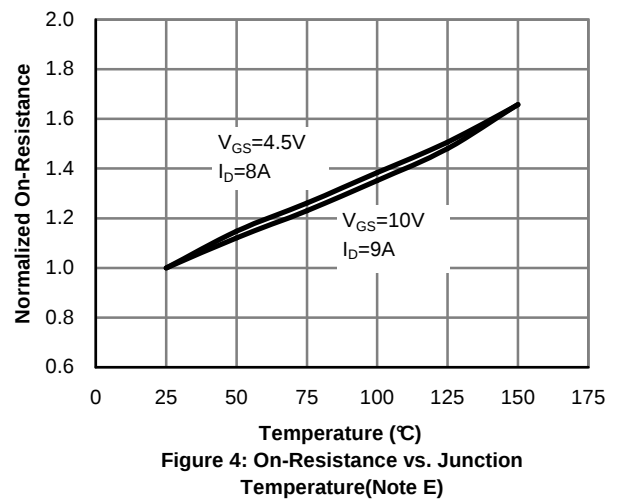
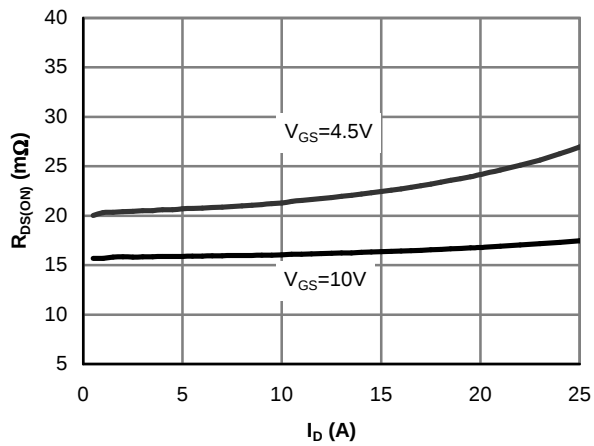
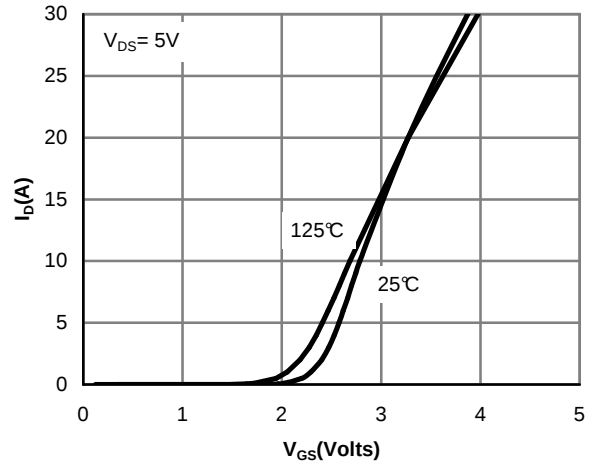
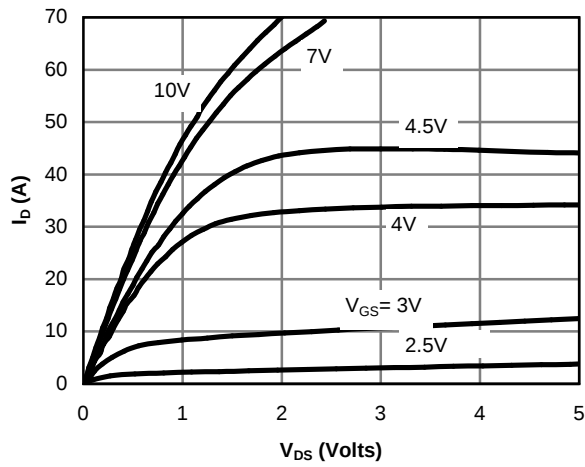
E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T_{J(MAX)}=150°C. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



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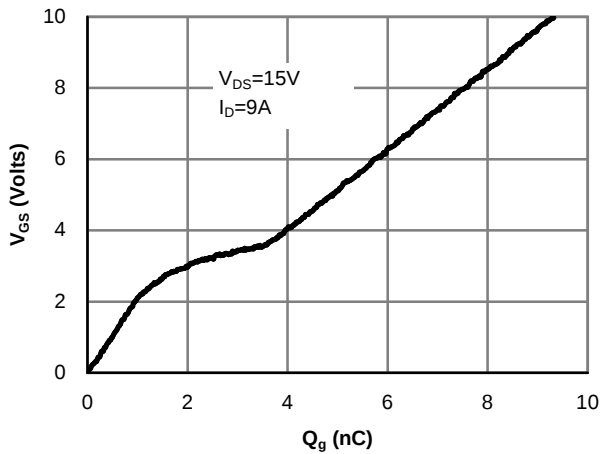


Figure 7: Gate-Charge Characteristics

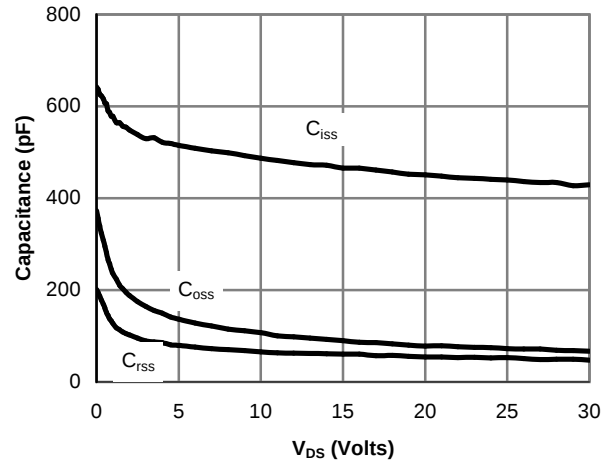


Figure 8: Capacitance Characteristics

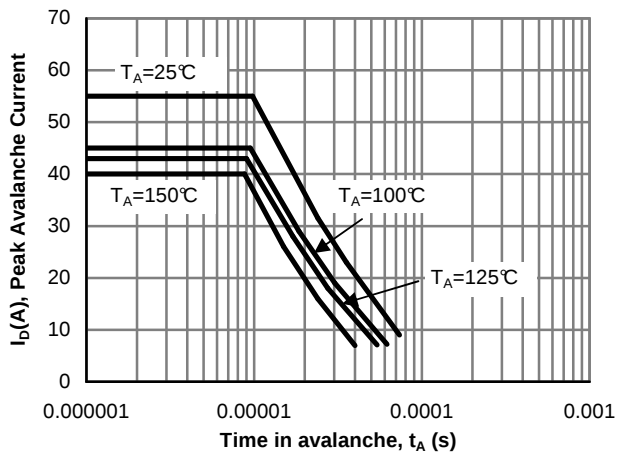


Figure 9: Single Pulse Avalanche capability (Note C)

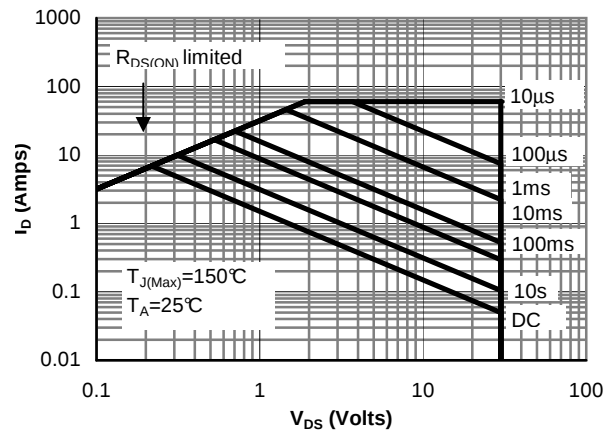


Figure 10: Maximum Forward Biased Safe Operating Area (Note F)

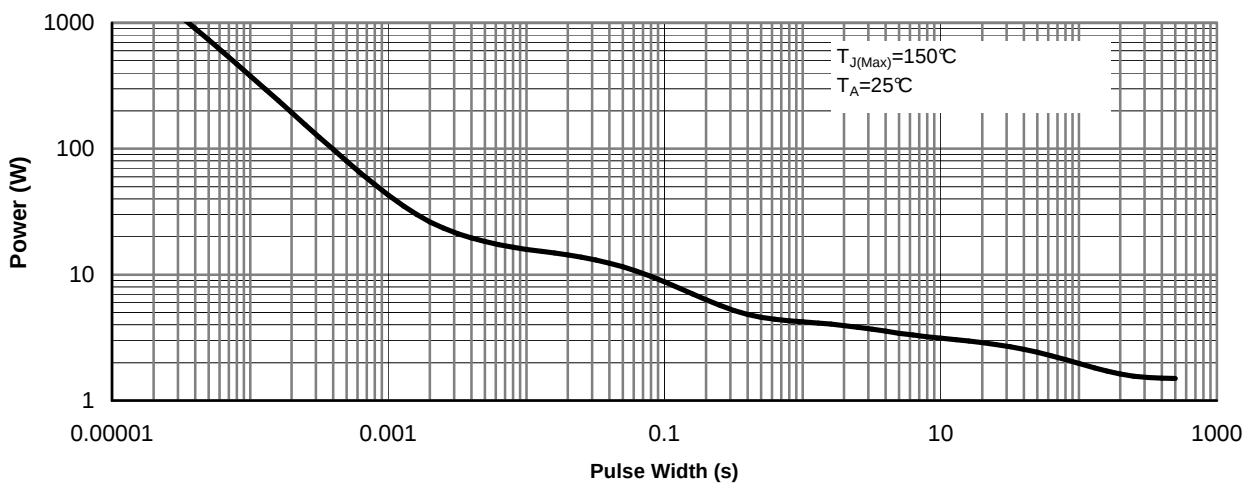


Figure 11: Single Pulse Power Rating Junction-to-Ambient (Note F)

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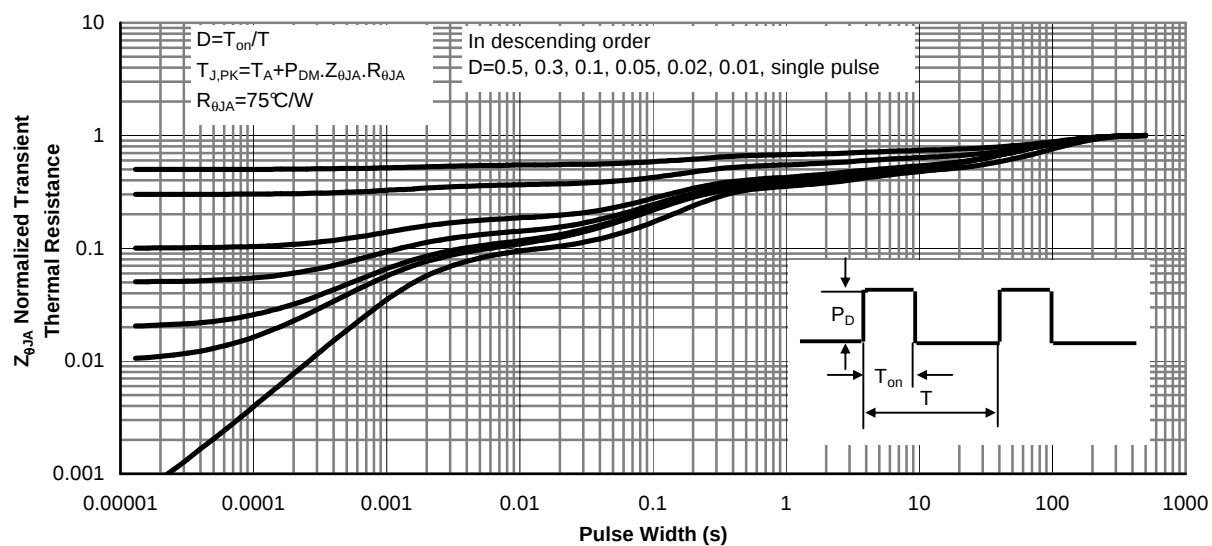
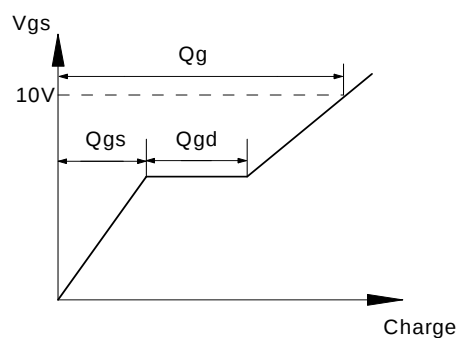
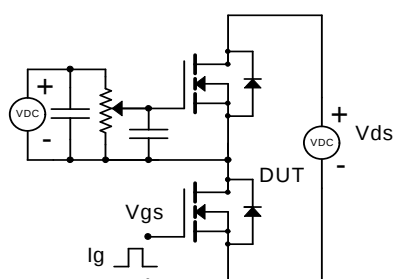
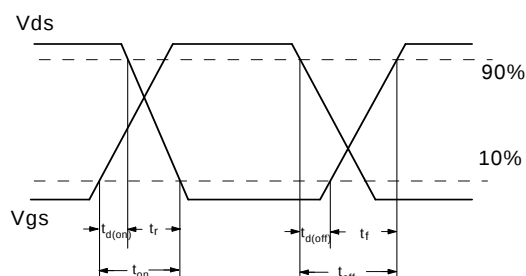
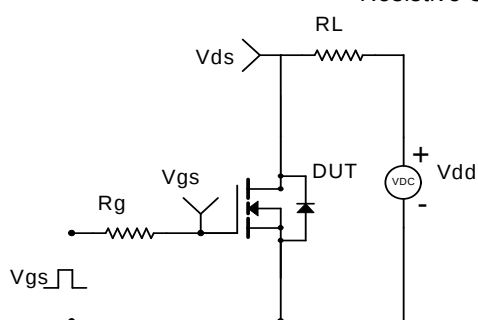


Figure 12: Normalized Maximum Transient Thermal Impedance (Note F)

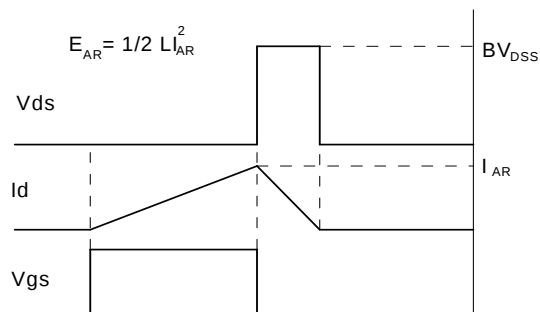
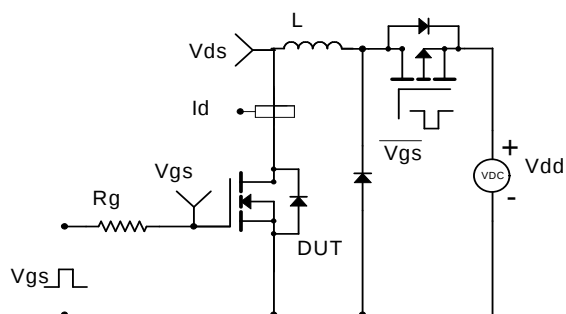
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

