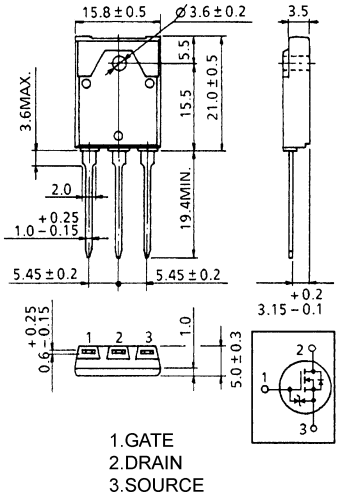
TOSHIBA Field Effect Transistor Silicon N-Channel MOS Type (π-MOSIV)

2SK3880

Switching Regulator Applications

- Low drain-source ON resistance: $R_{DS\ (ON)}$ = 1.35 Ω (typ.)
- High forward transfer admittance: $|Y_{fs}|$ = 5.2 S (typ.)
- Low leakage current: I_{DSS} = 100 μA (max) (V_{DS} = 640 V)
- Enhancement model: V_{th} = 2.0~4.0 V (V_{DS} = 10 V, I_D = 1 mA)

Unit: mm



JEDEC	—
JEITA	—
TOSHIBA	2-16F1B

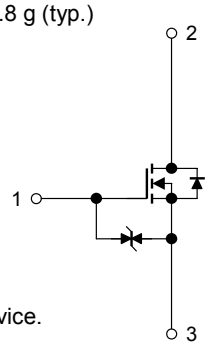
Weight: 5.8 g (typ.)

Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	800	V
Drain-gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	800	V
Gate-source voltage		V_{GSS}	±30	V
Drain current	DC (Note 1)	I_D	6.5	A
	Pulse (Note 1)	I_{DP}	19.5	
Drain power dissipation (Tc = 25°C)		P_D	80	W
Single pulse avalanche energy (Note 2)		E_{AR}	375	mJ
Avalanche current		I_{AR}	6.5	A
Repetitive avalanche energy (Note 3)		E_{AR}	8	mJ
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55~150	°C

Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th\ (ch-c)}$	1.56	°C/W
Thermal resistance, channel to ambient	$R_{th\ (ch-a)}$	41.6	°C/W



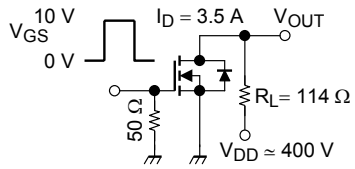
Note 1: Ensure that the channel temperature does not exceed 150°C during use of the device.

Note 2: V_{DD} = 90 V, T_{ch} = 25°C (initial), L = 16.1 mH, R_G = 25 Ω, I_{AR} = 6.5 A

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

This transistor is an electrostatic-sensitive device. Handle with care.

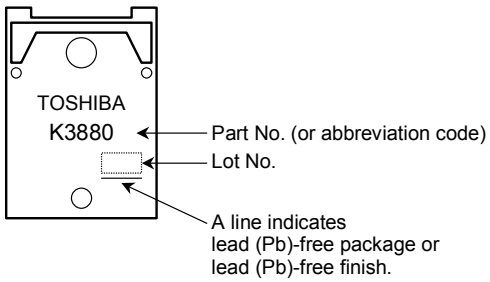
Electrical Characteristics (Ta = 25°C)

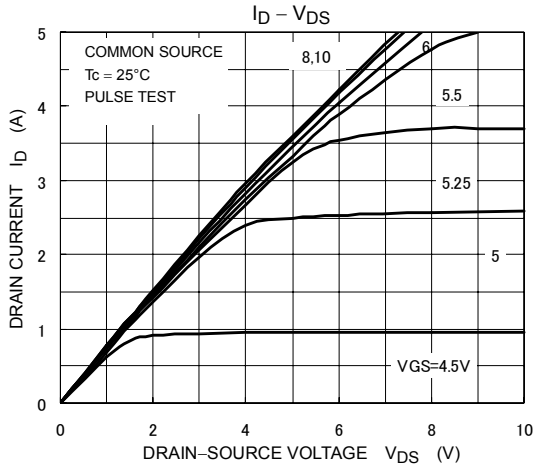
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±25 V, V_{DS} = 0 V	—	—	±10	μA
Drain-source breakdown voltage		$V_{(BR)\ GSS}$	I_G = ±10 μA, V_{DS} = 0 V	±30	—	—	V
Drain cutoff current		I_{DSS}	V_{DS} = 640 V, V_{GS} = 0 V	—	—	100	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	800	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1 mA	2.0	—	4.0	V
Drain-source ON resistance		$R_{DS\ (ON)}$	V_{GS} = 10 V, I_D = 3.5 A	—	1.35	1.7	Ω
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 20 V, I_D = 3.5 A	2.5	5.2	—	S
Input capacitance		C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	—	1500	—	pF
Reverse transfer capacitance		C_{rss}		—	25	—	
Output capacitance		C_{oss}		—	140	—	
Switching time	Rise time	t_r	 Duty ≦ 1%, t_w = 10 μs	—	35	—	ns
	Turn-on time	t_{on}		—	80	—	
	Fall time	t_f		—	50	—	
	Turn-off time	t_{off}		—	220	—	
Total gate charge (gate-source plus gate-drain)		Q_g	V_{DD} ≃ 400 V, V_{GS} = 10 V, I_D = 6.5 A	—	35	—	nC
Gate-source charge		Q_{gs}		—	22	—	
Gate-drain (“Miller”) charge		Q_{gd}		—	13	—	

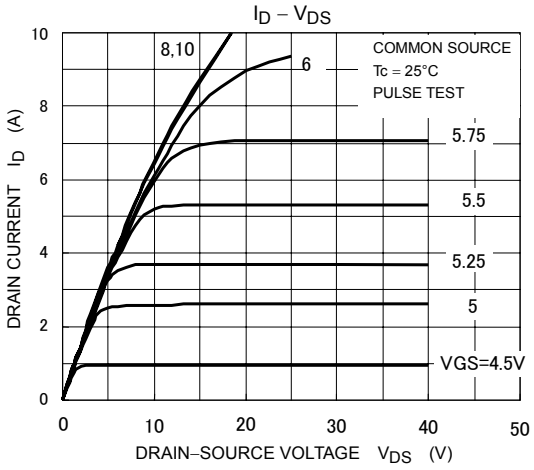
Source-Drain Ratings and Characteristics (Ta = 25°C)

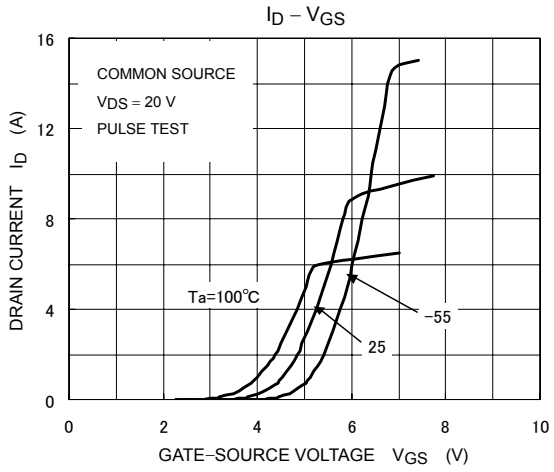
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	6.5	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	19.5	A
Forward voltage (diode)	V_{DSF}	I_{DR} = 6.5 A, V_{GS} = 0 V	—	—	−1.7	V
Reverse recovery time	t_{rr}	I_{DR} = 6.5 A, V_{GS} = 0 V, dI_{DR}/dt = 100 A/μs	—	1200	—	ns
Reverse recovery charge	Q_{rr}		—	11.5	—	μC

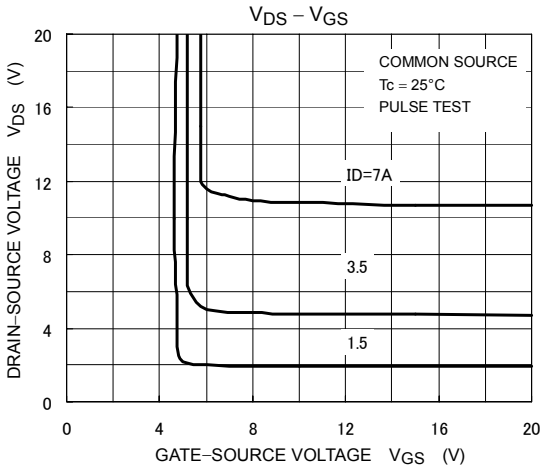
Marking

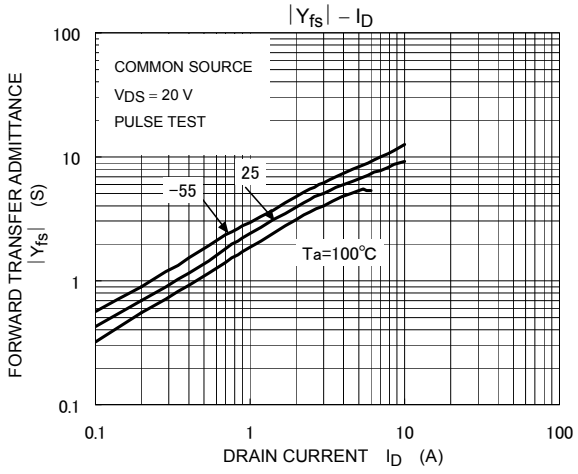


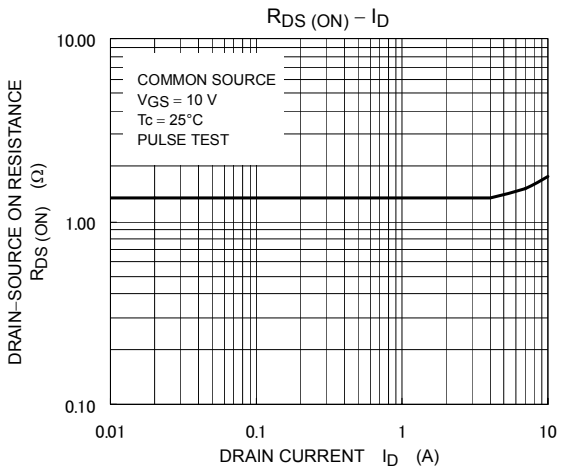

$I_D - V_{DS}$
COMMON SOURCE
Tc = 25°C
PULSE TEST
8,10
6
5.5
5.25
5
VGS=4.5V
DRAIN CURRENT I_D (A)
DRAIN–SOURCE VOLTAGE V_{DS} (V)


$I_D - V_{DS}$
COMMON SOURCE
Tc = 25°C
PULSE TEST
8,10
6
5.75
5.5
5.25
5
VGS=4.5V
DRAIN CURRENT I_D (A)
DRAIN–SOURCE VOLTAGE V_{DS} (V)

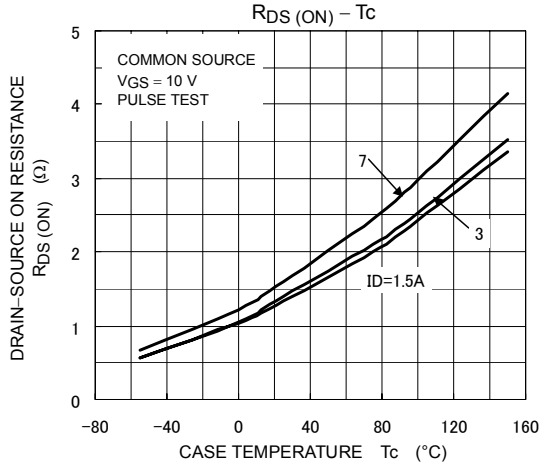

$I_D - V_{GS}$
COMMON SOURCE
VDS = 20 V
PULSE TEST
Ta=100°C
−55
25
DRAIN CURRENT I_D (A)
GATE–SOURCE VOLTAGE V_{GS} (V)


$V_{DS} - V_{GS}$
COMMON SOURCE
Tc = 25°C
PULSE TEST
ID=7A
3.5
1.5
DRAIN–SOURCE VOLTAGE V_{DS} (V)
GATE–SOURCE VOLTAGE V_{GS} (V)

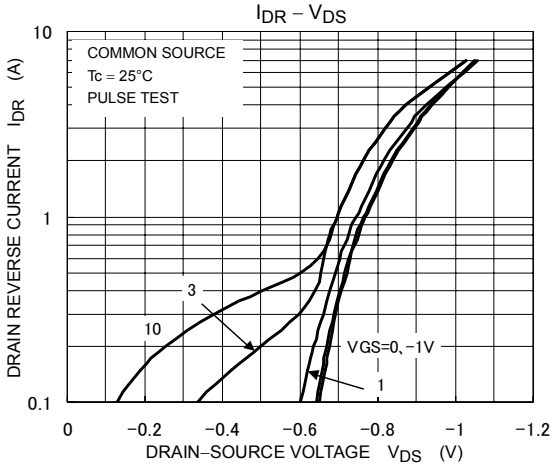

$|Y_{fs}| - I_D$
COMMON SOURCE
VDS = 20 V
PULSE TEST
−55
25
Ta=100°C
FORWARD TRANSFER ADMITTANCE $|Y_{fs}|$ (S)
DRAIN CURRENT I_D (A)


$R_{DS\ (ON)} - I_D$
COMMON SOURCE
VGS = 10 V
Tc = 25°C
PULSE TEST
DRAIN–SOURCE ON RESISTANCE $R_{DS\ (ON)}$ (Ω)
DRAIN CURRENT I_D (A)

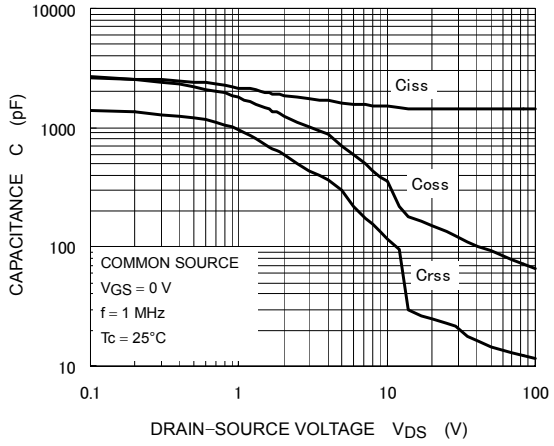
$R_{DS\ (ON)}$ – Tc



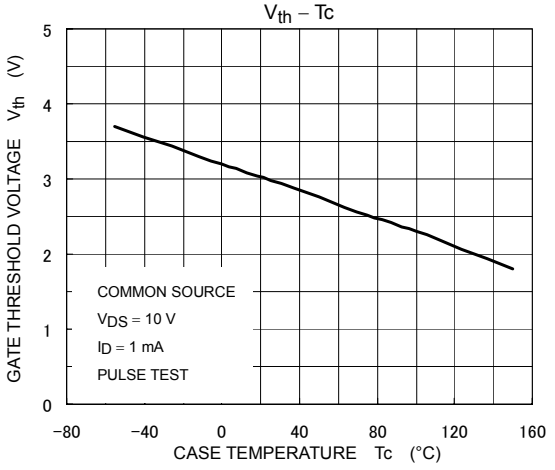
I_{DR} – V_{DS}



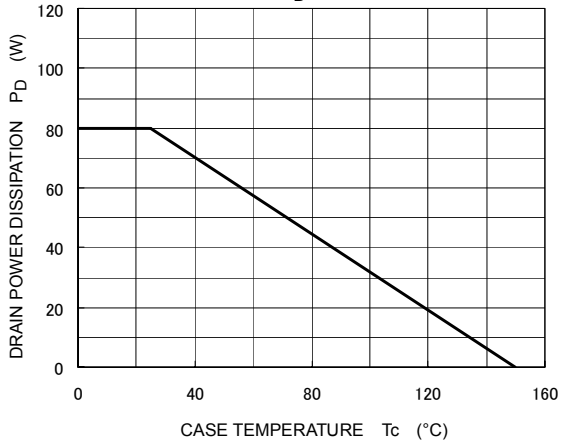
CAPACITANCE – V_{DS}



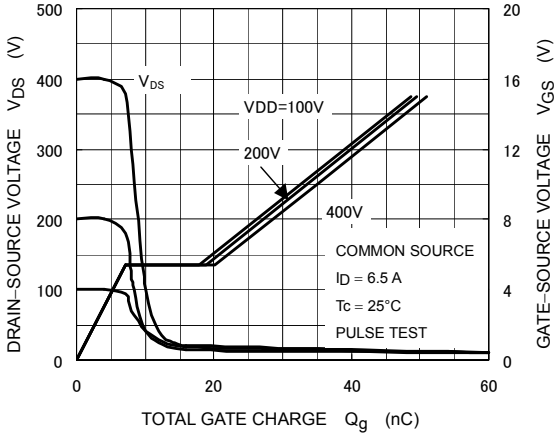
V_{th} – Tc



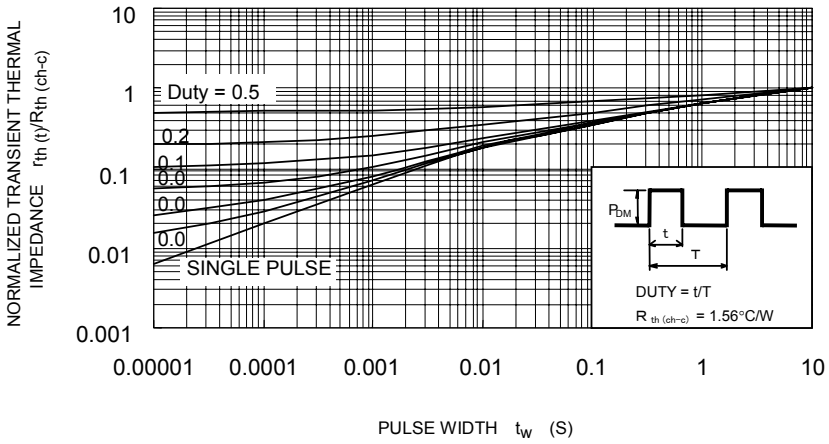
P_D – Tc



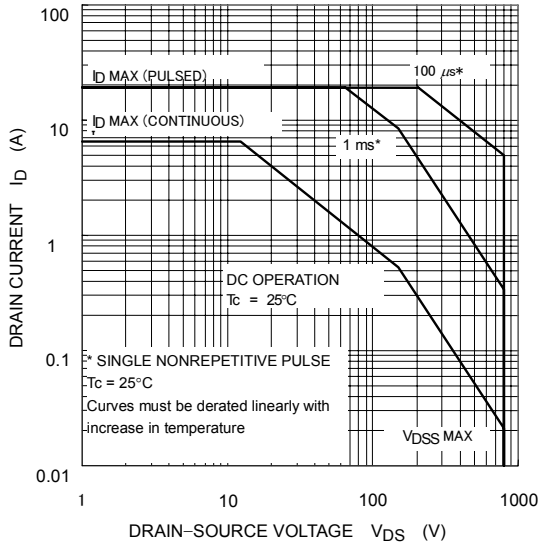
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



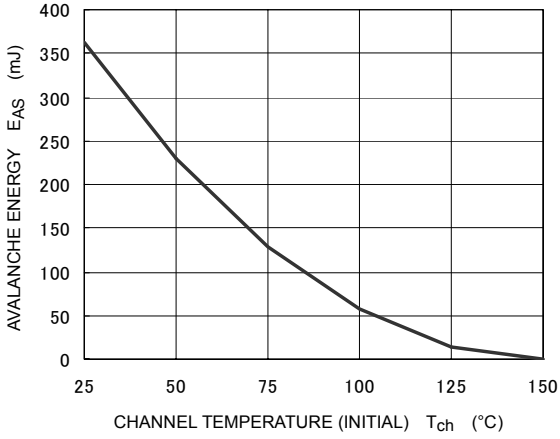
$r_{th} - t_w$

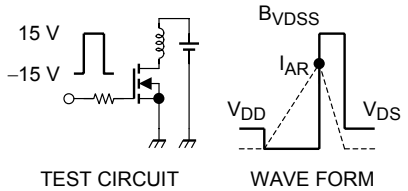


SAFE OPERATING AREA



$E_{AS} - T_{ch}$





TEST CIRCUIT WAVE FORM

R_G = 25 Ω
V_{DD} = 90 V, L = 16.1 mH

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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