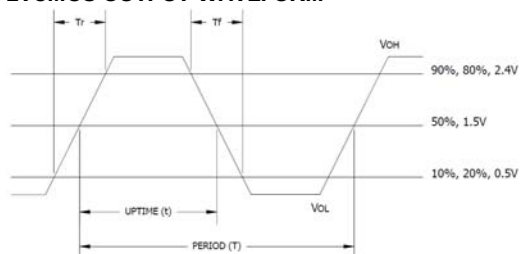
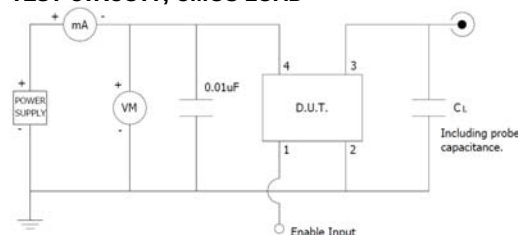


ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Supply Voltage	V_{CC}	-	-0.5	-	4.0	V
Storage Temperature	T_{STG}	-	-40	-	+100	°C
Frequency Range	f_0	-	1.0	-	110	MHz
Frequency Stability [See Note 1 and Ordering Information]	$\Delta f/f_0$	-	-	-	20, 25, 50	± ppm
Aging	$\Delta f/f_0$	@+25°C, 1st year	-	-	3	± ppm
Operating Temperature						
Commercial	T_A	-	-10 -20	+25	+60 +70	°C
Industrial			-40		+85	
Supply Voltage						
Model 625M	V_{CC}	±10%	1.62	1.8	1.98	V
Model 625N			2.25	2.5	2.75	
Model 625L			2.97	3.3	3.63	
Supply Current		$C_L = 15pF$				
Model 625M	I_{CC}	1.0 MHz to 50 MHz	-	-	7	mA
[+1.8V]		50.1 MHz to 110 MHz	-	-	15	
Model 625N		1.0 MHz to 50 MHz	-	-	10	
[+2.5V]		50.1 MHz to 110 MHz	-	-	15	
Model 625L		1.0 MHz to 50 MHz	-	-	15	
[+3.3V]		50.1 MHz to 110 MHz	-	-	20	
Output Load	C_L		-	-	15	pF
Output Voltage Levels						
Logic '1' Level	V_{OH}	CMOS Load	90% V_{CC}	-	-	V
Logic '0' Level	V_{OL}	CMOS Load	-	-	10% V_{CC}	
Output Current						
Logic '1' Level [M,N,L]	I_{OH}	$V_{OH} = 90\%V_{CC}$ (1.8V, 2.5, 3.3V)	-	-	-2, -4, -8	mA
Logic '0' Level [M,N,L]	I_{OL}	$V_{OL} = 10\%V_{CC}$ (1.8V, 2.5, 3.3V)	-	-	+2, +4, +8	
Output Duty Cycle	SYM	@ 50% Level	45	-	55	%
Rise and Fall Time		@ 10% - 90% Levels, $C_L = 15pF$				
Model 625M	T_R, T_F	1.0 MHz to 20 MHz	-	-	5	ns
[+1.8V]		20.1 MHz to 110 MHz	-	-	4	
Model 625N		1.0 MHz to 20 MHz	-	-	4	
[+2.5V]		20.1 MHz to 110 MHz	-	-	3	
Model 625L		1.0 MHz to 20 MHz	-	-	3	
[+3.3V]		20.1 MHz to 110 MHz	-	-	2	
Start Up Time	T_S	Application of V_{CC}	-	2	5	ms
Enable Function						
Enable Input Voltage	V_{IH}	Pin 1 Logic '1', Output Enabled	0.7* V_{CC}	-	-	V
Disable Input Voltage	V_{IL}	Pin 1 Logic '0', Output Disabled	-	-	0.3* V_{CC}	
Enable Time [M,N,L]	T_{PLZ}	Pin 1 Logic '1'	-	-	5	ms
Standby Current	I_{ST}	Pin 1 Logic '0', Output Disabled	-	-	15	µA
Period Jitter, pk-pk	pjpk-pk	-	-	-	40	ps
Period Jitter, RMS	pjrms	-	-	-	25	
Phase Jitter, RMS	tjrms	Bandwidth 12 kHz - 20 MHz	-	-	1	

Notes:

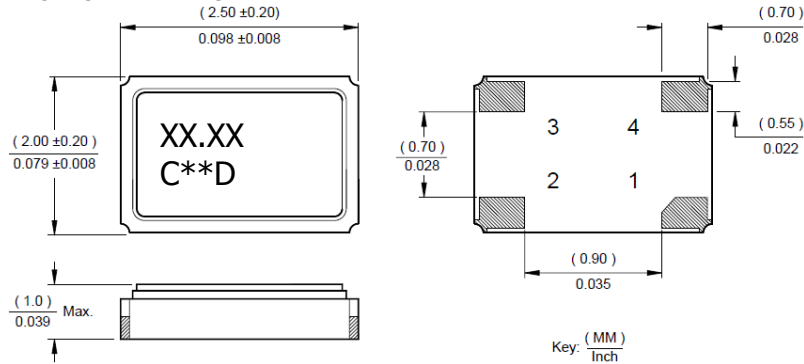
- Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and aging.

LVC MOS OUTPUT WAVEFORM

TEST CIRCUIT, CMOS LOAD

ENABLE TRUTH TABLE

PIN 1	PIN 3
Logic '1'	Output
Open	Output
Logic '0'	High Imp.

MECHANICAL SPECIFICATIONS

PACKAGE DRAWING



MARKING INFORMATION

1. XX.XX – Frequency in MHz.
2. C – CTS and Pin 1 identifier.
3. ** – Manufacturing Site Code.
4. D – Manufacturing Date Code.
[See Table 1 for codes.]
5. Complete CTS part number, frequency value and date code information must appear on reel and carton labels.

NOTES

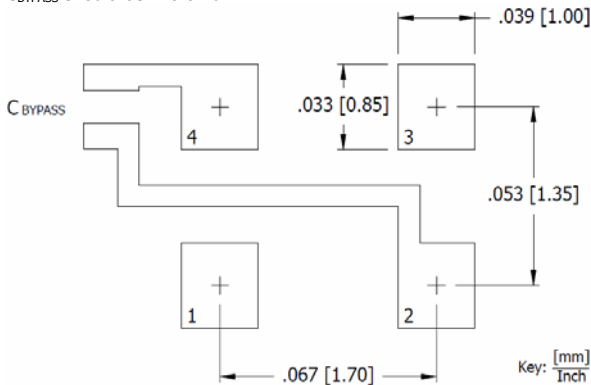
1. Termination pads [e4]. Barrier-plating is nickel [Ni] with gold [Au] flash plate.
2. Reflow conditions per JEDEC J-STD-020; 260°C maximum, 20 seconds.
3. MSL = 1.

TABLE I

YEAR \ MONTH					JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC
2001	2005	2009	2013	2017	A	B	C	D	E	F	G	H	J	K	L	M
2002	2006	2010	2014	2018	N	P	Q	R	S	T	U	V	W	X	Y	Z
2003	2007	2011	2015	2019	a	b	c	d	e	f	g	h	j	k	l	m
2004	2008	2012	2016	2020	n	p	q	r	s	t	u	v	w	x	y	z

SUGGESTED SOLDER PAD GEOMETRY

C_{BYPASS} should be ≥ 0.01 uF.



D.U.T. PIN ASSIGNMENTS

PIN	SYMBOL	DESCRIPTION
1	EOH	Enable
2	GND	Circuit & Package Ground
3	Output	RF Output
4	V _{CC}	Supply Voltage