OCTAL T1/E1 SHORT HAUL ANALOG FRONT END

IDT82V2048L

FEATURES

- Octal T1/E1 short haul analog front end which supports 100 Ω T1 twisted pair, 120 Ω E1 twisted pair and 75 Ω E1 coaxial applications
- Built-in transmit pre-equalization meets G.703 & T1.102
- Digital/Analog LOS detector meets ITU G.775, ETS 300 233 and T1.231
- ITU G.772 non-intrusive monitoring for in-service testing for any one of channel 1 to channel 7
- Low impedance transmit drivers with high-Z
- Selectable hardware and parallel/serial host interface
- Hitless Protection Switching (HPS) for 1 to 1 protection without relays
- JTAG boundary scan for board test
- 3.3 V supply with 5 V tolerant I/O
- Low power consumption
- Operating temperature range: -40°C to +85°C
- Available in 144-pin Thin Quad Flat Pack (TQFP) and 160-pin Plastic Ball Grid Array (PBGA) packages
  Green package options available

FUNCTIONAL BLOCK DIAGRAM

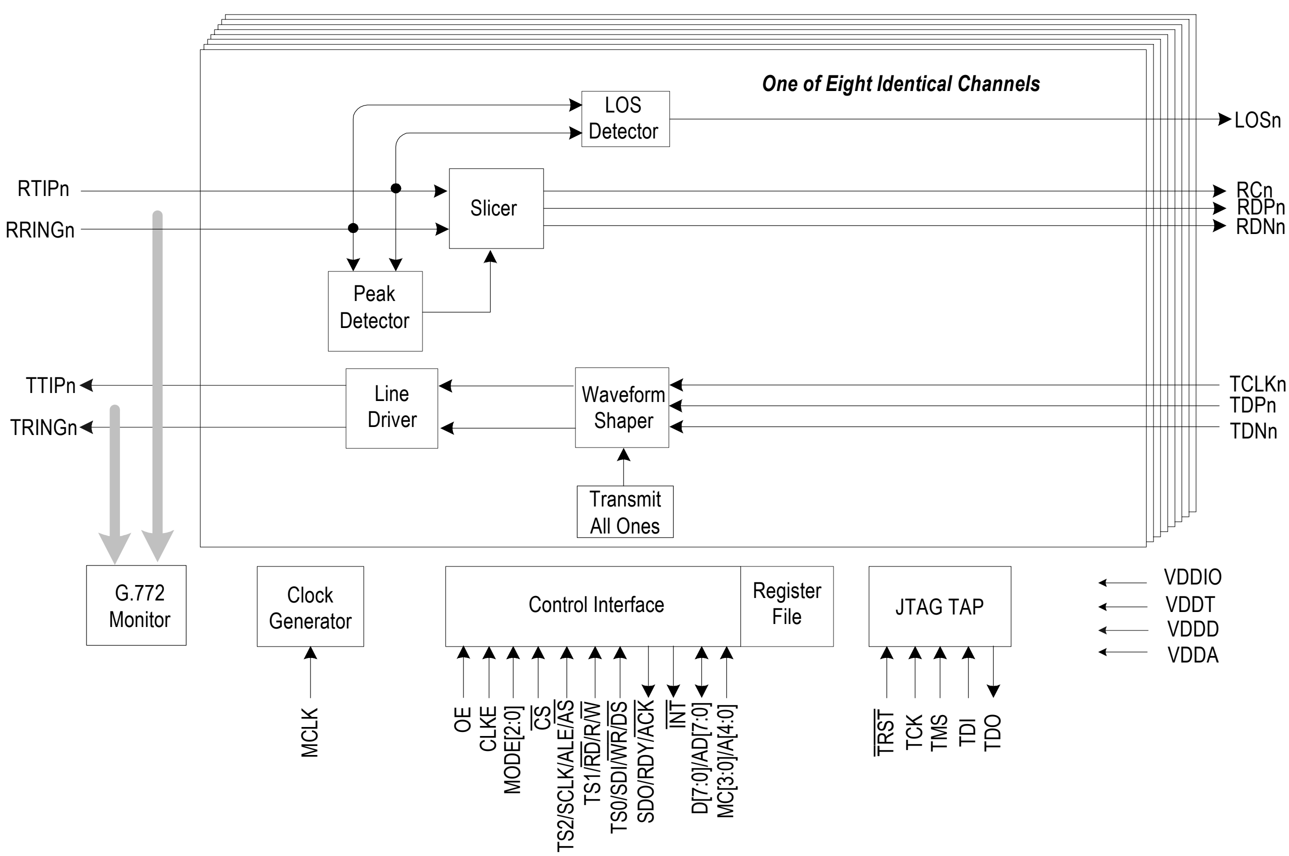


Figure-1 Block Diagram

July, 2005

PIN CONFIGURATIONS

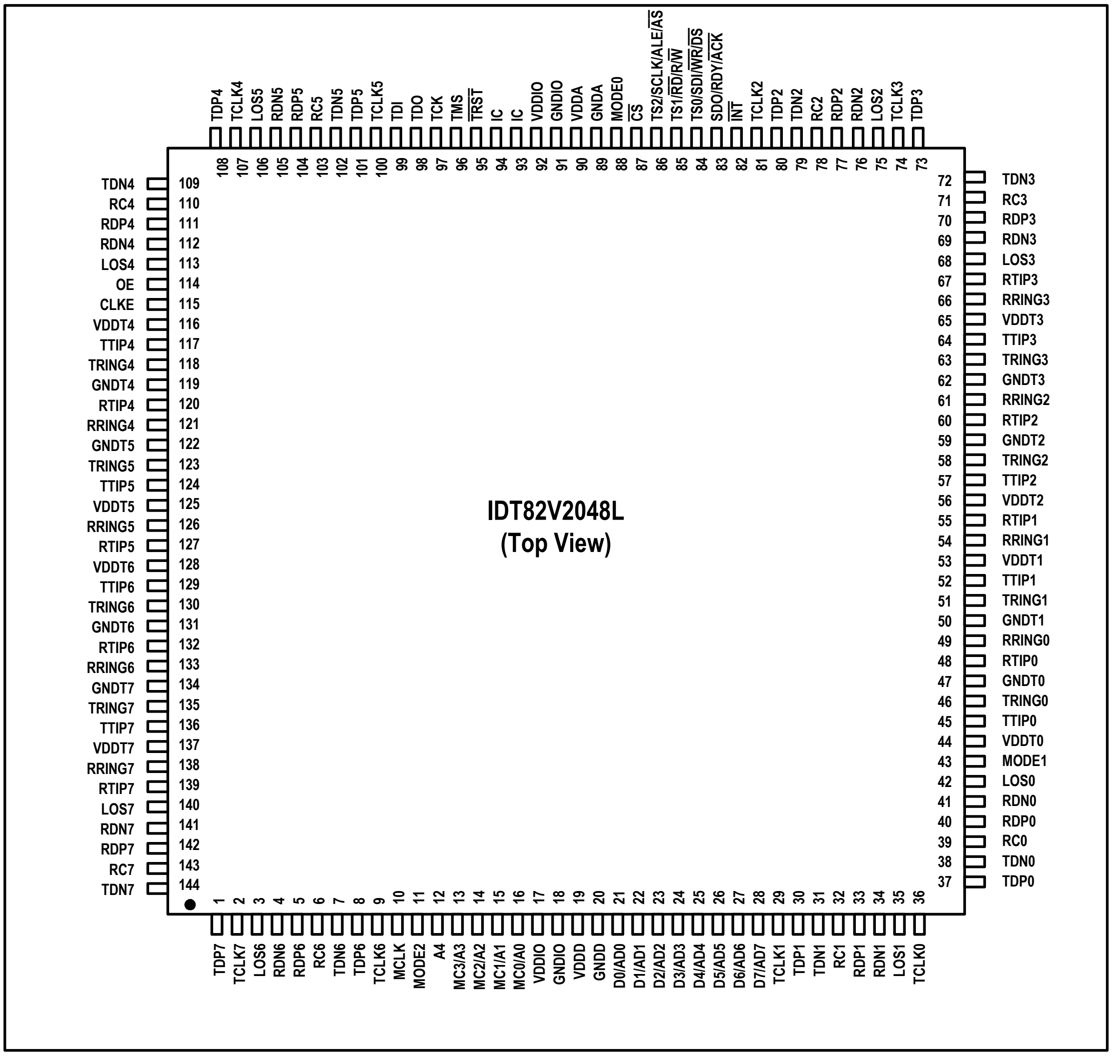


Figure-2 TQFP144 Package Pin Assignment

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	
1	RC7	TCLK7	RC6	TCLK6	MCLK	MC1	VDDIO	VDDD	D6	D7	TCLK1	RC1	TCLK0	RC0	1
2	RDP7	TDP7	RDP6	TDP6	MODE2	MC2	D0	D2	D5	MODE1	TDP1	RDP1	TDP0	RDP0	2
3	RDN7	TDN7	RDN6	TDN6	LOS6	MC3	MC0	D1	D4	LOS1	TDN1	RDN1	TDN0	RDN0	3
4	VDDT7	VDDT7	VDDT6	VDDT6	LOS7	A4	GNDIO	GNDD	D3	LOS0	VDDT1	VDDT1	VDDT0	VDDT0	4
5	TRING7	TTIP7	TRING6	TTIP6							TTIP1	TRING1	TTIP0	TRING0	5
6	GNDT7	GNDT7	GNDT6	GNDT6							GNDT1	GNDT1	GNDT0	GNDT0	6
7	RTIP7	RRING7	RTIP6	RRING6							RRING1	RTIP1	RRING0	RTIP0	7
8	RTIP4	RRING4	RTIP5	RRING5							RRING2	RTIP2	RRING3	RTIP3	8
9	GNDT4	GNDT4	GNDT5	GNDT5							GNDT2	GNDT2	GNDT3	GNDT3	9
10	TRING4	TTIP4	TRING5	TTIP5							TTIP2	TRING2	TTIP3	TRING3	10
11	VDDT4	VDDT4	VDDT5	VDDT5	LOS4	TMS	GNDIO	GNDA	$\overline{CS}$	LOS3	VDDT2	VDDT2	VDDT3	VDDT3	11
12	RDN4	TDN4	RDN5	TDN5	LOS5	TDI	$\overline{TRST}$	MODE0	TS2	LOS2	TDN2	RDN2	TDN3	RDN3	12
13	RDP4	TDP4	RDP5	TDP5	CLKE	TDO	IC	IC	TS1	$\overline{INT}$	TDP2	RDP2	TDP3	RDP3	13
14	RC4	TCLK4	RC5	TCLK5	OE	TCK	VDDIO	VDDA	TS0	SDO	TCLK2	RC2	TCLK3	RC3	14
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	

IDT82V2048L
(Bottom View)

Figure-3 PBGA160 Package Pin Assignment

1 PIN DESCRIPTION

Table-1 Pin Description

Name	Type	Pin No. TQFP144	Pin No. PBGA160	Description
Transmit and Receive Line Interface				
TTIP0 TTIP1 TTIP2 TTIP3 TTIP4 TTIP5 TTIP6 TTIP7 TRING0 TRING1 TRING2 TRING3 TRING4 TRING5 TRING6 TRING7	Analog Output	45 52 57 64 117 124 129 136 46 51 58 63 118 123 130 135	N5 L5 L10 N10 B10 D10 D5 B5 P5 M5 M10 P10 A10 C10 C5 A5	**TTIPn/TRINGn: Transmit Bipolar Tip/Ring for Channel 0~7** These pins are the differential line driver outputs. They will be in high impedance state if pin OE is low or the corresponding pin TCLKn is low (pin OE is global control, while pin TCLKn is per-channel control). In host mode, each pin can be in high impedance by programming a '1' to the corresponding bit in register **OE**[1].
RTIP0 RTIP1 RTIP2 RTIP3 RTIP4 RTIP5 RTIP6 RTIP7 RRING0 RRING1 RRING2 RRING3 RRING4 RRING5 RRING6 RRING7	Analog Input	48 55 60 67 120 127 132 139 49 54 61 66 121 126 133 138	P7 M7 M8 P8 A8 C8 C7 A7 N7 L7 L8 N8 B8 D8 D7 B7	**RTIPn/RRINGn: Receive Bipolar Tip/Ring for Channel 0~7** These pins are the differential line receiver inputs.

1. Register name is indicated by bold capital letter. For example, **OE** indicates Output Enable Register.

Table-1 Pin Description (Continued)

<table>
<tr><th rowspan="2">Name</th><th rowspan="2">Type</th><th colspan="2">Pin No.</th><th rowspan="2">Description</th></tr>
<tr><th>TQFP144</th><th>PBGA160</th></tr>
<tr><td colspan="5">Transmit and Receive Digital Data Interface</td></tr>
<tr><td>TDP0
TDP1
TDP2
TDP3
TDP4
TDP5
TDP6
TDP7

TDN0
TDN1
TDN2
TDN3
TDN4
TDN5
TDN6
TDN7</td><td>I</td><td>37
30
80
73
108
101
8
1

38
31
79
72
109
102
7
144</td><td>N2
L2
L13
N13
B13
D13
D2
B2

N3
L3
L12
N12
B12
D12
D3
B3</td><td>TDPn/TDNn: Positive/Negative Transmit Data for Channel 0~7
The NRZ data to be transmitted for positive/negative pulse is input on this pin. Data on TDPn/TDNn are active high and are sampled on the falling edges of TCLKn.<table><tr><th>TDPn</th><th>TDNn</th><th>Output Pulse</th></tr><tr><td>0</td><td>0</td><td>Space</td></tr><tr><td>0</td><td>1</td><td>Negative Pulse</td></tr><tr><td>1</td><td>0</td><td>Positive Pulse</td></tr><tr><td>1</td><td>1</td><td>Space</td></tr></table></td></tr>
<tr><td>TCLK0
TCLK1
TCLK2
TCLK3
TCLK4
TCLK5
TCLK6
TCLK7</td><td>I</td><td>36
29
81
74
107
100
9
2</td><td>N1
L1
L14
N14
B14
D14
D1
B1</td><td>TCLKn: Transmit Clock for Channel 0~7
The clock of 1.544 MHz (for T1 mode) or 2.048 MHz (for E1 mode) for transmit is input on this pin. The transmit data at TDPn or TDNn is sampled into the device on the falling edges of TCLKn.
Different combinations of TCLKn and MCLK result in different transmit mode. It is summarized as Table-2 System Interface Configuration.</td></tr>
<tr><td>RDP0
RDP1
RDP2
RDP3
RDP4
RDP5
RDP6
RDP7

RDN0
RDN1
RDN2
RDN3
RDN4
RDN5
RDN6
RDN7</td><td>O

High Imped-ance</td><td>40
33
77
70
111
104
5
142

41
34
76
69
112
105
4
141</td><td>P2
M2
M13
P13
A13
C13
C2
A2

P3
M3
M12
P12
A12
C12
C3
A3</td><td>RDPn/RDNn: Positive/Negative Receive Data for Channel 0~7
These pins output the raw RZ sliced data. The active polarity of RDPn/RDNn is determined by pin CLKE. When pin CLKE is low, RDPn/RDNn is active low. When pin CLKE is high, RPDn/RDNn is active high. RDPn/RDNn will remain active during LOS. RDPn/RDNn is set into high impedance when the correspond-ing receiver is powered down.</td></tr>
<tr><td>RC0
RC1
RC2
RC3
RC4
RC5
RC6
RC7</td><td>O

High Imped-ance</td><td>39
32
78
71
110
103
6
143</td><td>P1
M1
M14
P14
A14
C14
C1
A1</td><td>RCn: Receive Pulse for Channel 0~7
RCn is the output of an internal exclusive OR (XOR) which is connected with RDPn and RDNn. The clock is recovered from the signal on RCn. If receiver n is powered down, the corresponding RCn will be in high impedance.</td></tr>
</table>

Table-1 Pin Description (Continued)

<table>
<tr><th rowspan="2">Name</th><th rowspan="2">Type</th><th colspan="2">Pin No.</th><th rowspan="2">Description</th></tr>
<tr><th>TQFP144</th><th>PBGA160</th></tr>
<tr><td>MCLK</td><td>I</td><td>10</td><td>E1</td><td>MCLK: Master Clock
This is an independent, free running reference clock. A clock of 1.544 MHz (for T1 mode) or 2.048 MHz (for E1 mode) is supplied to this pin as the clock reference of the device for normal operation.
When MCLK is low, all the receivers are powered down, and the output pins RCn, RDPn and RDNn are switched to high impedance.
In transmit path, the operation mode is decided by the combination of MCLK and TCLKn (See Table-2 System Interface Configuration for details).
NOTE: Wait state generation via RDY/$\overline{\text{ACK}}$ is not available if MCLK is not provided.</td></tr>
<tr><td>LOS0
LOS1
LOS2
LOS3
LOS4
LOS5
LOS6
LOS7</td><td>O</td><td>42
35
75
68
113
106
3
140</td><td>K4
K3
K12
K11
E11
E12
E3
E4</td><td>LOSn: Loss of Signal Output for Channel 0~7
A high level on this pin indicates the loss of signal when there is no transition over a specified period of time or no enough ones density in the received signal. The transition will return to low automatically when there is enough transitions over a specified period of time with a certain ones density in the received signal. The LOS assertion and desertion criteria are described in 2.4.3 Loss of Signal (LOS) Detection.</td></tr>
<tr><td colspan="5">Hardware/Host Control Interface</td></tr>
<tr><td>MODE2</td><td>I

(Pulled to VDDIO/2)</td><td>11</td><td>E2</td><td>MODE2: Control Mode Select 2[2]
The signal on this pin determines which control mode is selected to control the device:
<table><tr><th>MODE2</th><th>Control Interface</th></tr><tr><td>Low</td><td>Hardware Mode</td></tr><tr><td>VDDIO/2</td><td>Serial Host Interface</td></tr><tr><td>High</td><td>Parallel Host Interface</td></tr></table>Hardware control pins include MODE[2:0], TS[2:0], CLKE and OE.
Serial host Interface pins include $\overline{\text{CS}}$, SCLK, SDI, SDO and $\overline{\text{INT}}$.
Parallel host Interface pins include $\overline{\text{CS}}$, A[4:0], D[7:0], $\overline{\text{WR}}$/DS, $\overline{\text{RD}}$/R/$\overline{\text{W}}$, ALE/$\overline{\text{AS}}$, $\overline{\text{INT}}$ and RDY/$\overline{\text{ACK}}$. The device supports multiple parallel host interface as follows (refer to MODE1 and MODE0 pin descriptions below for details):
<table><tr><th>MODE[2:0]</th><th>Host Interface</th></tr><tr><td>100</td><td>Non-multiplexed Motorola Mode Interface</td></tr><tr><td>101</td><td>Non-multiplexed Intel Mode Interface</td></tr><tr><td>110</td><td>Multiplexed Motorola Mode Interface</td></tr><tr><td>111</td><td>Multiplexed Intel Mode Interface</td></tr></table></td></tr>
<tr><td>MODE1</td><td>I</td><td>43</td><td>K2</td><td>MODE1: Control Mode Select 1[2]
In parallel host mode, the parallel interface operates with separate address bus and data bus when this pin is low, and operates with multiplexed address and data bus when this pin is high.
In serial host mode or hardware mode, this pin should be grounded.</td></tr>
<tr><td>MODE0</td><td>I</td><td>88</td><td>H12</td><td>MODE0: Control Mode Select 0[2]
In parallel host mode, the parallel host interface is configured for Motorola compatible hosts when this pin is low, or for Intel compatible hosts when this pin is high.
In serial host mode or hardware mode, this pin should be grounded.</td></tr>
<tr><td>$\overline{\text{CS}}$</td><td>I

(Pulled to VDDIO/2)</td><td>87</td><td>J11</td><td>$\overline{\text{CS}}$: Chip Select (Active Low)
In host mode, this pin is asserted low by the host to enable host interface. A high to low transition must occur on this pin for each read/write operation and the level must not return to high until the operation is over.
In hardware control mode, this pin should be pulled to VDDIO/2.</td></tr>
</table>

2. In host mode, register **e-AFE** has to be set to ‘FFH’ for proper device operation. See Expanded Register Description on page 28 for more details.

Table-1 Pin Description (Continued)

Name	Type	Pin No.		Description
		TQFP144	PBGA160	
TS2/SCLK/ ALE/$\overline{\text{AS}}$	I	86	J12	**TS2: Template Select 2** In hardware control mode, the signal on this pin is the most significant bit for the transmit template select. Refer to 2.5.1 Waveform Shaper for details. **SCLK: Shift Clock** In serial host mode, the signal on this pin is the shift clock for the serial interface. Data on pin SDO is clocked out on falling edges of SCLK if pin CLKE is high, or on rising edges of SCLK if pin CLKE is low. Data on pin SDI is always sampled on rising edges of SCLK. **ALE: Address Latch Enable** In parallel Intel multiplexed host mode, the address on AD[4:0] is sampled into the device on the falling edges of ALE (signals on AD[7:5] are ignored). In non-multiplexed host mode, ALE should be pulled high. **$\overline{\text{AS}}$: Address Strobe (Active Low)** In parallel Motorola multiplexed host mode, the address on AD[4:0] is latched into the device on the falling edges of $\overline{\text{AS}}$ (signals on AD[7:5] are ignored). In non-multiplexed host mode, $\overline{\text{AS}}$ should be pulled high.
TS1/$\overline{\text{RD}}$/R/$\overline{\text{W}}$	I	85	J13	**TS1: Template Select 1** In hardware control mode, the signal on this pin is the second most significant bit for the transmit template select. Refer to 2.5.1 Waveform Shaper for details. **$\overline{\text{RD}}$: Read Strobe (Active Low)** In parallel Intel multiplexed or non-multiplexed host mode, this pin is active low for read operation. **R/$\overline{\text{W}}$: Read/Write Select** In parallel Motorola multiplexed or non-multiplexed host mode, the pin is active low for write operation and high for read operation.
TS0/SDI/$\overline{\text{WR}}$/ $\overline{\text{DS}}$	I	84	J14	**TS0: Template Select 0** In hardware control mode, the signal on this pin is the least significant bit for the transmit template select. Refer to 2.5.1 Waveform Shaper for details. **SDI: Serial Data Input** In serial host mode, this pin input the data to the serial interface. Data on this pin is sampled on the rising edges of SCLK. **$\overline{\text{WR}}$: Write Strobe (Active Low)** In parallel Intel host mode, this pin is active low during write operation. The data on D[7:0] (in non-multiplexed mode) or AD[7:0] (in multiplexed mode) is sampled into the device on the rising edges of $\overline{\text{WR}}$. **$\overline{\text{DS}}$: Data Strobe (Active Low)** In parallel Motorola host mode, this pin is active low. During a write operation (R/$\overline{\text{W}}$ = 0), the data on D[7:0] (in non-multiplexed mode) or AD[7:0] (in multiplexed mode) is sampled into the device on the rising edges of $\overline{\text{DS}}$. During a read operation (R/$\overline{\text{W}}$ = 1), the data is driven to D[7:0] (in non-multiplexed mode) or AD[7:0] (in multiplexed mode) by the device on the rising edges of $\overline{\text{DS}}$. In parallel Motorola non-multiplexed host mode, the address information on the 5 bits of address bus A[4:0] are latched into the device on the falling edges of $\overline{\text{DS}}$.

Table-1 Pin Description (Continued)

<table>
<tr><th rowspan="2">Name</th><th rowspan="2">Type</th><th colspan="2">Pin No.</th><th rowspan="2">Description</th></tr>
<tr><th>TQFP144</th><th>PBGA160</th></tr>
<tr><td>SDO/RDY/$\overline{ACK}$</td><td>O</td><td>83</td><td>K14</td><td>SDO: Serial Data Output
In serial host mode, the data is output on this pin. In serial write operation, SDO is always in high impedance. In serial read operation, SDO is in high impedance only when SDI is in address/command byte. Data on pin SDO is clocked out of the device on the falling edges of SCLK if pin CLKE is high, or on the rising edges of SCLK if pin CLKE is low.

RDY: Ready Output
In parallel Intel host mode, the high level of this pin reports to the host that bus cycle can be completed, while low reports the host must insert wait states.

$\overline{ACK}$: Acknowledge Output (Active Low)
In parallel Motorola host mode, the low level of this pin indicates that valid information on the data bus is ready for a read operation or acknowledges the acceptance of the written data during a write operation.</td></tr>
<tr><td>$\overline{INT}$</td><td>O
Open
Drain</td><td>82</td><td>K13</td><td>$\overline{INT}$: Interrupt (Active Low)
This is an open drain, active low interrupt output. Two sources may cause the interrupt. Refer to 2.19 Interrupt Handling for details.</td></tr>
<tr><td>D7/AD7
D6/AD6
D5/AD5
D4/AD4
D3/AD3
D2/AD2
D1/AD1
D0/AD0</td><td>I/O

High
Imped-
ance</td><td>28
27
26
25
24
23
22
21</td><td>K1
J1
J2
J3
J4
H2
H3
G2</td><td>Dn: Data Bus 7~0
In non-multiplexed host mode, these pins are the bi-directional data bus.

ADn: Address/Data Bus 7~0
In multiplexed host mode, these pins are the multiplexed bi-directional address/data bus.
In hardware mode, these pins should be tied to VDDIO/2.
In serial host mode, these pins should be grounded.</td></tr>
</table>

Table-1 Pin Description (Continued)

<table>
<tr><th rowspan="2">Name</th><th rowspan="2">Type</th><th colspan="2">Pin No.</th><th rowspan="2">Description</th></tr>
<tr><th>TQFP144</th><th>PBGA160</th></tr>
<tr><td>A4
MC3/A3
MC2/A2
MC1/A1
MC0/A0</td><td>I</td><td>12
13
14
15
16</td><td>F4
F3
F2
F1
G3</td><td>MCn: Performance Monitor Configuration 3~0
In hardware control mode, A4 must be connected to GND. MC[3:0] are used to select a transmitter or receiver of channel 1 to 7 for non-intrusive monitoring. Channel 0 is used as the monitoring channel. If a transmitter is monitored, signals on the corresponding pins TTIPn and TRINGn are internally transmitted to RTIP0 and RRING0 pins. If a receiver is monitored, signals on the corresponding pins RTIPn and RRINGn are internally transmitted to RTIP0 and RRING0 pins. The monitored is then output to RDP0 and RDN0 pins.
Performance Monitor Configuration determined by MC[3:0] is shown below. Note that if MC[2:0] = 000, the device is in normal operation of all the channels.
<table>
<tr><th>MC[3:0]</th><th>Monitoring Configuration</th></tr>
<tr><td>0000</td><td>Normal operation without monitoring</td></tr>
<tr><td>0001</td><td>Monitor Receiver 1</td></tr>
<tr><td>0010</td><td>Monitor Receiver 2</td></tr>
<tr><td>0011</td><td>Monitor Receiver 3</td></tr>
<tr><td>0100</td><td>Monitor Receiver 4</td></tr>
<tr><td>0101</td><td>Monitor Receiver 5</td></tr>
<tr><td>0110</td><td>Monitor Receiver 6</td></tr>
<tr><td>0111</td><td>Monitor Receiver 7</td></tr>
<tr><td>1000</td><td>Normal operation without monitoring</td></tr>
<tr><td>1001</td><td>Monitor Transmitter 1</td></tr>
<tr><td>1010</td><td>Monitor Transmitter 2</td></tr>
<tr><td>1011</td><td>Monitor Transmitter 3</td></tr>
<tr><td>1100</td><td>Monitor Transmitter 4</td></tr>
<tr><td>1101</td><td>Monitor Transmitter 5</td></tr>
<tr><td>1110</td><td>Monitor Transmitter 6</td></tr>
<tr><td>1111</td><td>Monitor Transmitter 7</td></tr>
</table>
In host mode operation, the monitoring channel is selected in the PMON register. The signals monitored by channel 0 can be routed to TTIP0/RING0 by activating the remote loopback in this channel (refer to 2.13 G.772 Monitoring).

An: Address Bus 4~0
When pin MODE1 is low, the parallel host interface operates with separate address and data bus. In this mode, the signal on this pin is the address bus of the host interface.
When pin MODE1 is high or in serial host mode, these pins should be tied to GND.</td></tr>
<tr><td>OE</td><td>I</td><td>114</td><td>E14</td><td>OE: Output Driver Enable
Pulling this pin low can drive all driver output into high impedance for redundancy application without external mechanical relays. In this condition, all other internal circuits remain active.</td></tr>
<tr><td>CLKE</td><td>I</td><td>115</td><td>E13</td><td>CLKE: Clock Edge Select
The signal on this pin determines the active edge of RCn, RDPn, RDNn and SCLK. Refer to 2.3 Clock Edges for details.</td></tr>
<tr><td colspan="5">JTAG Signals</td></tr>
<tr><td>$\overline{\text{TRST}}$</td><td>I
Pull-up</td><td>95</td><td>G12</td><td>$\overline{\text{TRST}}$: JTAG Test Port Reset (Active Low)
This is the active low asynchronous reset to the JTAG Test Port. This pin has an internal pull-up resistor and can be left disconnected.</td></tr>
<tr><td>TMS</td><td>I
Pull-up</td><td>96</td><td>F11</td><td>TMS: JTAG Test Mode Select
The signal on this pin controls the JTAG test performance and is clocked into the device on the rising edges of TCK. This pin has an internal pull-up resistor and can be left disconnected.</td></tr>
<tr><td>TCK</td><td>I</td><td>97</td><td>F14</td><td>TCK: JTAG Test Clock
The clock of the JTAG test is input on this pin. The data on TDI and TMS are clocked into the device on rising edges of TCK while the data on TDO pin is clocked out of the device on falling edges of TCK. This pin should be connected to GNDIO or VDDIO pin when unused.</td></tr>
</table>

Table-1 Pin Description (Continued)

Name	Type	Pin No.		Description
		TQFP144	PBGA160	
TDO	O High Imped-ance	98	F13	**TDO: JTAG Test Data Output** The serial data of the JTAG test is output on this pin. The data on TDO pin is clocked out of the device on the falling edges of TCK. TDO is a high impedance output signal. It is active only when scanning of data is over. This pin should be left float when unused.
TDI	I Pull-up	99	F12	**TDI: JTAG Test Data Input** The serial data of the JTAG test is input on this pin. The data on TDI pin is clocked into the device on the rising edges of TCK. This pin has an internal pull-up resistor and it can be left disconnected.
Power Supplies and Grounds				
VDDIO	-	17 92	G1 G14	**3.3 V I/O Power Supply**
GNDIO	-	18 91	G4 G11	**I/O GND**
VDDT0 VDDT1 VDDT2 VDDT3 VDDT4 VDDT5 VDDT6 VDDT7	-	44 53 56 65 116 125 128 137	N4, P4 L4, M4 L11, M11 N11, P11 A11, B11 C11, D11 C4, D4 A4, B4	**3.3 V/5 V Power Supply for Transmitter Driver** All VDDT pins must be connected to 3.3 V or all VDDT must be connected to 5 V. It is not allowed to leave any of the VDDT pins open (not-connected) even if the channel is not used. T1 is only 5V VDDT.
GNDT0 GNDT1 GNDT2 GNDT3 GNDT4 GNDT5 GNDT6 GNDT7	-	47 50 59 62 119 122 131 134	N6, P6 L6, M6 L9, M9 N9, P9 A9, B9 C9, D9 C6, D6 A6, B6	**Analog GND for Transmitter Driver**
VDDD VDDA	-	19 90	H1 H14	**3.3 V Digital/Analog Core Power Supply**
GNDD GNDA	-	20 89	H4 H11	**Digital/Analog Core GND**
Others				
IC	-	93	G13	**IC: Internal Connection** Internal use. Leave it open for normal operation.
IC	-	94	H13	**IC: Internal Connection** Internal use. Leave it open for normal operation.

2 FUNCTIONAL DESCRIPTION

2.1 OVERVIEW

The IDT82V2048L is a fully integrated octal short-haul analog front end (AFE), which contains eight transmit and receive channels for use in either T1 or E1 applications. The raw sliced data (no retiming) is output to the system. Transmit equalization is implemented with low-impedance output drivers that provide shaped waveforms to the transformer, guaranteeing template conformance. Moreover, testing functions, such as JTAG boundary scan is provided. The device is optimized for flexible software control through a serial or parallel host mode interface. Hardware control is also available. Figure-1 on page 1 shows one of the eight identical channels operation.

2.2 T1/E1 MODE SELECTION

T1/E1 mode selection configures the device globally. In Hardware control Mode, the template selection pins TS[2:0], determine whether the operation mode is T1 or E1 (see Table-5 on page 14). In Software Mode, the register **TS** determines whether the operation mode is T1 or E1.

2.2.1 SYSTEM INTERFACE

The system interface of each channel operates in Dual Rail Mode with data recovery, that is, with raw data slicing only and without clock recovery.

The Dual Rail interface consist of TDPn[1], TDNn, TCLKn, RDPn, RDNn and RCn. Data transmitted from TDPn and TDNn appears on TTIPn and TRINGn at the line interface. The interface of the AFE is shown in Figure-4. Pin RDPn and RDNn, are raw RZ slice outputs and internally connected to an XOR which is fed to the RCn output for external clock recovery applications.

2.2.1.1 SYSTEM INTERFACE CONFIGURATION

For normal transmit and receive operation, the device is configured as follows:

In host mode, MCLK can be either clocked or pulled high. If MCLK is pulled high, TCLK1 has to be provided for proper device operation. In addition, register **e-AFE**[2] has to be set to 'FFH' to ensure proper device operation. See Expanded Register Description on page 28 for details.

In hardware mode, MCLK has to be pulled high and TCLK1 has to be provided for proper device operation.

Depending on the state of TCLK1 and TCLKn, the transmitter will Transmit All Ones (TAOS), will go into power down, or will go into high impedance.

The status of TCLK1 and TCLKn has no effect on the receive paths. By setting MCLK low, all the receive paths are powered down.

Table-2 summarizes the different combinations between MCLK and TCLKn.

1. The footprint 'n' (n = 0 - 7) indicates one of the eight channels.
2. The first letter 'e-' indicates expanded register.

Table-2 System Interface Configuration

Host or Hardware Mode	MCLK	TCLK1	TCLKn	AFEn in e-AFE	Transmitter Mode
Transmit and Receive Normal Operation					
Host[1] only	Clocked	Clocked	Clocked	1	Normal operation
Host or Hardware[2]	High	Clocked	Clocked	DC[3]	Normal operation
Transmit Interface Modes					
Host only	Clocked	High (≥ 16 MCLK)		1	Transmit All Ones (TAOS) signals to the line side in the corresponding transmit channel.
		Low (≥ 64 MCLK)			Corresponding transmit channel is set into power down state.
Host or Hardware	High/Low	TCLK1 is clocked	TCLKn is high (≥ 16 TCLK1)	DC	Transmit All Ones (TAOS) signals to the line side in the corresponding transmit channel.
			TCLKn is low (≥ 64 TCLK1)		Corresponding transmit channel is set into power down state.
		TCLK1 is unavailable.	DC		All eight transmitters (TTIPn & TRINGn) are in high impedance.
Receive Interface Modes					
Host or Hardware	Low	The receive path is not affected by the status of TCLK1 or TCLKn.		DC	All the receive paths are powered down.

1. In host mode, register **e-AFE** must be set to 'FFH' for proper operation. See Expanded Register Description on page 28 for details.

2. In hardware mode, MCLK must be pulled high and TCLK1 provided for proper operation.

3. DC means Don't Care

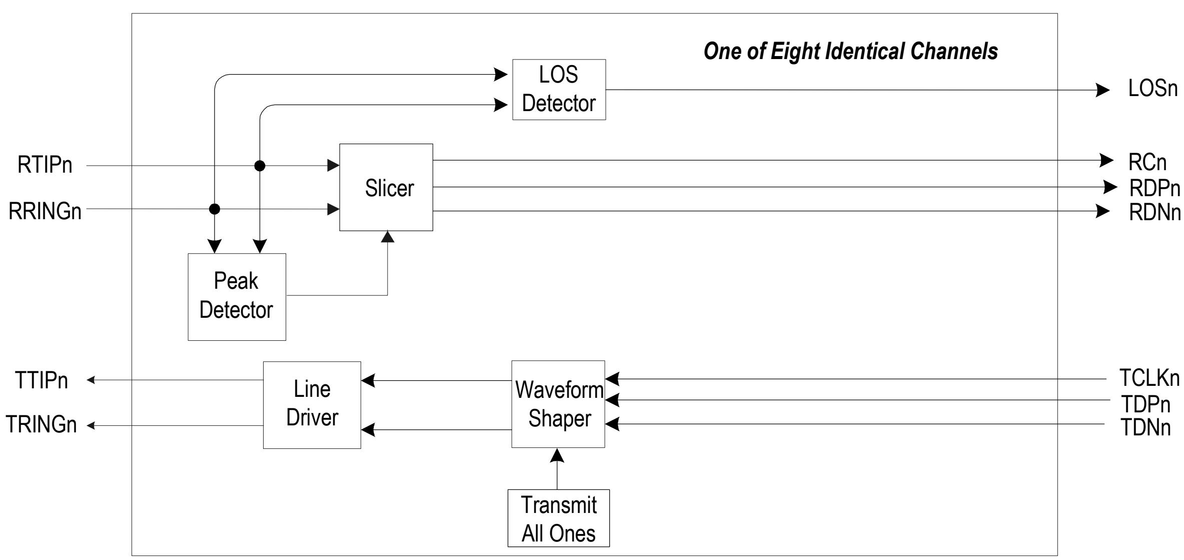
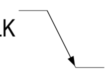
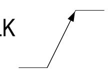


Figure-4 Analog Front End (AFE) Interface

2.3 CLOCK EDGES

The active edge of SCLK is selectable. If pin CLKE is high, the active edge of SCLK is the falling edge. On the contrary, if CLKE is low, the active edge SCLK is the rising edge. Pin SDO is always active high, and the output signals are valid on the active edge of SCLK. See Table-3 Active Clock Edge and Active Level for details. Pin CLKE is used to set the active level for RDPn/RDNn raw slicing output: high for active high polarity and low for active low. It should be noted that data on pin SDI are always active high and are sampled on the rising edges of SCLK. The data on pin TDPn or TDNn are also always active high but are sampled on the falling edges of TCLKn, despite the level on CLKE.

Table-3 Active Clock Edge and Active Level

Pin CLKE	Pin RDPn and RDNn Slicer Output	Pin SDO	
High	Active High	SCLK 	Active High
Low	Active Low	SCLK 	Active High

2.4 RECEIVER

In receive path, the line signals couple into RRINGn and RTIPn via a transformer and are converted into RZ digital pulses by a data slicer. Adaptation for attenuation is achieved using an integral peak detector that sets the slicing levels. The recovered data on pin RDPn/RDNn in an undecoded dual rail RZ format. Loss of signal is detected. This change in status may be enabled to generate an interrupt.

2.4.1 PEAK DETECTOR AND SLICER

The slicer determines the presence and polarity of the received pulses. The raw positive slicer output appears on RDPn while the negative slicer output appears on RDNn. The slicer circuit has a built-in peak detector from which the slicing threshold is derived. The slicing threshold is default to 50% (typical) of the peak value.

Signals with an attenuation of up to 12 dB (from 2.4 V) can be recovered by the receiver. To provide immunity from impulsive noise, the peak detectors are held above a minimum level of 0.150 V typically, despite the received signal level.

2.4.2 DATA RECOVERY

The analog line signal are converted to RZ digital bit streams on the RDPn/RDNn pins and internally connected to an XOR which is fed to the RCn output for external clock recovery applications.

2.4.3 LOSS OF SIGNAL (LOS) DETECTION

The Loss of Signal Detector monitors the amplitude and density of the received signal on receiver line before the transformer (measured on port A, B shown in Figure-7). The loss condition is reported by pulling pin LOSn high. At the same time, LOS alarm registers track LOS condition. When LOS is detected or cleared, an interrupt will generate if not masked. In host mode, the detection supports the ANSI T1.231 for T1 mode, ITU G.775 and ETSI 300 233 for E1 mode. In hardware mode, it supports the ITU G.775 and ANSI T1.231.

Table-4 summarizes the conditions of LOS. During LOS, the RDPn/RDNn continue to output the sliced data.

Table-4 LOS Condition

		Standard			Signal on LOSn
		ANSI T1.231 for T1	G.775 for E1	ETSI 300 233 for E1	
LOS Detected	Continuous Intervals	175	32	2048 (1 ms)	High
	Amplitude[1]	below typical 200 mVp	below typical 200 mVp	below typical 200 mVp	
LOS Cleared	Density	12.5% (16 marks in a sliding 128-bit period) with no more than 99 continuous zeros	12.5% (4 marks in a sliding 32-bit period) with no more than 15 continuous zeros	12.5% (4 marks in a sliding 32-bit period) with no more than 15 continuous zeros	Low
	Amplitude[1]	exceed typical 250 mVp	exceed typical 250 mVp	exceed typical 250 mVp	

1. LOS levels at device (RTIPn, RRINGn) with all ones signal. For more detail regarding the LOS parameters, please refer to Receiver Characteristics on page 38.

2.5 TRANSMITTER

In transmit path, data in NRZ format is clocked into the device on TDPn and TDNn. The data is sampled into the device on falling edges of TCLKn. The shape of the pulses are user programmable to ensure that the T1/E1 pulse template is met after the signal passes through different cable lengths or types.

2.5.1 WAVEFORM SHAPER

T1 pulse template, specified in the DSX-1 Cross-Connect by ANSI T1.102, is illustrated in Figure-5. The device has built-in transmit waveform templates, corresponding to 5 levels of pre-equalization for cable of a length from 0 to 655 ft with each increment of 133 ft.

E1 pulse template, specified in ITU-T G.703, is shown in Figure-6. The device has built-in transmit waveform templates for cable of 75 Ω or 120 Ω.

Any one of the six built-in waveforms can be chosen in both hardware mode and host mode. In hardware control mode, setting pins TS[2:0] can select the required waveform template for all the transmitters, as shown in Table-5. In host mode, the waveform template can be configured on a per-channel basis. Bits TSIA[2:0] in register **TSIA** are used to select the channel and bits TS[2:0] in register **TS** are used to select the required waveform template.

The built-in waveform shaper uses an internal high frequency clock which is 16XMCLK as the clock reference. This function will be bypassed when MCLK is unavailable.

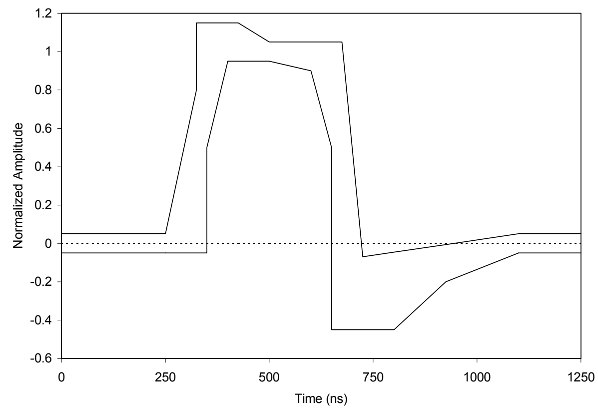


Figure-5 DSX-1 Waveform Template

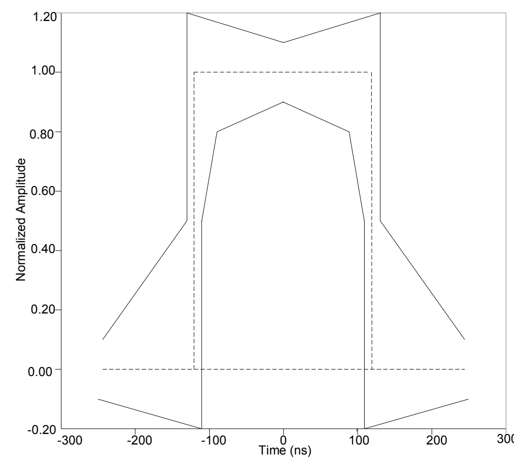


Figure-6 CEPT Waveform Template

Table-5 Built-in Waveform Template Selection

TS2	TS1	TS0	Service	Clock Rate	Cable Length	Maximum Cable Loss (dB)[1]
0	0	0	E1	2.048 MHz	120 Ω/75 Ω Cable	-
						-
0	0	1	Reserved			
0	1	0				
0	1	1	T1	1.544 MHz	0-133 ft. ABAM	0.6
1	0	0			133-266 ft. ABAM	1.2
1	0	1			266-399 ft. ABAM	1.8
1	1	0			399-533 ft. ABAM	2.4
1	1	1			533-655 ft. ABAM	3.0

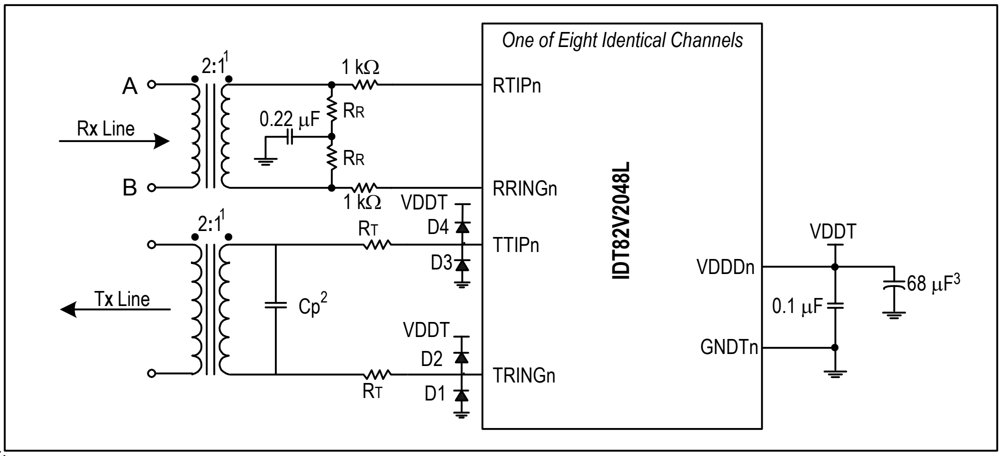
1. Maximum cable loss at 772 kHz.

2.6 LINE INTERFACE CIRCUITRY

The transmit and receive interface RTIPn/RRINGn and TTIPn/TRINGn connections provide a matched interface to the cable. Figure-7 shows the appropriate external components to connect with the cable for one transmit/receive channel. Table-6 summarizes the component values based on the specific application.

Table-6 External Components Values

Component	E1		T1
	75 Ω Coax	**120 Ω Twisted Pair**	**100 Ω Twisted Pair, VDDT = 5.0 V**
R_T	9.5 Ω ± 1%	9.5 Ω ± 1%	9.1 Ω ± 1%
R_R	9.31 Ω ± 1%	15 Ω ± 1%	12.4 Ω ± 1%
Cp	2200 pF		1000 pF
D1 - D4	Nihon Inter Electronics - EP05Q03L, 11EQS03L, EC10QS04, EC10QS03L; Motorola - MBR0540T1		



NOTE:
1. Pulse T1124 transformer is recommended to be used in Standard (STD) operating temperature range (0°C to 70°C), while Pulse T1114 transformer is recommended to be used in Extended (EXT) operating temperature range is -40°C to +85°C. See Transformer Specifications Table for details.
2. Typical value. Adjust for actual board parasitics to obtain optimum return loss.
3. Common decoupling capacitor for all VDDT and GNDT pins. One per chip.

Figure-7 External Transmit/Receive Line Circuitry

2.7 TRANSMIT DRIVER POWER SUPPLY

All transmit driver power supplies must be 5.0 V or 3.3 V.

In E1 mode, despite the power supply voltage, the 75 Ω/120 Ω lines are driven through a pair of 9.5 Ω series resistors and a 1:2 transformer.

In T1 mode, only 5.0 V can be selected, 100 Ω lines are driven through a pair of 9.1 Ω series resistors and a 1:2 transformer.

In harsh cable environment, series resistors are required to improve the transmit return loss performance and protect the device from surges coupling into the device.

Table-7 Transformer Specifications(1)

Electrical Specification @ 25°C										
Part No.		Turns Ratio (Pri: sec ± 2%)		OCL @ 25°C (mH MIN)		L_L (µH MAX)		$C_{W/W}$ (pF MAX)		Package/Schematic
STD Temp.	EXT Temp.	Transmit	Receive	Transmit	Receive	Transmit	Receive	Transmit	Receive	
T1124	T1114	1:2CT	1CT:2	1.2	1.2	.6	.6	35	35	TOU/3

1. Pulse T1124 transformer is recommended to be used in Standard (STD) operating temperature range (0°C to 70°C), while Pulse T1114 transformer is recommended to be used in Extended (EXT) operating temperature range is -40°C to +85°C.

2.8 POWER DRIVER FAILURE MONITOR

An internal power Driver Failure Monitor (DFMON), parallel connected with TTIPn and TRINGn, can detect short circuit failure between TTIPn and TRINGn pins. Bit SCPB in register **GCF** decides whether the output driver short circuit protection is enabled. When the short circuit protection is enabled, the driver output current is limited to a typical value: 180 mAp. Also, register **DF**, **DFI** and **DFM** will be available. When DFMON will detect a short circuit, register **DF** will be set. With a short circuit failure detected, register **DFI** will be set and an interrupt will be generated on pin $\overline{\text{INT}}$.

2.9 TRANSMIT LINE SIDE SHORT CIRCUIT

In E1 or T1 with 5 V VDDT, a pair of 9.5 Ω serial resistors connect with TTIPn and TRINGn pins and limit the output current. In this case, the output current is a limited value which is always lower than the typical line short circuit current 180 mAp, even if the transmit line side is shorted.

Refer to Table-6 External Components Values for details.

2.10 LINE PROTECTION

In transmit side, the Schottky diodes D1~D4 are required to protect the line driver and improve the design robustness. In receive side, the series resistors of 1 kΩ are used to protect the receiver against current surges coupled in the device. The series resistors do not affect the receiver sensitivity, since the receiver impedance is as high as 120 kΩ typically.

2.11 HITLESS PROTECTION SWITCHING (HPS)

The IDT82V2048L transceivers include an output driver with high impedance feature for T1/E1 redundancy applications. This feature reduces the cost of redundancy protection by eliminating external relays. Details of HPS are described in relative Application Note.

2.12 TRANSMIT ALL ONES (TAOS)

In hardware mode, the TAOS mode is set by pulling pin TCLKn high for more than 16 MCLK cycles. In host mode, TAOS mode is set by programming register **TAO**. In addition, automatic TAOS signals are inserted by setting register **ATAO** when Loss of Signal occurs. Note that the TAOS generator adopts MCLK as a timing reference. In order to assure that the output frequency is within specified limits, MCLK must have the applicable stability.

Refer to Figure-8 TAOS Data Path.

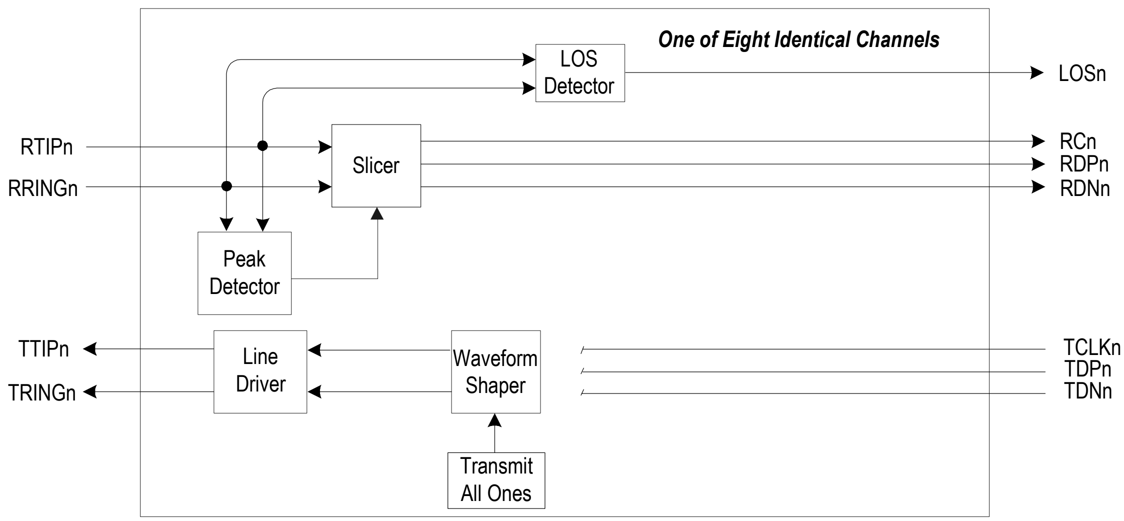


Figure-8 TAOS Data Path

2.13 G.772 MONITORING

The eight channels of IDT82V2048L can all be configured to work as regular transceivers. In applications using only seven channels (channels 1 to 7), channel 0 is configured to non-intrusively monitor any of the other channels' inputs or outputs on the line side. The monitoring is non-intrusive per ITU-T G.772. Figure-9 shows the Monitoring Principle. The receiver path or transmitter path to be monitored is configured by pin MC[3:0] in hardware mode or by **PMON** in host mode.

The signal which is monitored can be observed digitally at the output pin RC0, RDP0 and RDN0. LOS detector is still in use in channel 0 for the monitored signal.

In monitoring mode, a clock and data recovery circuit can be enabled for Remote Loopback operation. In Remote Loopback operation, the signal which is being monitored will be also output on TTIP0 and TRING0 pins. The output signal can then be connected to a standard test equipment for non-intrusive monitoring. RC0 pin will also output the recovered clock (DPLL).

The remote loopback is only available in host mode operation.

To enable the remote loopback, bit 0 in register **RL0** has to be set, and bit 0 in register **e-AFE** has to be cleared. The register setting are: register **RL0** set '01'H, register **e-AFE** set 'FE'H.

For normal operation register **RL0** has to be set '00H' and register **e-AFE** has to be set 'FFH'.

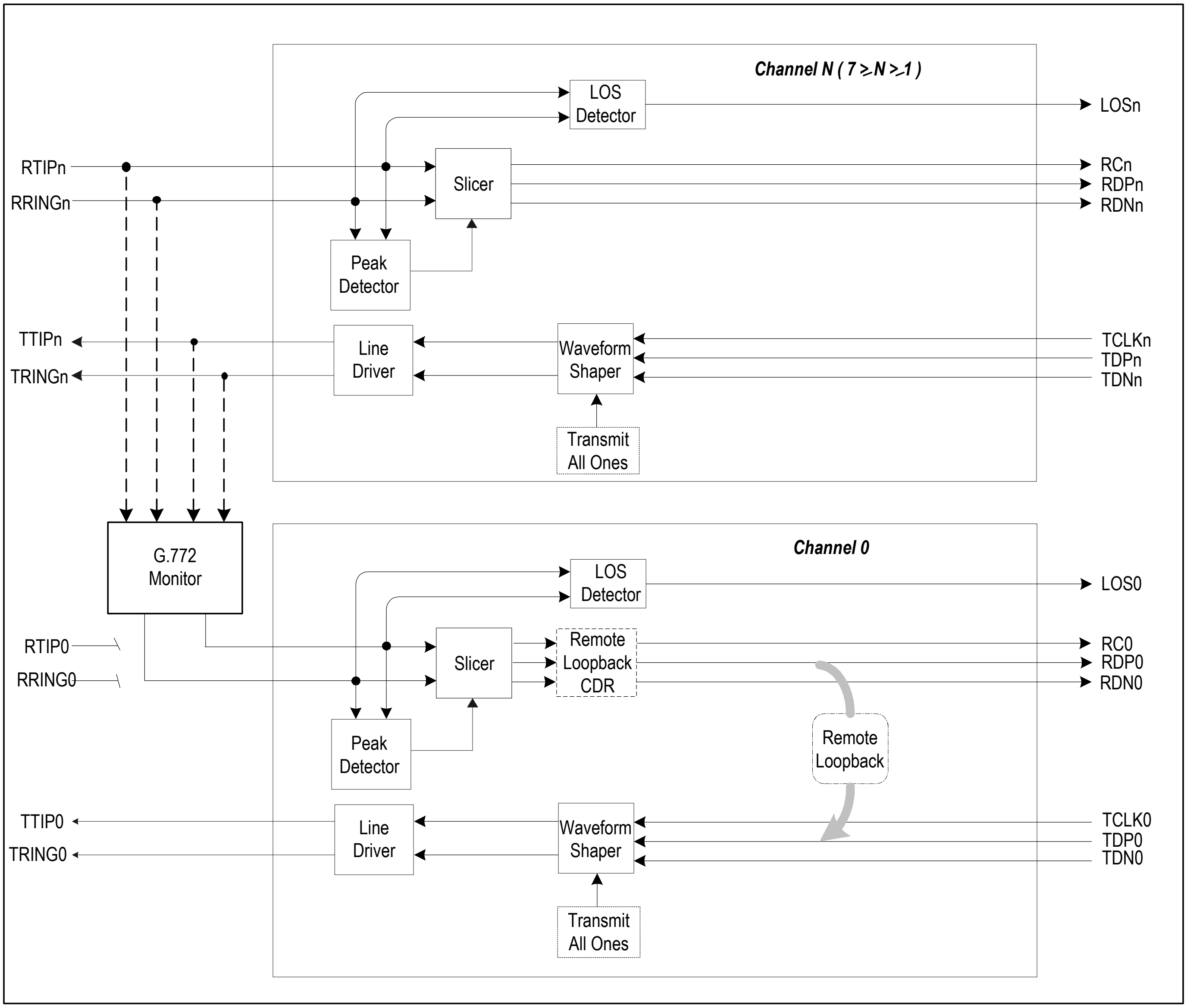


Figure-9 Monitoring Principle

2.14 SOFTWARE RESET

Writing register **RS** will cause software reset by initiating about 1 µs reset cycle. This operation set all the registers to their default value.

2.15 POWER ON RESET

During power up, an internal reset signal sets all the registers to default values. The power-on reset takes at least 10 µs, starting from when the power supply exceeds 2/3 VDDA.

2.16 POWER DOWN

Each transmit channel will be powered down by pulling pin TCLKn low for more than 64 MCLK cycles (if MCLK is available) or about 30 µs (if MCLK is not available). In host mode, each transmit channel will also be powered down by setting bit TPDNn in register **e-TPDN** to '1'.

All the receivers will be powered down when MCLK is low. When MCLK is clocked or high, setting bit RPDNn in register **e-RPDN** to '1' will configure the corresponding receiver to be powered down.

2.17 INTERFACE WITH 5 V LOGIC

The IDT82V2048L can interface directly with 5 V TTL family devices. The internal input pads are tolerant to 5 V output from TTL and CMOS family devices.

2.18 HOST INTERFACE

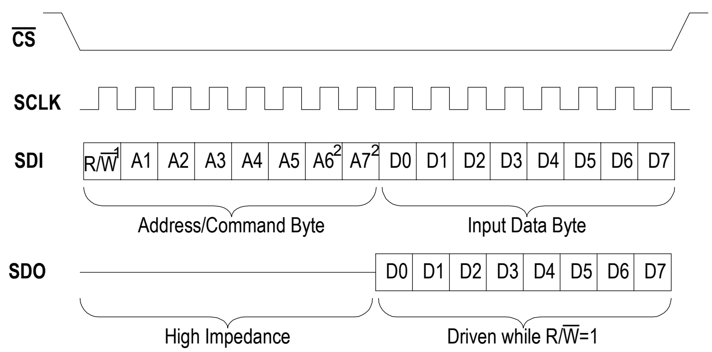
The host interface provides access to read and write the registers in the device. The interface consists of serial host interface and parallel host interface. By pulling pin MODE2 to VDDIO/2 or high, the device can be set to work in serial mode and in parallel mode respectively. In host mode operation, expanded register **e-FAE** has to be set to 'FFH' for proper device operation. See Expanded Register Description on page 28 for details.

2.18.1 PARALLEL HOST INTERFACE

The interface is compatible with Motorola and Intel host. Pins MODE[1:0] are used to select the operating mode of the parallel host interface. When pin MODE1 is pulled low, the host uses separate address bus and data bus. When high, multiplexed address/data bus is used. When pin MODE0 is pulled low, the parallel host interface is configured for Motorola compatible hosts. When pin MODE0 is pulled high, the parallel host interface is configured for Intel compatible hosts. See Table-1 Pin Description for more details. The host interface pins in each operation mode is tabulated in Table-8:

Table-8 Parallel Host Interface Pins

MODE[2:0]	Host Interface	Generic Control, Data and Output Pin
100	Non-multiplexed Motorola interface	$\overline{CS}$, $\overline{ACK}$, $\overline{DS}$, R/$\overline{W}$, $\overline{AS}$, A[4:0], D[7:0], $\overline{INT}$
101	Non-multiplexed Intel interface	$\overline{CS}$, RDY, $\overline{WR}$, $\overline{RD}$, ALE, A[4:0], D[7:0], $\overline{INT}$
110	Multiplexed Motorola interface	$\overline{CS}$, $\overline{ACK}$, $\overline{DS}$, R/$\overline{W}$, $\overline{AS}$, AD[7:0], $\overline{INT}$
111	Multiplexed Intel interface	$\overline{CS}$, RDY, $\overline{WR}$, $\overline{RD}$, ALE, AD[7:0], $\overline{INT}$



1. While R/$\overline{W}$=1, read from IDT82V2048L; While R/$\overline{W}$=0, write to IDT82V2048L.
2. Ignored.

Figure-10 Serial Host Mode Timing

2.18.2 SERIAL HOST INTERFACE

By pulling pin MODE2 to VDDIO/2, the device operates in the serial host Mode. In this mode, the registers are accessible through a 16-bit word which contains an 8-bit command/address byte (bit R/$\overline{W}$ and 5-address-bit A1~A5, A6 and A7 bits are ignored) and a subsequent 8-bit data byte (D7~D0), as shown in Figure-10. When bit R/$\overline{W}$ is set to '1', data is read out from pin SDO. When bit R/$\overline{W}$ is set to '0', data on pin SDI is written into the register whose address is indicated by address bits A5~A1. Refer to Figure-10 Serial Host Mode Timing.

2.19 INTERRUPT HANDLING

2.19.1 INTERRUPT SOURCES

There are two kinds of interrupt sources:

1. *Status change in register **LOS**. The analog/digital loss of signal detector continuously monitors the received signal to update the specific bit in register **LOS** which indicates presence or absence of a LOS condition.*
2. *Status change in register **DF**. The automatic power driver circuit continuously monitors the output drivers signal to update the specific bit in register **DFM** which indicates presence or absence of an output driver short circuit condition.*

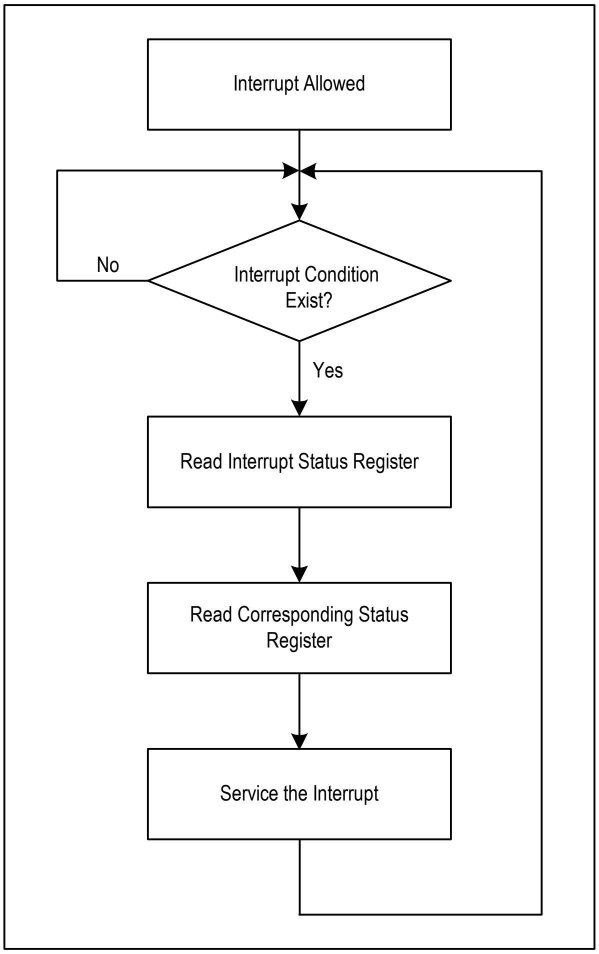


Figure-11 Interrupt Service Routine

2.19.2 INTERRUPT ENABLE

The IDT82V2048L provides a latched interrupt output ($\overline{\text{INT}}$) and the two kinds of interrupts are all reported by this pin. When the Interrupt Mask register: **LOSM** and **DFM**, are set to '1', the Interrupt Status register: **LOSI** and **DFI**, are enabled respectively. Whenever there is a transition ('0' to '1' or '1' to '0') in the corresponding status register, the Interrupt Status register will change into '1', which means an interrupt occurs, and there will be a high to low transition on $\overline{\text{INT}}$ pin. An external pull-up resistor of approximately 10 kΩ is required to support the wire-OR operation of $\overline{\text{INT}}$. When any of the two Interrupt Mask registers is set to '0' (the power-on default value is '0'), the corresponding Interrupt Status register is disabled and the transition on status register is ignored.

2.19.3 INTERRUPT CLEARING

When an interrupt occurs, the Interrupt Status registers: **LOSI** and **DFI**, are read to identify the interrupt source. These registers will be cleared to '0' after the corresponding status registers: **LOS** and **DF** are read. The Status registers will be cleared once the corresponding conditions are met.

Pin $\overline{\text{INT}}$ is pulled high when there is no pending interrupt left. The interrupt handling in the interrupt service routine is shown in Figure-11.

3 PROGRAMMING INFORMATION

3.1 REGISTER LIST AND MAP

There are 18 primary registers (including an Address Pointer Control Register and 4 expanded registers in the device).

Whatever the control interface is, 5 address bits are used to set the registers. In non-multiplexed parallel interface mode, the five dedicated address bits are A[4:0]. In multiplexed parallel interface mode, AD[4:0] carries the address information. In serial interface mode, A[5:1] are used to address the register.

The Register **ADDP**, addressed as 11111 or 1F Hex, switches between primary registers bank and expanded registers bank.

By setting register **ADDP** to ‘AAH’, the 5 address bits point to the expanded register bank, that is, 4 expanded registers are available. By clearing register **ADDP**, the primary registers are available.

3.2 RESERVED AND TEST REGISTERS

Primary Registers, whose address are 01H, 0CH, 13H to 1EH, are reserved. Expanded registers, whose address are 00H, 01H, 05H, 06H, 08H to 0FH, are reserved. Expanded registers, whose address are 10H to 1EH, are used for test and must be set to ‘0’ (default).

Table-9 Primary Register List

Address			Register	R/W	Explanation
Hex	Serial Interface A7-A1	Parallel Interface A7-A0			
00	XX00000	XXX00000	ID	R	Device ID Register
01	XX00001	XXX00001	Reserved		
02	XX00010	XXX00010	RL0	R/W	G.772 Monitoring, Remote Loopback Configuration Register
03	XX00011	XXX00011	TAO	R/W	Transmit All Ones Configuration Register
04	XX00100	XXX00100	LOS	R	Loss of Signal Status Register
05	XX00101	XXX00101	DF	R	Driver Fault Status Register
06	XX00110	XXX00110	LOSM	R/W	LOS Interrupt Mask Register
07	XX00111	XXX00111	DFM	R/W	Driver Fault Interrupt Mask Register
08	XX01000	XXX01000	LOSI	R	LOS Interrupt Status Register
09	XX01001	XXX01001	DFI	R	Driver Fault Interrupt Status Register
0A	XX01010	XXX01010	RS	W	Software Reset Register
0B	XX01011	XXX01011	PMON	R/W	Performance Monitor Configuration Register
0C	XX01100	XXX01100	Reserved		
0D	XX01101	XXX01101	LAC	R/W	LOS/AIS Criteria Configuration Register
0E	XX01110	XXX01110	ATAO	R/W	Automatic TAOS Configuration Register
0F	XX01111	XXX01111	GCF	R/W	Global Configuration Register
10	XX10000	XXX10000	TSIA	R/W	Indirect Address Register for Transmit Template Select
11	XX10001	XXX10001	TS	R/W	Transmit Template Select Register
12	XX10010	XXX10010	OE	R/W	Output Enable Configuration Register
13	XX10011	XXX10011	Reserved		
14	XX10100	XXX10100			
15	XX10101	XXX10101			
16	XX10110	XXX10110			
17	XX10111	XXX10111			
18	XX11000	XXX11000			
19	XX11001	XXX11001			
1A	XX11010	XXX11010			
1B	XX11011	XXX11011			
1C	XX11100	XXX11100			
1D	XX11101	XXX11101			
1E	XX11110	XXX11110			
1F	XX11111	XXX11111	ADDP	R/W	Address pointer control Register for switching between primary register bank and expanded register bank

Table-10 Expanded (Indirect Address Mode) Register List

Address			Register	R/W	Explanation
Hex	Serial Interface A7-A1	Parallel Interface A7-A0			
00	XX00000	XXX00000	Reserved		
01	XX00001	XXX00001			
02	XX00010	XXX00010	e-AFE	R/W	AFE Enable Register
03	XX00011	XXX00011	e-RPDN	R/W	Receiver n Powerdown Enable/Disable Register
04	XX00100	XXX00100	e-TPDN	R/W	Transmitter n Powerdown Enable/Disable Register
05	XX00101	XXX00101	Reserved		
06	XX00110	XXX00110			
07	XX00111	XXX00111	e-EQUA	R/W	Enable Equalizer Enable/Disable Register
08	XX01000	XXX01000	Reserved		
09	XX01001	XXX01001			
0A	XX01010	XXX01010			
0B	XX01011	XXX01011			
0C	XX01100	XXX01100			
0D	XX01101	XXX01101			
0E	XX01110	XXX01110			
0F	XX01111	XXX01111			
10	XX10000	XXX10000	Test		
11	XX10001	XXX10001			
12	XX10010	XXX10010			
13	XX10011	XXX10011			
14	XX10100	XXX10100			
15	XX10101	XXX10101			
16	XX10110	XXX10110			
17	XX10111	XXX10111			
18	XX11000	XXX11000			
19	XX11001	XXX11001			
1A	XX11010	XXX11010			
1B	XX11011	XXX11011			
1C	XX11100	XXX11100			
1D	XX11101	XXX11101			
1E	XX11110	XXX11110			
1F	XX11111	XXX11111	ADDP	R/W	Address pointer control register for switching between primary register bank and expanded register bank

Table-11 Primary Register Map

Register	Address R/W Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ID	00H R Default	ID 7 R 0	ID 6 R 0	ID 5 R 0	ID 4 R 1	ID 3 R 0	ID 2 R 0	ID 1 R 0	ID 0 R 0
RL0	02H R/W Default	- R/W 0	- R/W 0	- R/W 0	- R/W 0	- R/W 0	- R/W 0	- R/W 0	RL0 R/W 0
TAO	03H R/W Default	TAO 7 R/W 0	TAO 6 R/W 0	TAO 5 R/W 0	TAO 4 R/W 0	TAO 3 R/W 0	TAO 2 R/W 0	TAO 1 R/W 0	TAO 0 R/W 0
LOS	04H R Default	LOS 7 R 0	LOS 6 R 0	LOS 5 R 0	LOS 4 R 0	LOS 3 R 0	LOS 2 R 0	LOS 1 R 0	LOS 0 R 0
DF	05H R Default	DF 7 R 0	DF 6 R 0	DF 5 R 0	DF 4 R 0	DF 3 R 0	DF 2 R 0	DF 1 R 0	DF 0 R 0
LOSM	06H R/W Default	LOSM 7 R/W 0	LOSM 6 R/W 0	LOSM 5 R/W 0	LOSM 4 R/W 0	LOSM 3 R/W 0	LOSM 2 R/W 0	LOSM 1 R/W 0	LOSM 0 R/W 0
DFM	07H R/W Default	DFM 7 R/W 0	DFM 6 R/W 0	DFM 5 R/W 0	DFM 4 R/W 0	DFM 3 R/W 0	DFM 2 R/W 0	DFM 1 R/W 0	DFM 0 R/W 0
LOSI	08H R Default	LOSI 7 R 0	LOSI 6 R 0	LOSI 5 R 0	LOSI 4 R 0	LOSI 3 R 0	LOSI 2 R 0	LOSI 1 R 0	LOSI 0 R 0
DFI	09H R Default	DFI 7 R 0	DFI 6 R 0	DFI 5 R 0	DFI 4 R 0	DFI 3 R 0	DFI 2 R 0	DFI 1 R 0	DFI 0 R 0
RS	0AH W Default	RS 7 W 1	RS 6 W 1	RS 5 W 1	RS 4 W 1	RS 3 W 1	RS 2 W 1	RS 1 W 1	RS 0 W 1
PMON	0BH R/W Default	- R/W 0	- R/W 0	- R/W 0	- R/W 0	MC 3 R/W 0	MC 2 R/W 0	MC 1 R/W 0	MC 0 R/W 0
LAC	0DH R/W Default	LAC 7 R/W 0	LAC 6 R/W 0	LAC 5 R/W 0	LAC 4 R/W 0	LAC 3 R/W 0	LAC 2 R/W 0	LAC 1 R/W 0	LAC 0 R/W 0
ATAO	0EH R/W Default	ATAO 7 R/W 0	ATAO 6 R/W 0	ATAO 5 R/W 0	ATAO 4 R/W 0	ATAO 3 R/W 0	ATAO 2 R/W 0	ATAO 1 R/W 0	ATAO 0 R/W 0
GCF	0FH R/W Default	- R/W 0	- R/W 0	SCPB R/W 0	- R/W 0	- R/W 0	- R/W 0	- R/W 0	- R/W 0
TSIA	10 Hex R/W Default	- R/W 0	- R/W 0	- R/W 0	- R/W 0	- R/W 0	TSIA 2 R/W 0	TSIA 1 R/W 0	TSIA 0 R/W 0

Table-11 Primary Register Map (Continued)

Register	Address R/W Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TS	11 Hex R/W Default	- R/W 0	- R/W 0	- R/W 0	- R/W 0	- R/W 0	TS 2 R/W 0	TS 1 R/W 0	TS 0 R/W 0
OE	12 Hex R/W Default	OE 7 R/W 0	OE 6 R/W 0	OE 5 R/W 0	OE 4 R/W 0	OE 3 R/W 0	OE 2 R/W 0	OE 1 R/W 0	OE 0 R/W 0
ADDP	1F Hex R/W Default	ADDP 7 R/W 0	ADDP 6 R/W 0	ADDP 5 R/W 0	ADDP 4 R/W 0	ADDP 3 R/W 0	ADDP 2 R/W 0	ADDP 1 R/W 0	ADDP 0 R/W 0

Table-12 Expanded (Indirect Address Mode) Register Map

Register	Address R/W Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
e-AFE(1)	02H R/W Default	AFE 7 R/W 0	AFE 6 R/W 0	AFE 5 R/W 0	AFE 4 R/W 0	AFE 3 R/W 0	AFE 2 R/W 0	AFE 1 R/W 0	AFE 0 R/W 0
e-RPDN	03H R/W Default	RPDN 7 R/W 0	RPDN 6 R/W 0	RPDN 5 R/W 0	RPDN 4 R/W 0	RPDN 3 R/W 0	RPDN 2 R/W 0	RPDN 1 R/W 0	RPDN 0 R/W 0
e-TPDN	04H R/W Default	TPDN 7 R/W 0	TPDN 6 R/W 0	TPDN 5 R/W 0	TPDN 4 R/W 0	TPDN 3 R/W 0	TPDN 2 R/W 0	TPDN 1 R/W 0	TPDN 0 R/W 0
e-EQUA	07H R/W Default	EQUA 7 R/W 0	EQUA 6 R/W 0	EQUA 5 R/W 0	EQUA 4 R/W 0	EQUA 3 R/W 0	EQUA 2 R/W 0	EQUA 1 R/W 0	EQUA 0 R/W 0
ADDP	1FH R/W Default	ADDP 7 R/W 0	ADDP 6 R/W 0	ADDP 5 R/W 0	ADDP 4 R/W 0	ADDP 3 R/W 0	ADDP 2 R/W 0	ADDP 1 R/W 0	ADDP 0 R/W 0

1. In host mode, register **e-AFE** has to be set to ‘FFH’ for proper device operation. See e-AFE: AFE Enable Selection Register (R/W, Expanded Address = 02H) on page 28 for more details.

3.3 REGISTER DESCRIPTION

3.3.1 PRIMARY REGISTERS

ID: Device ID Register (R, Address = 00H)

Symbol	Position	Default	Description
ID[7:0]	ID.7-0	10H	An 8-bit word is pre-set into the device as the identification and revision number. This number is different with the functional changes and is mask programmed.

RL0: G.772 Monitoring, Remote Loopback Configuration Register (R/W, Address = 02H)

Symbol	Position	Default	Description
-	RL.7-1	0000000	Reserved
RL[0]	RL.0	0	0 = Normal operation. (Default) 1 = Remote loopback enabled.

TAO: Transmit All Ones Configuration Register (R/W, Address = 03H)

Symbol	Position	Default	Description
TAO[7:0]	TAO.7-0	00H	0 = Normal operation. (Default) 1 = Transmit all ones.

LOS: Loss of Signal Status Register (R, Address = 04H)

Symbol	Position	Default	Description
LOS[7:0]	LOS.7-0	00H	0 = Normal operation. (Default) 1 = Loss of signal detected.

DF: Driver Fault Status Register (R, Address = 05H)

Symbol	Position	Default	Description
DF[7:0]	DF.7-0	00H	0 = Normal operation. (Default) 1 = Driver fault detected.

LOSM: Loss of Signal Interrupt Mask Register (R/W, Address = 06H)

Symbol	Position	Default	Description
LOSM[7:0]	LOSM.7-0	00H	0 = LOS interrupt is not allowed. (Default) 1 = LOS interrupt is allowed.

DFM: Driver Fault Interrupt Mask Register (R/W, Address = 07H)

Symbol	Position	Default	Description
DFM[7:0]	DFM.7-0	00H	0 = Driver fault interrupt not allowed. (Default) 1 = Driver fault interrupt allowed.

LOSI: Loss of Signal Interrupt Status Register (R, Address = 08H)

Symbol	Position	Default	Description
LOSI[7:0]	LOSI.7-0	00H	0 = (Default). Or after a **LOS** read operation. 1 = Any transition on **LOSn** (Corresponding **LOSMn** is set to ‘1’).

DFI: Driver Fault Interrupt Status Register (R, Address = 09H)

Symbol	Position	Default	Description
DFI[7:0]	DFI.7-0	00H	0 = (Default). Or after a **DF** read operation. 1 = Any transition on **DFn** (Corresponding **DFMn** is set to '1').

RS: Software Reset Register (W, Address = 0AH)

Symbol	Position	Default	Description
RS[7:0]	RS.7-0	FFH	Writing to this register will not change the content in this register but initiate a 1 µs reset cycle, which means all the registers in the device are set to their default values.

PMON: Performance Monitor Configuration Register (R/W, Address = 0BH)

Symbol	Position	Default	Description
-	PMON.7-4	0000	0 = Normal operation. (Default) 1 = Reserved.
MC[3:0]	PMON.3-0	0000	0000 = Normal operation without monitoring (Default) 0001 = Monitor Receiver 1 0010 = Monitor Receiver 2 0011 = Monitor Receiver 3 0100 = Monitor Receiver 4 0101 = Monitor Receiver 5 0110 = Monitor Receiver 6 0111 = Monitor Receiver 7 1000 = Normal operation without monitoring 1001 = Monitor Transmitter 1 1010 = Monitor Transmitter 2 1011 = Monitor Transmitter 3 1100 = Monitor Transmitter 4 1101 = Monitor Transmitter 5 1110 = Monitor Transmitter 6 1111 = Monitor Transmitter 7

LAC: LOS/AIS Criteria Configuration Register (R/W, Address = 0DH)

Symbol	Position	Default	Description
LAC[7:0]	LAC.7-0	00H	For E1 mode, the criterion is selected as below: 0 = G.775 (Default) 1 = ETSI 300 233 For T1 mode, the criterion meets T1.231.

ATAO: Automatic TAOS Configuration Register (R/W, Address = 0EH)

Symbol	Position	Default	Description
ATAO[7:0]	ATAO.7-0	00H	0 = No automatic transmit all ones. (Default) 1 = Automatic transmit all ones to the line side during LOS.

GCF: Global Configuration Register (R/W, Address = 0FH)

Symbol	Position	Default	Description
-	GCF.7-6	00	0 = Normal operation. 1 = Reserved.
SCPB	GCF.5	0	0 = Short circuit protection is enabled. 1 = Short circuit protection is disabled.
-	GCF.4-0	00000	0 = Normal operation. 1 = Reserved.

TSIA: Indirect Address Register for Transmit Template Select Registers (R/W, Address = 10H)

Symbol	Position	Default	Description
-	TSIA.7-3	00000	0 = Normal operation. (Default) 1 = Reserved.
TSIA[2:0]	TSIA.2-0	000	000 = Channel 0 (Default) 001 = Channel 1 010 = Channel 2 011 = Channel 3 100 = Channel 4 101 = Channel 5 110 = Channel 6 111 = Channel 7

TS: Transmit Template Select Register (R/W, Address = 11H)

Symbol	Position	Default	Description		
-	TS.7-3	00000	0 = Normal operation. (Default) 1 = Reserved.		
TS[2-0]	TS.2-0	000	TS[2:0] pins select one of eight built-in transmit template for different applications.		
			TS[2:0]	**Mode**	**Cable Length**
			000	E1	75 Ω coaxial cable/120 Ω twisted pair cable.
			001	Reserved.	
			010		
			011	T1	0 - 133 ft.
			100	T1	133 - 266 ft.
			101	T1	266 - 399 ft.
			110	T1	399 - 533 ft.
			111	T1	533 - 655 ft.

OE: Output Enable Configuration Register (R/W, Address = 12H)

Symbol	Position	Default	Description
OE[7:0]	OE.7-0	00H	0 = Transmit drivers enabled. (Default) 1 = Transmit drivers in high impedance state.

ADDP: Address Pointer Control Register (R/W, Address = 1F H)

Symbol	Position	Default	Description
ADDP[7:0]	ADDP.7-0	00H	Two kinds of configuration in this register can be set to switch between primary register bank and expanded register bank. When power up, the address pointer will point to the top address of primary register bank automatically. 00H = The address pointer points to the top address of primary register bank (default). AAH = The address pointer points to the top address of expanded register bank.

3.3.2 EXPANDED REGISTER DESCRIPTION

e-AFE: AFE Enable Selection Register (R/W, Expanded Address = 02H)

Symbol	Position	Default	Description
AFE[7:0]	AFE.7-0	00H(1)	0 = Reserved (Default) Note: For remote loopback operation in G.772 monitoring mode, bit 0 can be set to '0'. 1 = AFE mode enabled.

1. In host mode, AFE[7:0] bits must be set to 'FFH' for normal device operation.

e-RPDN: Receiver n Powerdown Register (R/W, Expanded Address = 03H)

Symbol	Position	Default	Description
RPDN[7:0]	RPDN.7-0	00H	0 = Normal operation. (Default) 1 = Receiver n is powered down.

e-TPDN: Transmitter n Powerdown Register (R/W, Expanded Address = 04H)

Symbol	Position	Default	Description
TPDN[7:0]	TPDN.7-0	00H	0 = Normal operation. (Default) 1 = Transmitter n is powered down(1) (the corresponding transmit output driver enters a low power high impedance mode).

1. Transmitter n is powered down when either pin TCLKn is pulled low or TPDNn is set to '1'

e-EQUA: Receive Equalizer Enable/Disable Register (R/W, Expanded Address = 07H)

Symbol	Position	Default	Description
EQUA[7:0]	EQUA.7-0	00H	0 = Normal operation. (Default) 1 = Equalizer in Receiver n is enabled, which can improve the receive performance when transmission length is more than 200 m.

4 IEEE STD 1149.1 JTAG TEST ACCESS PORT

The IDT82V2048L supports the digital Boundary Scan Specification as described in the IEEE 1149.1 standards.

The boundary scan architecture consists of data and instruction registers plus a Test Access Port (TAP) controller. Control of the TAP is achieved through signals applied to the TMS and TCK pins. Data is shifted into the registers via the TDI pin, and shifted out of the registers via the TDO pin. JTAG test data are clocked at a rate determined by JTAG test clock.

The JTAG boundary scan registers includes BSR (Boundary Scan Register), IDR (Device Identification Register), BR (Bypass Register) and IR (Instruction Register). These will be described in the following pages. Refer to Figure-12 for architecture.

4.1 JTAG INSTRUCTIONS AND INSTRUCTION REGISTER (IR)

The IR with instruction decode block is used to select the test to be executed or the data register to be accessed or both.

The instructions are shifted in LSB first to this 3-bit register. See Table-13 Instruction Register Description on page 30 for details of the codes and the instructions related.

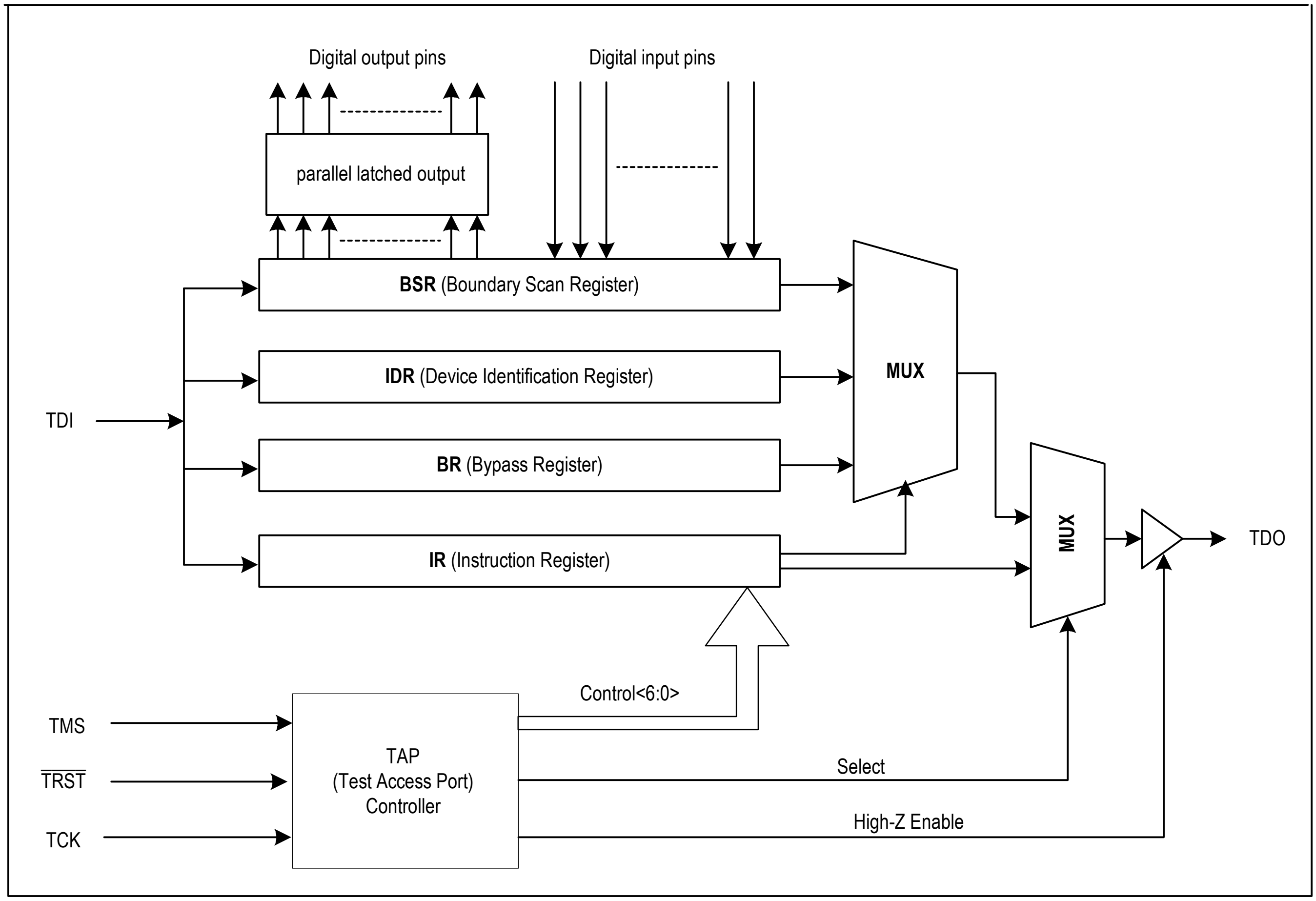


Figure-12 JTAG Architecture

Table-13 Instruction Register Description

IR Code	Instruction	Comments
000	Extest	The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is placed between TDI and TDO. The signal on the input pins can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. The signal on the output pins can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.
100	Sample/Preload	The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. The normal path between IDT82V2048L logic and the I/O pins is maintained. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.
110	Idcode	The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.
111	Bypass	The bypass instruction shifts data from input TDI to output TDO with one TCK clock period delay. The instruction is used to bypass the device.

Table-14 Device Identification Register Description

Bit No.	Comments
0	Set to '1'
1~11	Producer Number
12~27	Part Number
28~31	Device Revision

4.2 JTAG DATA REGISTER

4.2.1 DEVICE IDENTIFICATION REGISTER (IDR)

The IDR can be set to define the producer number, part number and the device revision, which can be used to verify the proper version or revision number that has been used in the system under test. The IDR is 32 bits long and is partitioned as in Table-14. Data from the IDR is shifted out to TDO LSB first.

4.2.2 BYPASS REGISTER (BR)

The BR consists of a single bit. It can provide a serial path between the TDI input and TDO output, bypassing the BSR to reduce test access times.

4.2.3 BOUNDARY SCAN REGISTER (BSR)

The BSR can apply and read test patterns in parallel to or from all the digital I/O pins. The BSR is a 98 bits long shift register and is initialized and read using the instruction EXTEST or SAMPLE/PRELOAD. Each pin is related to one or more bits in the BSR. Please refer to Table-15 for details of BSR bits and their functions.

Table-15 Boundary Scan Register Description

Bit No.	Bit Symbol	Pin Signal	Type	Comments
0	POUT0	D0	I/O	
1	PIN0	D0	I/O	
2	POUT1	D1	I/O	
3	PIN1	D1	I/O	
4	POUT2	D2	I/O	
5	PIN2	D2	I/O	
6	POUT3	D3	I/O	
7	PIN3	D3	I/O	
8	POUT4	D4	I/O	
9	PIN4	D4	I/O	
10	POUT5	D5	I/O	
11	PIN5	D5	I/O	
12	POUT6	D6	I/O	
13	PIN6	D6	I/O	
14	POUT7	D7	I/O	
15	PIN7	D7	I/O	

Table-15 Boundary Scan Register Description (Continued)

Bit No.	Bit Symbol	Pin Signal	Type	Comments
16	PIOS	N/A	-	Controls pins D[7:0]. When ‘0’, the pins are configured as outputs. The output values to the pins are set in POUT 7~0. When ‘1’, the pins are in high impedance. The input values to the pins are read in PIN 7~0.
17	TCLK1	TCLK1	I	
18	TDP1	TDP1	I	
19	TDN1	TDN1	I	
20	RC1	RC1	O	
21	RDP1	RDP1	O	
22	RDN1	RDN1	O	
23	HZEN1	N/A	-	Controls pin RDP1, RDN1 and RC1. When ‘0’, the outputs are enabled on the pins. When ‘1’, the pins are in high impedance.
24	LOS1	LOS1	O	
25	TCLK0	TCLK0	I	
26	TDP0	TDP0	I	
27	TDN0	TDN0	I	
28	RC0	RC0	O	
29	RDP0	RDP0	O	
30	RDN0	RDN0	O	
31	HZEN0	N/A	-	Controls pin RDP0, RDN0 and RC0. When ‘0’, the outputs are enabled on the pins. When ‘1’, the pins are in high impedance.
32	LOS0	LOS0	O	
33	MODE1	MODE1	I	
34	LOS3	LOS3	O	
35	RDN3	RDN3	O	
36	RDP3	RDP3	O	
37	HZEN3	N/A	-	Controls pin RDP3, RDN3 and RC3. When ‘0’, the outputs are enabled on the pins. When ‘1’, the pins are in high impedance.
38	RC3	RC3	O	
39	TDN3	TDN3	I	
40	TDP3	TDP3	I	
41	TCLK3	TCLK3	I	
42	LOS2	LOS2	O	
43	RDN2	RDN2	O	
44	RDP2	RDP2	O	
45	HZEN2	N/A	-	Controls pin RDP2, RDN2 and RC2. When ‘0’, the outputs are enabled on the pins. When ‘1’, the pins are in high impedance.
46	RC2	RC2	O	
47	TDN2	TDN2	I	
48	TDP2	TDP2	I	
49	TCLK2	TCLK2	I	
50	INT	$\overline{\text{INT}}$	O	
51	ACK	$\overline{\text{ACK}}$	O	
52	SDORDYS	N/A	-	Control pin $\overline{\text{ACK}}$. When ‘0’, the output is enabled on pin $\overline{\text{ACK}}$. When ‘1’, the pin is in high impedance.
53	WRB	$\overline{\text{DS}}$	I	
54	RDB	R/$\overline{\text{W}}$	I	
55	ALE	ALE	I	

Table-15 Boundary Scan Register Description (Continued)

Bit No.	Bit Symbol	Pin Signal	Type	Comments
56	CSB	$\overline{CS}$	I	
57	MODE0	MODE0	I	
58	TCLK5	TCLK5	I	
59	TDP5	TDP5	I	
60	TDN5	TDN5	I	
61	RC5	RC5	O	
62	RDP5	RDP5	O	
63	RDN5	RDN5	O	
64	HZEN5	N/A	-	Controls pin RDP5, RDN5 and RC5. When ‘0’, the outputs are enabled on the pins. When ‘1’, the pins are in high impedance.
65	LOS5	LOS5	O	
66	TCLK4	TCLK4	I	
67	TDP4	TDP4	I	
68	TDN4	TDN4	I	
69	RC4	RC4	O	
70	RDP4	RDP4	O	
71	RDN4	RDN4	O	
72	HZEN4	N/A	-	Controls pin RDP4, RDN4 and RC4. When ‘0’, the outputs are enabled on the pins. When ‘1’, the pins are in high impedance.
73	LOS4	LOS4	O	
74	OE	OE	I	
75	CLKE	CLKE	I	
76	LOS7	LOS7	O	
77	RDN7	RDN7	O	
78	RDP7	RDP7	O	
79	HZEN7	N/A	-	Controls pin RDP7, RDN7 and RC7. When ‘0’, the outputs are enabled on the pins. When ‘1’, the pins are in high impedance.
80	RC7	RC7	O	
81	TDN7	TDN7	I	
82	TDP7	TDP7	I	
83	TCLK7	TCLK7	I	
84	LOS6	LOS6	O	
85	RDN6	RDN6	O	
86	RDP6	RDP6	O	
87	HZEN6	N/A	-	Controls pin RDP6, RDN6 and RC6. When ‘0’, the outputs are enabled on the pins. When ‘1’, the pins are in high impedance.
88	RC6	RC6	O	
89	TDN6	TDN6	I	
90	TDP6	TDP6	I	
91	TCLK6	TCLK6	I	
92	MCLK	MCLK	I	
93	MODE2	MODE2	I	
94	A4	A4	I	
95	A3	A3	I	
96	A2	A2	I	
97	A1	A1	I	
98	A0	A0	I	

4.3 TEST ACCESS PORT CONTROLLER

The TAP controller is a 16-state synchronous state machine. Figure-13 shows its state diagram A description of each state follows. Note that the figure contains two main branches to access either the data or instruction registers. The value shown next to each state transition in this figure states the value present at TMS at each rising edge of TCK. Refer to Table-16 for details of the state description.

Table-16 TAP Controller State Description

State	Description
Test Logic Reset	In this state, the test logic is disabled. The device is set to normal operation. During initialization, the device initializes the instruction register with the IDCODE instruction. Regardless of the original state of the controller, the controller enters the Test-Logic-Reset state when the TMS input is held high for at least 5 rising edges of TCK. The controller remains in this state while TMS is high. The device processor automatically enters this state at power-up.
Run-Test/Idle	This is a controller state between scan operations. Once in this state, the controller remains in the state as long as TMS is held low. The instruction register and all test data registers retain their previous state. When TMS is high and a rising edge is applied to TCK, the controller moves to the Select-DR state.
Select-DR-Scan	This is a temporary controller state and the instruction does not change in this state. The test data register selected by the current instruction retains its previous state. If TMS is held low and a rising edge is applied to TCK when in this state, the controller moves into the Capture-DR state and a scan sequence for the selected test data register is initiated. If TMS is held high and a rising edge applied to TCK, the controller moves to the Select-IR-Scan state.
Capture-DR	In this state, the Boundary Scan Register captures input pin data if the current instruction is EXTEST or SAMPLE/PRELOAD. The instruction does not change in this state. The other test data registers, which do not have parallel input, are not changed. When the TAP controller is in this state and a rising edge is applied to TCK, the controller enters the Exit1-DR state if TMS is high or the Shift-DR state if TMS is low.
Shift-DR	In this controller state, the test data register connected between TDI and TDO as a result of the current instruction shifts data on stage toward its serial output on each rising edge of TCK. The instruction does not change in this state. When the TAP controller is in this state and a rising edge is applied to TCK, the controller enters the Exit1-DR state if TMS is high or remains in the Shift-DR state if TMS is low.
Exit1-DR	This is a temporary state. While in this state, if TMS is held high, a rising edge applied to TCK causes the controller to enter the Update-DR state, which terminates the scanning process. If TMS is held low and a rising edge is applied to TCK, the controller enters the Pause-DR state. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state.
Pause-DR	The pause state allows the test controller to temporarily halt the shifting of data through the test data register in the serial path between TDI and TDO. For example, this state could be used to allow the tester to reload its pin memory from disk during application of a long test sequence. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state. The controller remains in this state as long as TMS is low. When TMS goes high and a rising edge is applied to TCK, the controller moves to the Exit2-DR state.
Exit2-DR	This is a temporary state. While in this state, if TMS is held high, a rising edge applied to TCK causes the controller to enter the Update-DR state, which terminates the scanning process. If TMS is held low and a rising edge is applied to TCK, the controller enters the Shift-DR state. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state.
Update-DR	The Boundary Scan Register is provided with a latched parallel output to prevent changes while data is shifted in response to the EXTEST and SAMPLE/PRELOAD instructions. When the TAP controller is in this state and the Boundary Scan Register is selected, data is latched into the parallel output of this register from the shift-register path on the falling edge of TCK. The data held at the latched parallel output changes only in this state. All shift-register stages in the test data register selected by the current instruction retain their previous value and the instruction does not change during this state.
Select-IR-Scan	This is a temporary controller state. The test data register selected by the current instruction retains its previous state. If TMS is held low and a rising edge is applied to TCK when in this state, the controller moves into the Capture-IR state, and a scan sequence for the instruction register is initiated. If TMS is held high and a rising edge is applied to TCK, the controller moves to the Test-Logic-Reset state. The instruction does not change during this state.
Capture-IR	In this controller state, the shift register contained in the instruction register loads a fixed value of '100' on the rising edge of TCK. This supports fault-isolation of the board-level serial test data path. Data registers selected by the current instruction retain their value and the instruction does not change during this state. When the controller is in this state and a rising edge is applied to TCK, the controller enters the Exit1-IR state if TMS is held high, or the Shift-IR state if TMS is held low.
Shift-IR	In this state, the shift register contained in the instruction register is connected between TDI and TDO and shifts data one stage towards its serial output on each rising edge of TCK. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state. When the controller is in this state and a rising edge is applied to TCK, the controller enters the Exit1-IR state if TMS is held high, or remains in the Shift-IR state if TMS is held low.

Table-16 TAP Controller State Description (Continued)

State	Description
Exit1-IR	This is a temporary state. While in this state, if TMS is held high, a rising edge applied to TCK causes the controller to enter the Update-IR state, which terminates the scanning process. If TMS is held low and a rising edge is applied to TCK, the controller enters the Pause-IR state. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state.
Pause-IR	The pause state allows the test controller to temporarily halt the shifting of data through the instruction register. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state. The controller remains in this state as long as TMS is low. When TMS goes high and a rising edge is applied to TCK, the controller moves to the Exit2-IR state.
Exit2-IR	This is a temporary state. While in this state, if TMS is held high, a rising edge applied to TCK causes the controller to enter the Update-IR state, which terminates the scanning process. If TMS is held low and a rising edge is applied to TCK, the controller enters the Shift-IR state. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state.
Update-IR	The instruction shifted into the instruction register is latched into the parallel output from the shift-register path on the falling edge of TCK. When the new instruction has been latched, it becomes the current instruction. The test data registers selected by the current instruction retain their previous value.

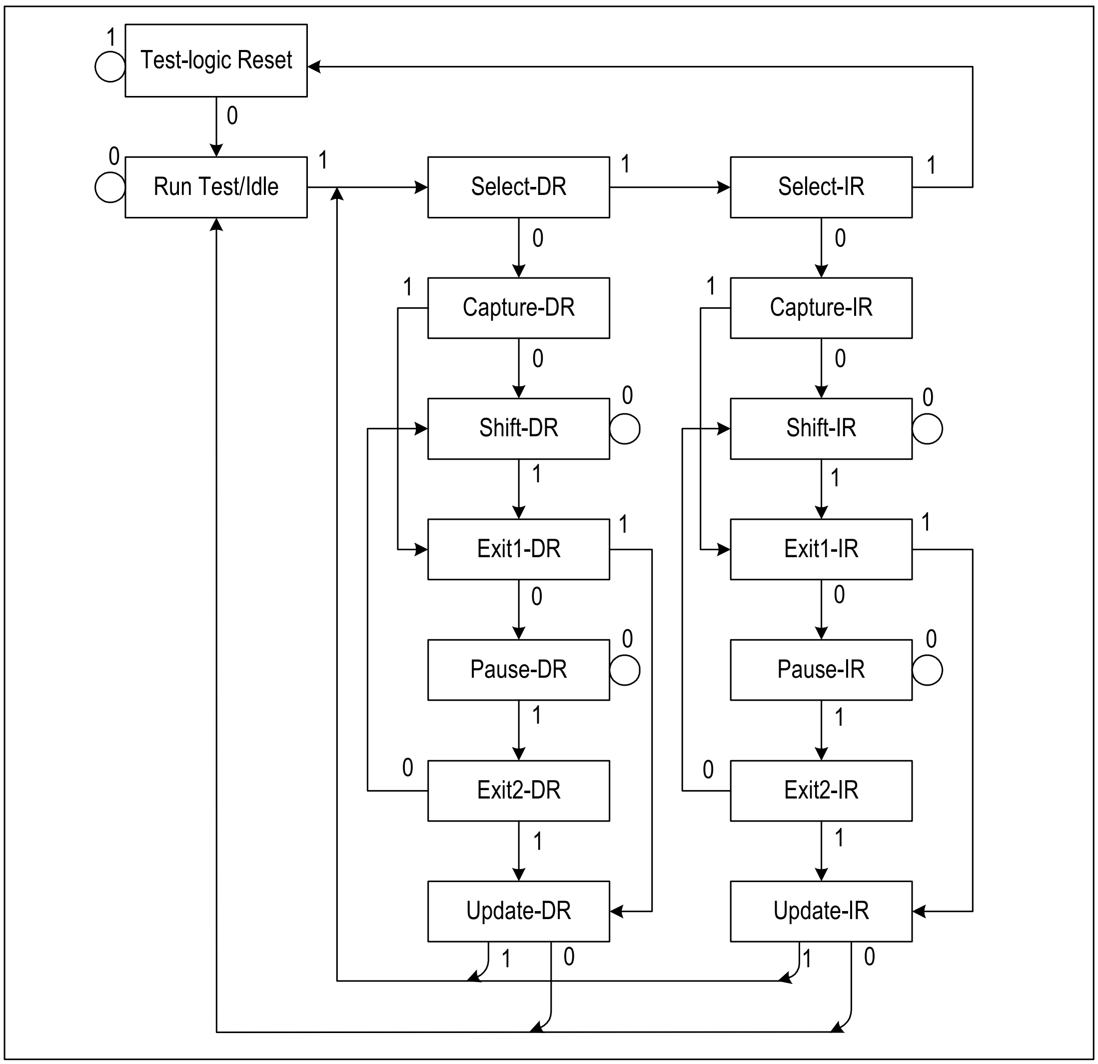


Figure-13 JTAG State Diagram

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Min	Max	Unit
VDDA, VDDD	Core Power Supply	-0.5	4.0	V
VDDIO0, VDDIO1	I/O Power Supply	-0.5	4.0	V
VDDT0-7	Transmit Power Supply	-0.5	7.0	V
Vin	Input Voltage, any digital pin	GND-0.5	5.5	V
	Input Voltage[1], RTIPn pins and RRINGn pins	GND-0.5	VDDA+ 0.5 VDDD+ 0.5	V V
	ESD Voltage, any pin[2]	2000		V
Iin	Transient Latch-up Current, any pin		100	mA
	Input Current, any digital pin[3]	-10	10	mA
	DC Input Current, any analog pin[3]		±100	mA
Pd	Maximum Power Dissipation in package		1.6	W
Ts	Storage Temperature	-65	+150	°C

CAUTION: Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. Referenced to ground
2. Human body model
3. Constant input current

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
VDDA, VDDD	Core Power Supply	3.13	3.3	3.47	V
VDDIO	I/O Power Supply	3.13	3.3	3.47	V
VDDT[1]	Transmitter Supply				
	3.3 V	3.13	3.3	3.47	V
	5 V	4.75	5.0	5.25	V
T_A	Ambient Operating Temperature	-40	25	85	°C
R_L	Output load at TTIPn pins and TRINGn pins	25			Ω
I_{VDD}	Average Core Power Supply Current[2]		55	65	mA
I_{VDDIO}	I/O Power Supply Current[3]		15	25	mA
I_{VDDT}	Average transmitter power supply current, T1 mode[2],[4],[5]				
	50% ones density data:			230	mA
	100% ones density data:			440	mA

1. T1 is only 5V VDDT.
2. Maximum power and current consumption over the full operating temperature and power supply voltage range. Includes all channels.
3. Digital output is driving 50 pF load, digital input is within 10% of the supply rails.
4. T1 maximum values measured with maximum cable length (LEN = 111). Typical values measured with typical cable length (LEN = 101).
5. Power consumption includes power absorbed by line load and external transmitter components.

POWER CONSUMPTION

Symbol	Parameter	LEN	Min	Typ	Max[1][2]	Unit
	E1, 3.3 V, 75 Ω Load 50% ones density data: 100% ones density data:	 000 000	 - -	 662 1100	 - 1177	 mW mW
	E1, 3.3 V, 120 Ω Load 50% ones density data: 100% ones density data:	 000 000	 - -	 576 930	 - 992	 mW mW
	E1, 5.0 V, 75 Ω Load 50% ones density data: 100% ones density data:	 000 000	 - -	 910 1585	 - 1690	 mW mW
	E1, 5.0 V, 120 Ω Load 50% ones density data: 100% ones density data:	 000 000	 - -	 785 1315	 - 1410	 mW mW
	T1, 5.0 V, 100 Ω Load[3] 50% ones density data: 100% ones density data:	 101 111	 - -	 1185 2395	 - 2670	 mW mW

1. Maximum power and current consumption over the full operating temperature and power supply voltage range. Includes all channels.

2. Power consumption includes power absorbed by line load and external transmitter components.

3. T1 maximum values measured with maximum cable length (LEN = 111). Typical values measured with typical cable length (LEN = 101).

DC CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input Low Level Voltage MODE2 and Dn pins All other digital inputs pins			 $\frac{1}{3}$ VDDIO-0.2 0.8	 V V
V_{IM}	Input Mid Level Voltage MODE2 and Dn pins	 $\frac{1}{3}$ VDDIO+0.2	 $\frac{1}{2}$ VDDIO	 $\frac{2}{3}$ VDDIO-0.2	 V
V_{IH}	Input High Voltage MODE2 and Dn pins All other digital inputs pins	 $\frac{2}{3}$ VDDIO+ 0.2 2.0			 V V
V_{OL}	Output Low level Voltage[1] (Iout = 1.6 mA)			0.4	V
V_{OH}	Output High level Voltage[1] (Iout = 400 µA)	2.4		VDDIO	V
V_{MA}	Analog Input Quiescent Voltage (RTIPn/RRINGn pin while floating)	1.33	1.4	1.47	V
I_H	Input High Level Current (MODE2 and Dn pins)			50	µA
I_L	Input Low Level Current (MODE2 and Dn pins)			50	µA
I_I	Input Leakage Current TMS, TDI and $\overline{\text{TRST}}$ pins All other digital input pins	 -10		 50 10	 µA µA
I_{ZL}	High Impedance Leakage Current	-10		10	µA
Z_{OH}	Output High Impedance on TTIPn and TRINGn pins	150			kΩ

1. Output drivers will output CMOS logic levels into CMOS loads.

TRANSMITTER CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
V_{o-p}	Output Pulse Amplitudes[1] E1, 75 Ω load E1, 120 Ω load T1, 100 Ω load	 2.14 2.7 2.4	 2.37 3.0 3.0	 2.6 3.3 3.6	 V V V
V_{O-S}	Zero (space) Level E1, 75 Ω load E1, 120 Ω load T1, 100 Ω load	 -0.237 -0.3 -0.15		 0.237 0.3 0.15	 V V V
	Transmit Amplitude Variation with supply	-1		+1	%
	Difference between pulse sequences for 17 consecutive pulses			200	mV
T_{PW}	Output Pulse Width at 50% of nominal amplitude E1: T1:	 232 338	 244 350	 256 362	 ns ns
	Ratio of the amplitudes of Positive and Negative Pulses at the center of the pulse interval	0.95		1.05	
RTX	Transmit Return Loss[2]				
	E1, 75 Ω – 51 kHz – 102 kHz 102 kHz – 2.048 MHz 2.048 MHz – 3.072 MHz	15 15 15			dB dB dB
	E1, 120 Ω – 51 kHz – 102 kHz 102 kHz – 2.048 MHz 2.048 MHz – 3.072 MHz	15 15 15			dB dB dB
	T1 (VDDT = 5 V) – 51 kHz – 102 kHz 102 kHz – 2.048 MHz 2.048 MHz – 3.072 MHz	15 15 15			dB dB dB
Td	Transmit Path Delay		3		U.I.
I_{SC}	Line Short Circuit Current [3]		180		mAp

1. E1: measured at the line output ports; T1: measured at the DSX

2. Test at IDT82V2048L evaluation board

3. Measured on device, between TTIPn and TRINGn

RECEIVER CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
ATT	Permissible Cable Attenuation (E1: @ 1024 kHz, T1: @ 772 kHz)			15	dB
IA	Input Amplitude	0.1		0.9	Vp
SIR	Signal to Interference Ratio Margin(1)	-15			dB
SRE	Data Decision Threshold (refer to peak input voltage)		50		%
	Data Slicer Threshold		150		mV
	Analog Loss Of Signal(2) Declare/Clear:	120/150	200/250	280/350	mVp
	Allowable consecutive zeros before LOS E1, G.775: E1, ETSI 300 233: T1, T1.231-1993		32 2048 175		
	LOS Reset Clock Recovery Mode	12.5			% ones
$JRX_{p\text{-}p}$	Peak to Peak Intrinsic Receive Jitter (JA disabled) E1 (wide band): T1 (wide band):			0.0625 0.0625	U.I. U.I.
ZDM	Receiver Differential Input Impedance		120		kΩ
ZCM	Receiver Common Mode Input Impedance to GND	10			kΩ
RRX	Receive Return Loss 51 kHz – 102 kHz 102 kHz – 2.048 MHz 2.048 MHz – 3.072 MHz	20 20 20			dB dB dB
	Receive Path Delay		3		U.I.

1. E1: per G.703, O.151 @ 6 dB cable attenuation. T1: @ 655 ft. of 22 ABAM cable

2. Measured on device, between RTIPn and RRINGn, all ones signal

TRANSCEIVER TIMING CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
	MCLK Frequency E1: T1:		 2.048 1.544		 MHz MHz
	MCLK Tolerance	-100		100	ppm
	MCLK Duty Cycle	40		60	%
Transmit Path					
	TCLK Frequency E1: T1:		 2.048 1.544		 MHz MHz
	TCLK Tolerance	-50		+50	ppm
	TCLK Duty Cycle	10		90	%
t1	Transmit Data Setup Time	40			ns
t2	Transmit Data Hold Time	40			ns
	Delay time of OE low to driver High Impedance			1	µs
	Delay time of TCLK low to driver High Impedance	40	44	48	µs
Receive Path					
t4	RDN/RDP Pulse Width(1) E1: T1:	 200 300	 244 324		 ns ns
t5	RX Data Prop. Delay(2)			40	ns
t6	Receive Rise Time(2)			14	ns
t7	Receive Fall Time(2)			12	ns

1. 0 dB cable loss

2. 15 pF load

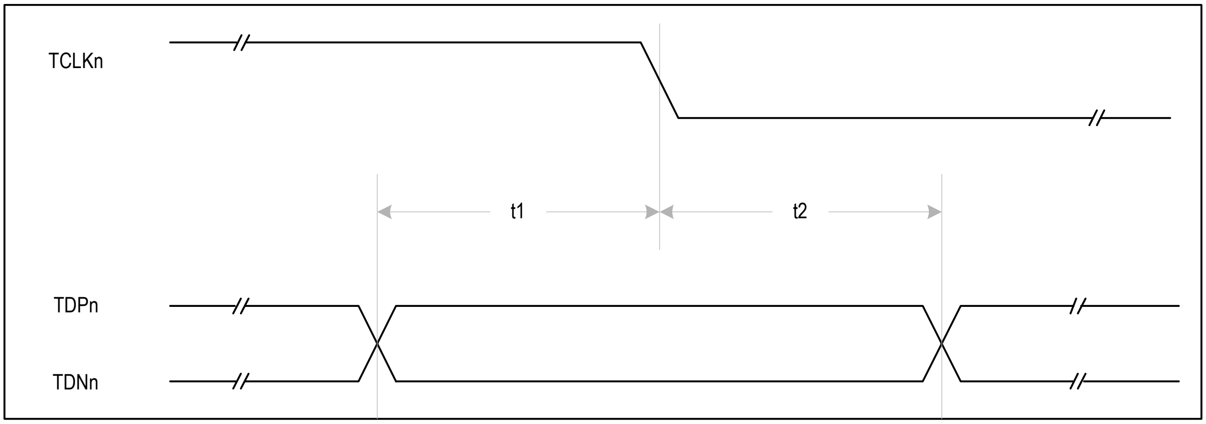


Figure-14 Transmit System Interface Timing

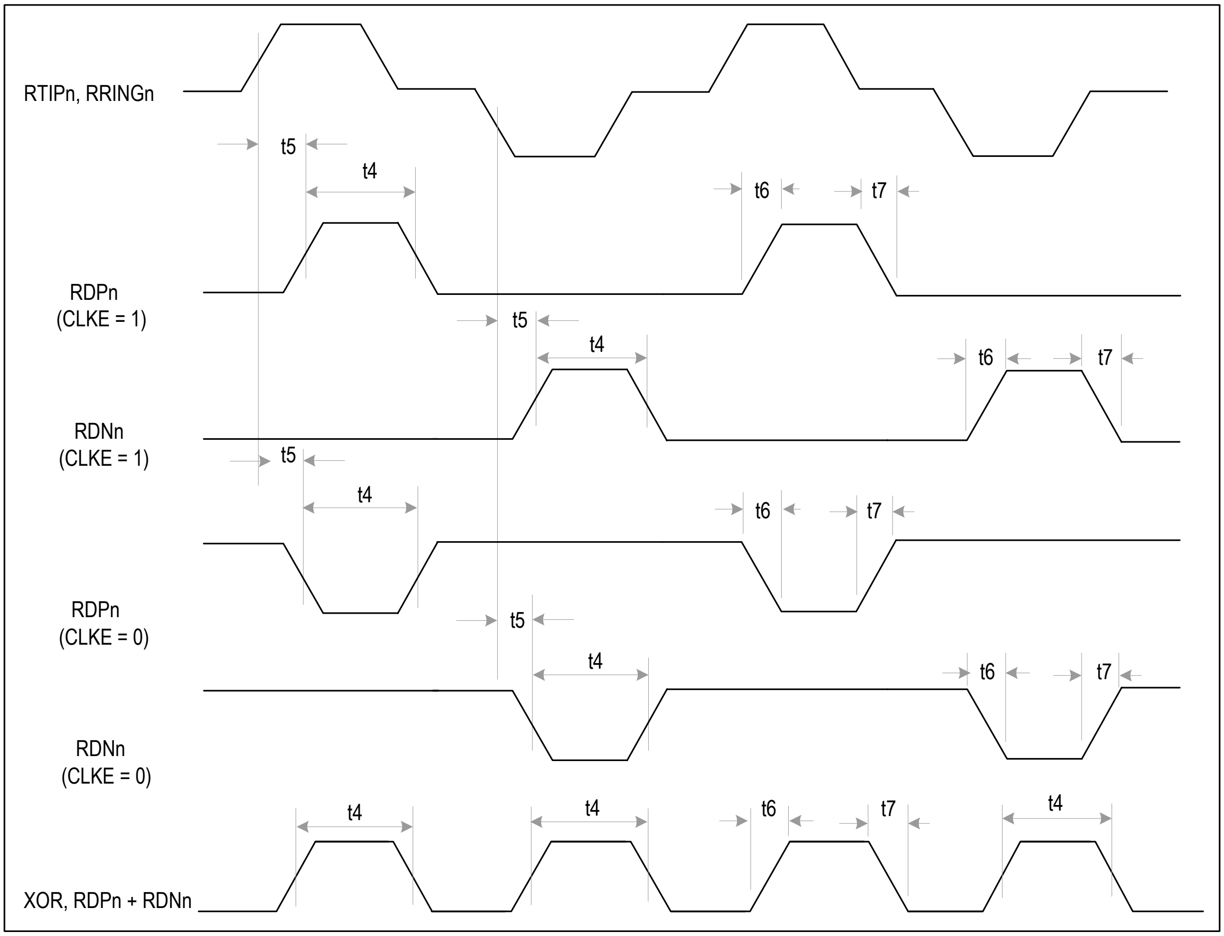


Figure-15 Receive System Interface Timing

JTAG TIMING CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Comments
t1	TCK Period	200			ns	
t2	TMS to TCK setup Time TDI to TCK Setup Time	50			ns	
t3	TCK to TMS Hold Time TCK to TDI Hold Time	50			ns	
t4	TCK to TDO Delay Time			100	ns	

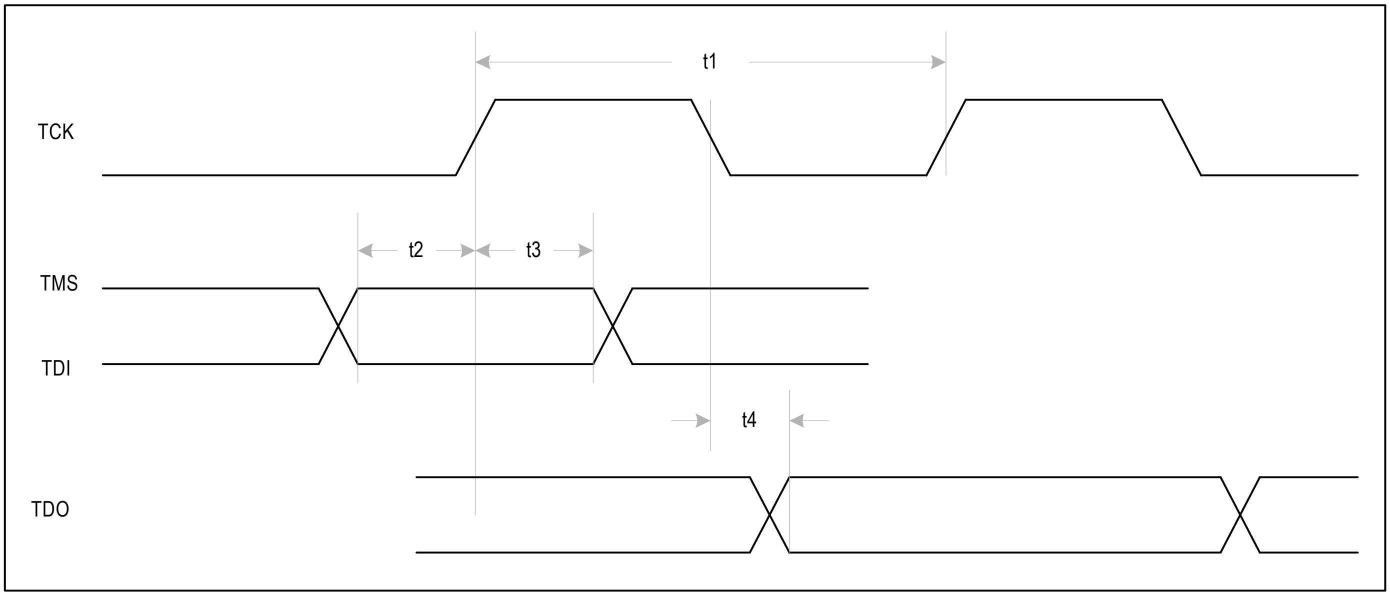


Figure-16 JTAG Interface Timing

PARALLEL HOST INTERFACE TIMING CHARACTERISTICS

INTEL MODE READ TIMING CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Comments
t1	Active $\overline{RD}$ Pulse Width	90			ns	(1)
t2	Active $\overline{CS}$ to Active $\overline{RD}$ Setup Time	0			ns	
t3	Inactive $\overline{RD}$ to Inactive $\overline{CS}$ Hold Time	0			ns	
t4	Valid Address to Inactive ALE Setup Time (in Multiplexed Mode)	5			ns	
t5	Invalid $\overline{RD}$ to Address Hold Time (in Non-Multiplexed Mode)	0			ns	
t6	Active $\overline{RD}$ to Data Output Enable Time	7.5		15	ns	
t7	Inactive $\overline{RD}$ to Data High Impedance Delay Time	7.5		15	ns	
t8	Active $\overline{CS}$ to RDY delay time	6		12	ns	
t9	Inactive $\overline{CS}$ to RDY High Impedance Delay Time	6		12	ns	
t10	Inactive $\overline{RD}$ to Inactive $\overline{INT}$ Delay Time			20	ns	
t11	Address Latch Enable Pulse Width (in Multiplexed Mode)	10			ns	
t12	Address Latch Enable to $\overline{RD}$ Setup Time (in Multiplexed Mode)	0			ns	
t13	Address Setup time to Valid Data Time (in Non-Multiplexed Mode)	18		32	ns	
t14	Inactive $\overline{RD}$ to Active RDY Delay Time	10		15	ns	
t15	Active $\overline{RD}$ to Active RDY Delay Time	30		85	ns	
t16	Inactive ALE to Address Hold Time (in Multiplexed Mode)	5			ns	

1. The t1 is determined by the start time of the valid data when the RDY signal is not used.

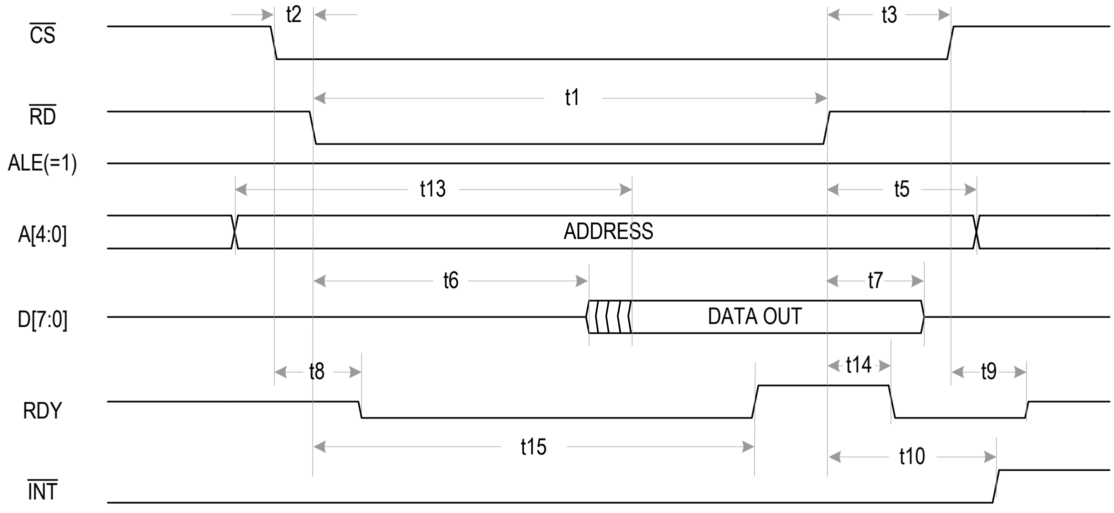


Figure-17 Non-Multiplexed Intel Mode Read Timing

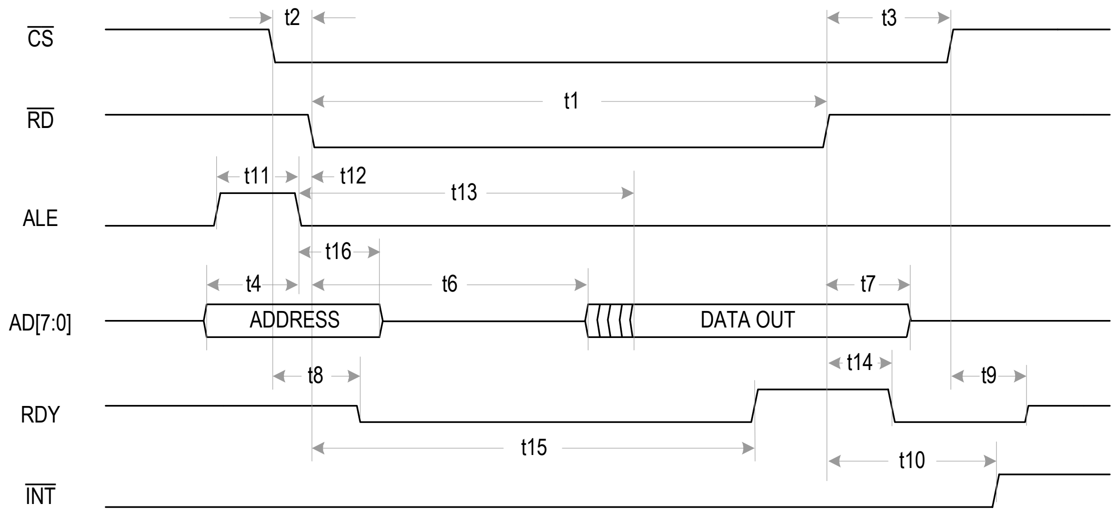


Figure-18 Multiplexed Intel Mode Read Timing

INTEL MODE WRITE TIMING CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Comments
t1	Active $\overline{WR}$ Pulse Width	90			ns	(1)
t2	Active $\overline{CS}$ to Active $\overline{WR}$ Setup Time	0			ns	
t3	Inactive $\overline{WR}$ to Inactive $\overline{CS}$ Hold Time	0			ns	
t4	Valid Address to Latch Enable Setup Time (in Multiplexed Mode)	5			ns	
t5	Invalid $\overline{WR}$ to Address Hold Time (in Non-Multiplexed Mode)	2			ns	
t6	Valid Data to Inactive $\overline{WR}$ Setup Time	5			ns	
t7	Inactive $\overline{WR}$ to Data Hold Time	10			ns	
t8	Active $\overline{CS}$ to Inactive RDY Delay Time	6		12	ns	
t9	Active $\overline{WR}$ to Active RDY Delay Time	30		85	ns	
t10	Inactive $\overline{WR}$ to Inactive RDY Delay Time	10		15	ns	
t11	Invalid $\overline{CS}$ to RDY High Impedance Delay Time	6		12	ns	
t12	Address Latch Enable Pulse Width (in Multiplexed Mode)	10			ns	
t13	Inactive ALE to $\overline{WR}$ Setup Time (in Multiplexed Mode)	0			ns	
t14	Inactive ALE to Address hold time (in Multiplexed Mode)	5			ns	
t15	Address setup time to Inactive $\overline{WR}$ time (in Non-Multiplexed Mode)	5			ns	

1. The t1 can be 15 ns when RDY signal is not used.

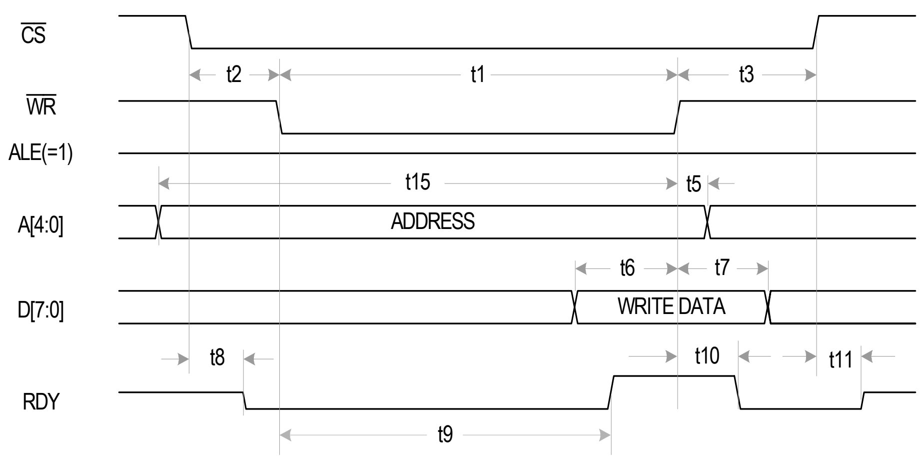


Figure-19 Non-Multiplexed Intel Mode Write Timing

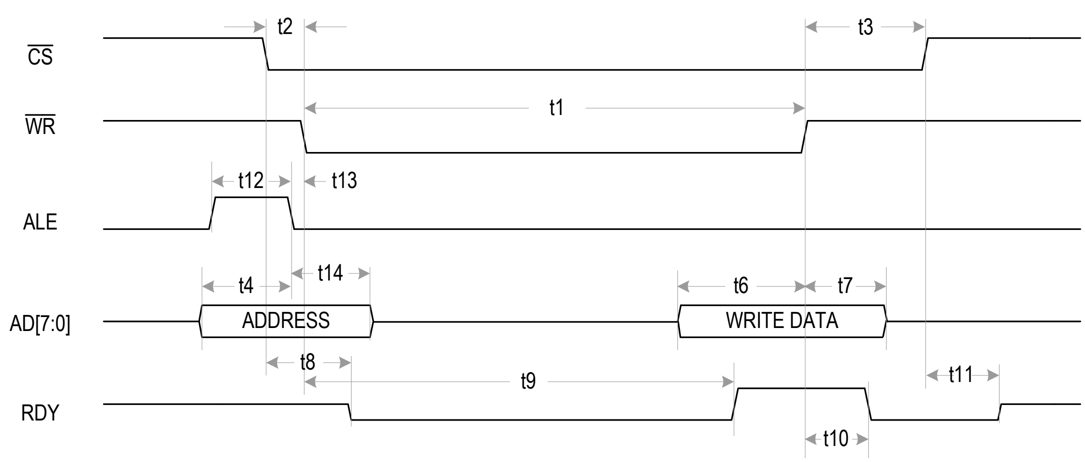


Figure-20 Multiplexed Intel Mode Write Timing

MOTOROLA MODE READ TIMING CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Comments
t1	Active $\overline{DS}$ Pulse Width	90			ns	(1)
t2	Active $\overline{CS}$ to Active $\overline{DS}$ Setup Time	0			ns	
t3	Inactive $\overline{DS}$ to Inactive $\overline{CS}$ Hold Time	0			ns	
t4	Valid R/$\overline{W}$ to Active $\overline{DS}$ Setup Time	0			ns	
t5	Inactive $\overline{DS}$ to R/$\overline{W}$ Hold Time	0.5			ns	
t6	Valid Address to Active $\overline{DS}$ Setup Time (in Non-Multiplexed Mode)	5			ns	
t7	Active $\overline{DS}$ to Address Hold Time (in Non-Multiplexed Mode)	10			ns	
t8	Active $\overline{DS}$ to Data Valid Delay Time (in Non-Multiplexed Mode)	20		35	ns	
t9	Active $\overline{DS}$ to Data Output Enable Time	7.5		15	ns	
t10	Inactive $\overline{DS}$ to Data High Impedance Delay Time	7.5		15	ns	
t11	Active $\overline{DS}$ to Active $\overline{ACK}$ Delay Time	30		85	ns	
t12	Inactive $\overline{DS}$ to Inactive $\overline{ACK}$ Delay Time	10		15	ns	
t13	Inactive $\overline{DS}$ to Invalid $\overline{INT}$ Delay Time			20	ns	
t14	Active $\overline{AS}$ to Active $\overline{DS}$ Setup Time (in Multiplexed Mode)	5			ns	

1. The t1 is determined by the start time of the valid data when the ACK signal is not used.

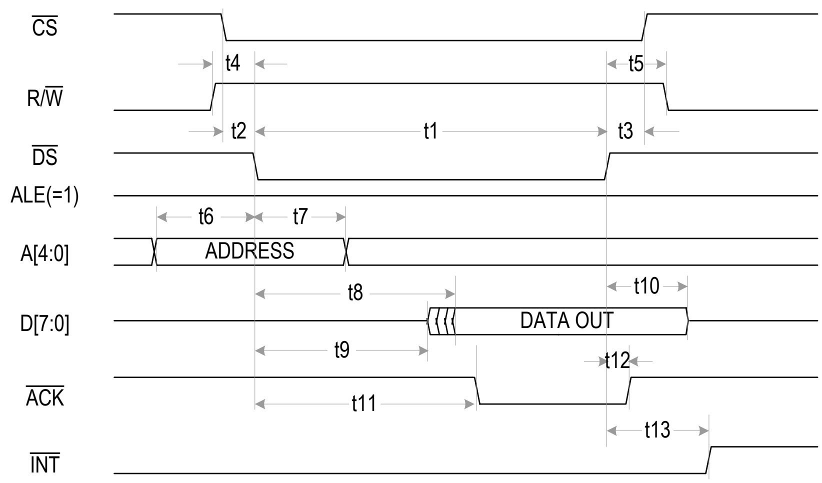


Figure-21 Non-Multiplexed Motorola Mode Read Timing

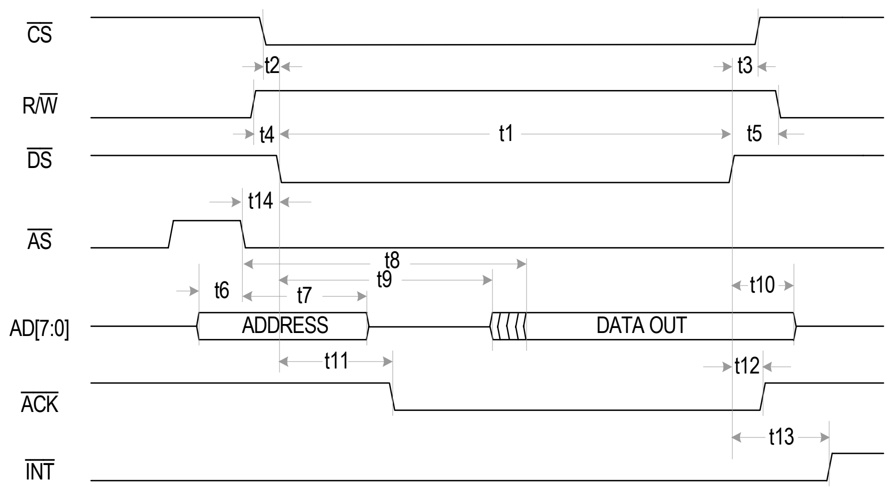


Figure-22 Multiplexed Motorola Mode Read Timing

MOTOROLA MODE WRITE TIMING CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Comments
t1	Active DS Pulse Width	90			ns	(1)
t2	Active CS to Active DS Setup Time	0			ns	
t3	Inactive DS to Inactive CS Hold Time	0			ns	
t4	Valid R/W to Active DS Setup Time	10			ns	
t5	Inactive DS to R/W Hold Time	0			ns	
t6	Valid Address to Active DS Setup Time (in Non-Multiplexed Mode)	10			ns	
t7	Valid DS to Address Hold Time (in Non-Multiplexed Mode)	10			ns	
t8	Valid Data to Inactive DS Setup Time	5			ns	
t9	Inactive DS to Data Hold Time	10			ns	
t10	Active DS to Active ACK Delay Time	30		85	ns	
t11	Inactive DS to Inactive ACK Delay Time	10		15	ns	
t12	Active AS to Active DS (in Multiplexed Mode)	0			ns	
t13	Inactive DS to Inactive AS Hold Time (in Multiplexed Mode)	15			ns	

1. The t1 can be 15ns when the ACK signal is not used.

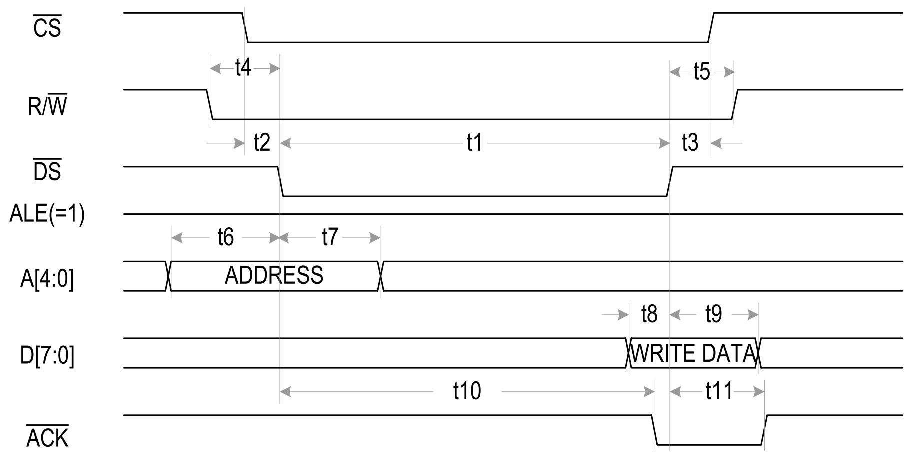


Figure-23 Non-Multiplexed Motorola Mode Write Timing

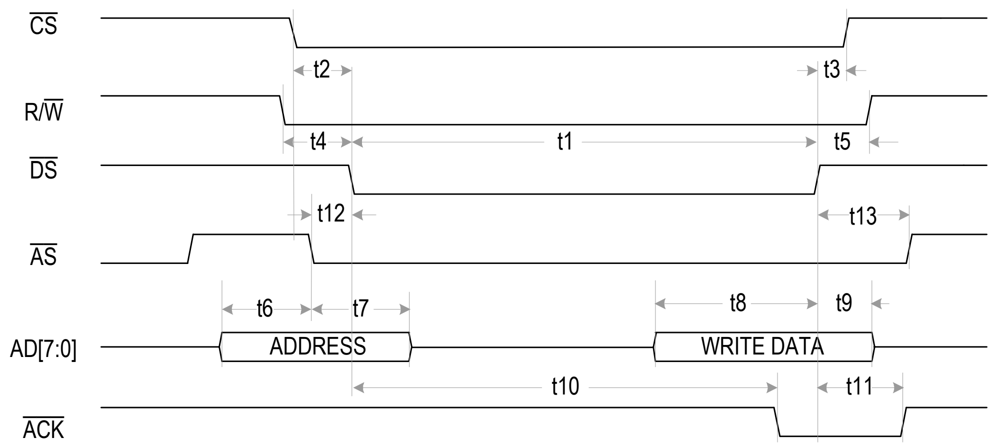


Figure-24 Multiplexed Motorola Mode Writing Timing

SERIAL HOST INTERFACE TIMING CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Comments
t1	SCLK High Time	25			ns	
t2	SCLK Low Time	25			ns	
t3	Active $\overline{CS}$ to SCLK Setup Time	10			ns	
t4	Last SCLK Hold Time to Inactive $\overline{CS}$ Time	50			ns	
t5	$\overline{CS}$ Idle Time	50			ns	
t6	SDI to SCLK Setup Time	5			ns	
t7	SCLK to SDI Hold Time	5			ns	
t8	Rise/Fall Time (any pin)			100	ns	
t9	SCLK Rise and Fall Time			50	ns	
t10	SCLK to SDO Valid Delay Time		25	35	ns	Load = 50 pF
t11	SCLK Falling Edge to SDO High Impedance Hold Time (CLKE = 0) or $\overline{CS}$ Rising Edge to SDO High Impedance Hold Time (CLKE = 1)		100		ns	

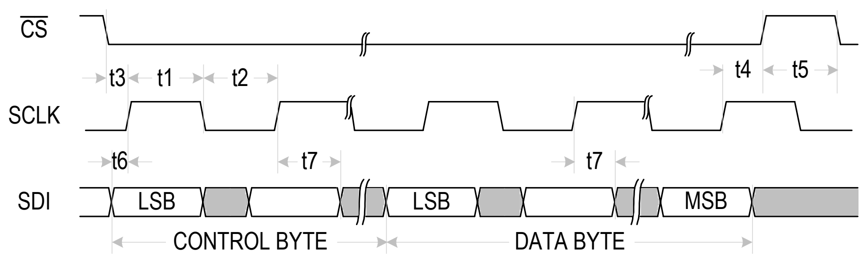


Figure-25 Serial Interface Write Timing

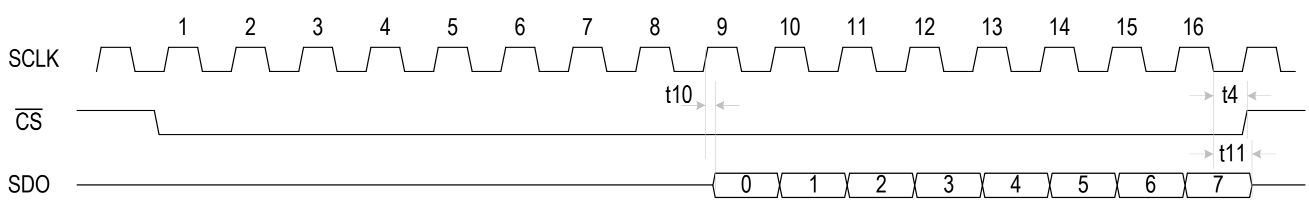


Figure-26 Serial Interface Read Timing with CLKE = 0

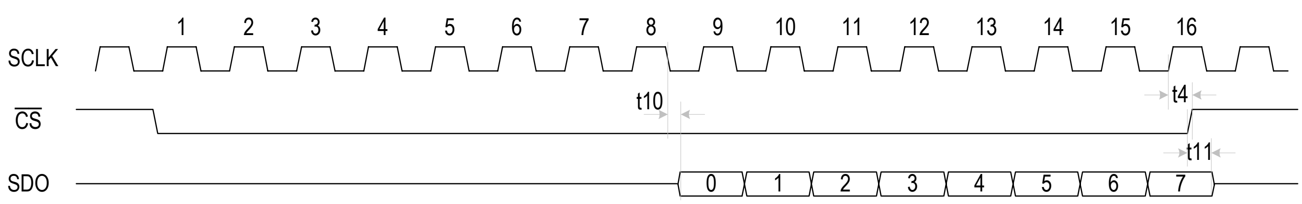


Figure-27 Serial Interface Read Timing with CLKE = 1

ORDERING INFORMATION

IDT XXXXXXX (Device Type) XX (Package) X (Process/ Temperature Range)

Blank	Industrial (-40 °C to + 85 °C)
BB	Plastic Ball Grid Array (PBGA, BB160)
BBG	Green Plastic Ball Grid Array (PBGA, BBG160)
DA	Thin Quad Flatpack (TQFP, DA144)
DAG	Green Thin Quad Flatpack (TQFP, DAG144)
82V2048L	T1/E1 Short Haul Analog Front End

DATASHEET DOCUMENT HISTORY

07/29/2005 pgs. 1, 4, 5, 7 to 10, 13, 15 to 17, 19, 20, 22, 23, 25, 25, 28, 32, 35, 37 to 40, 43 to 47

CORPORATE HEADQUARTERS
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San Jose, CA 95138
www.idt.com

for SALES:
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