

14 Pin DIP 5 Tap Fast-TTL Logic Compatible Active Delay Lines

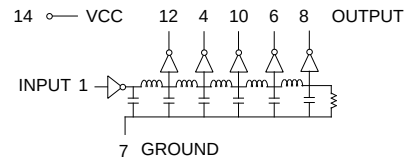
TAP DELAYS ±5% or ±2 nS†	TOTAL DELAYS ±5% or ±2 nS†	PART NUMBER	TAP DELAYS ±5% or ±2 nS†	TOTAL DELAYS ±5% or ±2 nS†	PART NUMBER
*3±1, 1±.5, 2±.5, 3±.5	4	EPA1145-4	35, 70, 105, 140	175	EPA1145-175
*3±1, 1.5±.5, 3±.5, 4.5±.5	6	EPA1145-6	40, 80, 120, 160	200	EPA1145-200
*3±1, 2±.5, 4±.5, 6±.5	8	EPA1145-8	45, 90, 135, 180	225	EPA1145-225
*3±1, 6±1.5, 9, 12	15	EPA1145-15	50, 100, 150, 200	250	EPA1145-250
4, 8, 12, 16	20	EPA1145-20	60, 120, 180, 240	300	EPA1145-300
5, 10, 15, 20	25	EPA1145-25	70, 140, 210, 280	350	EPA1145-350
6, 12, 18, 24	30	EPA1145-30	80, 160, 240, 320	400	EPA1145-400
8, 16, 24, 32	40	EPA1145-40	90, 180, 270, 360	450	EPA1145-450
10, 20, 30, 40	50	EPA1145-50	100, 200, 300, 400	500	EPA1145-500
12, 24, 36, 48	60	EPA1145-60	120, 240, 360, 480	600	EPA1145-600
15, 30, 45, 60	75	EPA1145-75	140, 280, 420, 560	700	EPA1145-700
20, 40, 60, 80	100	EPA1145-100	160, 320, 480, 640	800	EPA1145-800
25, 50, 75, 100	125	EPA1145-125	180, 360, 540, 720	900	EPA1145-900
30, 60, 90, 120	150	EPA1145-150	200, 400, 600, 800	1000	EPA1145-1000

†Whichever is greater. Delay times referenced from input to leading edges at 25°C, 5.0V, with no load.

* First tap is inherent delay (3 ± 1 nS), all other taps are measured referenced from first tap.

DC Electrical Characteristics					
Parameter	Test Conditions	Min	Max	Unit	
V _{OH}	High-Level Output Voltage	V _{CC} = min. V _{IL} = max. I _{OH} = max	2.7		V
V _{OL}	Low-Level Output Voltage	V _{CC} = min. V _{IH} = min. I _{OL} = max	0.5		V
V _{IK}	Input Clamp Voltage	V _{CC} = min. I _I = I _{IK}	-1.2		V
I _{IH}	High-Level Input Current	V _{CC} = max. V _{IN} = 2.7V	50		µA
		V _{CC} = max. V _{IN} = 5.25V	1.0		mA
I _{IL}	Low-Level Input Current	V _{CC} = max. V _{IN} = 0.5V	-0.6		mA
I _{OS}	Short Circuit Output Current	V _{CC} = max. V _{OUT} = 0. (One output at a time)	-40		mA
I _{CC}	High-Level Supply Current	V _{CC} = max. V _{IN} = OPEN	15		mA
I _{CL}	Low-Level Supply Current	V _{CC} = max. V _{IN} = 0	50		mA
T _{RO}	Output Rise Time	T _d ≤ 500 nS (0.75 to 2.4 Volts)	3		nS
		T _d > 500 nS	3		nS
N _H	Fanout High-Level Output	V _{CC} = max. V _{OH} = 2.7V	20		TTL LOAD
N _L	Fanout Low-Level Output	V _{CC} = max. V _{OL} = 0.5V	10		TTL LOAD

Schematic



Recommended Operating Conditions		Min	Max	Unit
V _{CC}	Supply Voltage	4.75	5.25	V
V _{IH}	High-Level Input Voltage	2.0		V
V _{IL}	Low-Level Input Voltage		0.8	V
I _{IK}	Input Clamp Current		-18	mA
I _{OH}	High-Level Output Current		-1.0	mA
I _{OL}	Low-Level Output Current		20	mA
PW*	Pulse Width of Total Delay	40		%
d*	Duty Cycle		40	%
T _A	Operating Free-Air Temperature	-55	+125	°C

*These two values are inter-dependent.

Input Pulse Test Conditions @ 25° C			Unit
E _{IN}	Pulse Input Voltage	3.2	Volts
PW	Pulse Width % of Total Delay	110	%
T _{RI}	Pulse Rise Time (0.75 - 2.4 Volts)	2.0	nS
P _{RR}	Pulse Repetition Rate @ T _d ≤ 200 nS	1.0	MHz
	Pulse Repetition Rate @ T _d > 200 nS	100	KHz
V _{CC}	Supply Voltage	5.0	Volts

Package Dimensions

