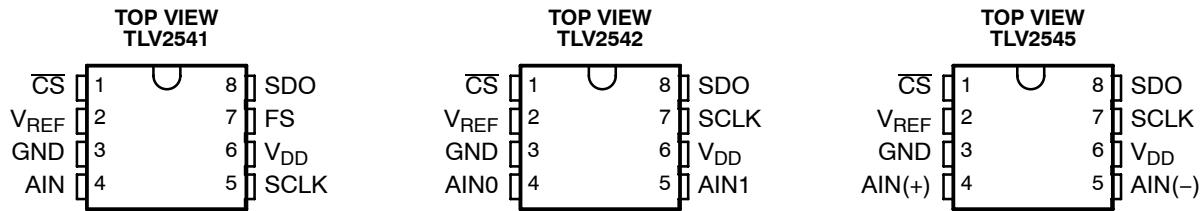


TLV2541, TLV2542, TLV2545
2.7-V TO 5.5-V, LOW-POWER, 12-BIT, 140/200 KSPS,
SERIAL ANALOG-TO-DIGITAL CONVERTERS WITH AUTOPOWER DOWN

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- Maximum Throughput . . . 140/200 KSPS
- Built-In Conversion Clock
- INL/DNL: ± 1 LSB Max, SINAD: 72 dB, SFDR: 85 dB, $f_i = 20$ kHz
- SPI/DSP-Compatible Serial Interface
- Single Supply: 2.7 Vdc to 5.5 Vdc
- Rail-to-Rail Analog Input With 500 kHz BW
- Three Options Available:
 - TLV2541: Single Channel Input
 - TLV2542: Dual Channels With Autosweep
 - TLV2545: Single Channel With Pseudo-Differential Input
- Low Power With Autopower Down
 - Operating Current: 1 mA at 2.7 V, 1.5 mA at 5 V
 - Autopower Down: 2 μ A at 2.7 V, 5 μ A at 5 V
- Small 8-Pin MSOP and SOIC Packages



description

The TLV2541, TLV2542, and TLV2545 are a family of high performance, 12-bit, low power, miniature, CMOS analog-to-digital converters (ADC). The TLV254x family operates from a single 2.7-V to 5.5-V supply. Devices are available with single, dual, or single pseudo-differential inputs. Each device has a chip select (\overline{CS}), serial clock (SCLK), and serial data output (SDO) that provides a direct 3-wire interface to the serial port of most popular host microprocessors (SPI interface). When interfaced with a TMS320™ DSP, a frame sync signal (FS) can be used to indicate the start of a serial data frame on \overline{CS} for all devices or FS for the TLV2541.

TLV2541, TLV2542, and TLV2545 are designed to operate with very low power consumption. The power saving feature is further enhanced with an autopower-down mode. This product family features a high-speed serial link to modern host processors with SCLK up to 20 MHz. The maximum SCLK frequency is dependent upon the mode of operation (see Table 1). The TLV254x family uses the built-in oscillator as the conversion clock, providing a 3.5- μ s conversion time.

AVAILABLE OPTIONS

| T _A | PACKAGED DEVICES | |
|----------------|-------------------|---------------|
| | 8-MSOP (DGK) | 8-SOIC (D) |
| 0°C to 70°C | TLV2541CDGK (AGZ) | |
| | TLV2542CDGK (AHB) | |
| | TLV2545CDGK (AHD) | |
| -40°C to 85°C | TLV2541IDGK (AHA) | TLV2541ID |
| | TLV2542IDGK (AHC) | TLV2542ID |
| | TLV2545IDGK (AHE) | TLV2545ID |



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TLV2541, TLV2542, TLV2545

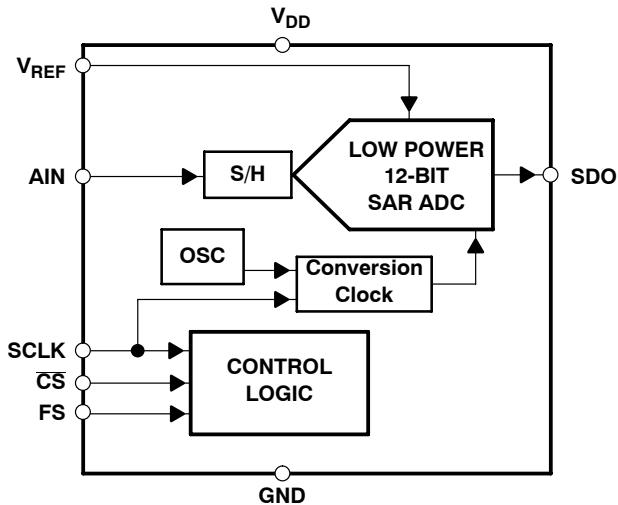
2.7-V TO 5.5-V, LOW-POWER, 12-BIT, 140/200 KSPS,

SERIAL ANALOG-TO-DIGITAL CONVERTERS WITH AUTOPOWER DOWN

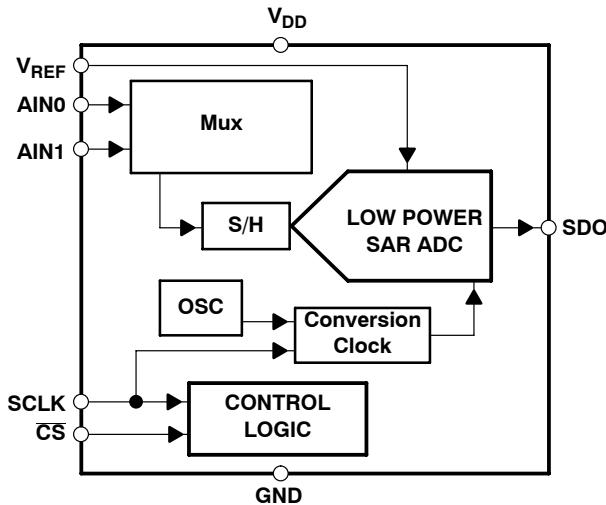
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functional block diagram

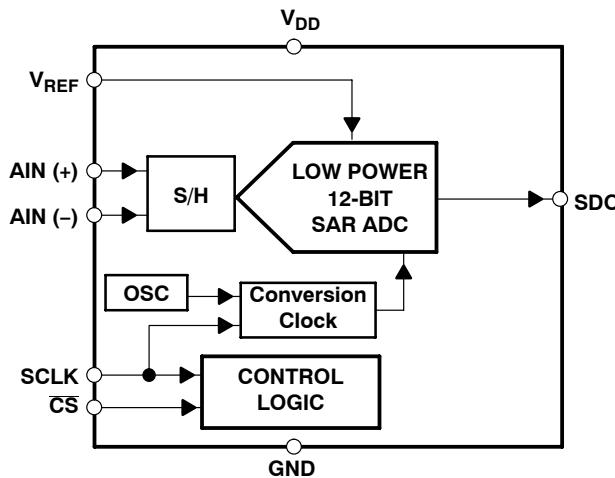
TLV2541



TLV2542



TLV2545



Terminal Functions

TLV2541

| TERMINAL | | I/O | DESCRIPTION |
|------------------|-----|-----|--|
| NAME | NO. | | |
| AIN | 4 | I | Analog input channel |
| CS | 1 | I | Chip select. A high-to-low transition on the CS input removes SDO from 3-state within a maximum setup time. CS can be used as the FS pin when a dedicated DSP serial port is used. |
| FS | 7 | I | DSP frame sync input. Indication of the start of a serial data frame. Tie this terminal to V _{DD} if not used. |
| GND | 3 | I | Ground return for the internal circuitry. Unless otherwise noted, all voltage measurements are with respect to GND. |
| SCLK | 5 | I | Output serial clock. This terminal receives the serial SCLK from the host processor. |
| SDO | 8 | O | The 3-state serial output for the A/D conversion result. SDO is kept in the high-impedance state until CS falling edge or FS rising edge, whichever occurs first. The output format is MSB first. When FS is not used (FS = 1 at the falling edge of CS): The MSB is presented to the SDO pin after CS falling edge and output data is valid on the first falling edge of SCLK. When CS and FS are both used (FS = 0 at the falling edge of CS): The MSB is presented to the SDO pin after the falling edge of CS. When CS is tied/held low, the MSB is presented on SDO after the rising FS. Output data is valid on the first falling edge of SCLK. (This is typically used with an active FS from a DSP using a dedicated serial port.) |
| V _{DD} | 6 | I | Positive supply voltage |
| V _{REF} | 2 | I | External reference input |

TLV2542/45

| TERMINAL | | I/O | DESCRIPTION |
|------------------|-----|-----|---|
| NAME | NO. | | |
| AIN0 /AIN(+) | 4 | I | Analog input channel 0 for TLV2542—Positive input for TLV2545. |
| AIN1/AIN (–) | 5 | I | Analog input channel 1 for TLV2542—Inverted input for TLV2545. |
| CS | 1 | I | Chip select. A high-to-low transition on CS removes SDO from 3-state within a maximum delay time. This pin can be connected to the frame sync of a DSP using a dedicated serial port. |
| GND | 3 | I | Ground return for the internal circuitry. Unless otherwise noted, all voltage measurements are with respect to GND. |
| SCLK | 7 | I | Output serial clock. This terminal receives the serial SCLK from the host processor. |
| SDO | 8 | O | The 3-state serial output for the A/D conversion result. SDO is kept in the high-impedance state when CS is high and presents output data after the CS falling edge until the LSB is presented. The output format is MSB first. SDO returns to the Hi-Z state after the 16th SCLK. Output data is valid on the falling SCLK edge. |
| V _{DD} | 6 | I | Positive supply voltage |
| V _{REF} | 2 | I | External reference input |

detailed description

The TLV2541, TLV2542, and TLV2545 are successive approximation (SAR) ADCs utilizing a charge redistribution DAC. Figure 1 shows a simplified version of the ADC.

The sampling capacitor acquires the signal on AIN during the sampling period. When the conversion process starts, the SAR control logic and charge redistribution DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator into a balanced condition. When the comparator is balanced, the conversion is complete and the ADC output code is generated.

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detailed description (continued)

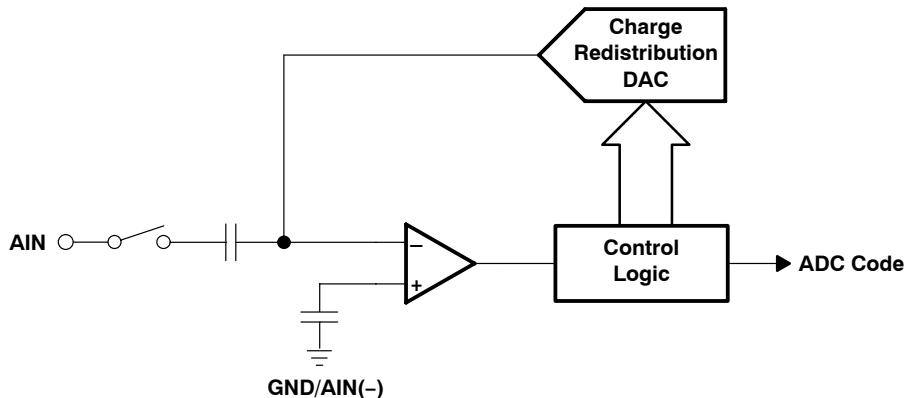


Figure 1. Simplified SAR Circuit

serial interface

| OUTPUT DATA FORMAT | |
|------------------------------|------------|
| MSB | LSB |
| D15-D4 | D3-D0 |
| Conversion result (OD11-OD0) | Don't care |

The output data format is binary (unipolar straight binary).

binary

Zero-scale code = 000h, Vcode = GND
Full-scale code = FFFh, Vcode = $V_{REF} - 1$ LSB

pseudo-differential inputs

The TLV2545 operates in pseudo-differential mode. The inverted input is available on pin 5. It can have a maximum input ripple of ± 0.2 V. This is normally used for ground noise rejection.

control and timing

start of the cycle

Each cycle may be started by either \overline{CS} , FS, or a combination of both. The internal state machine requires one SCLK high-to-low transition to determine the state of these control signals so internal blocks can be powered up in an active cycle. Special care to SPI mode is necessary. Make sure there is at least one SCLK whenever \overline{CS} (pin 1) is high to ensure proper operation.

TLV2541

- Control via \overline{CS} (FS = 1 at the falling edge of \overline{CS})—The falling edge of \overline{CS} is the start of the cycle. The MSB should be read on the first falling SCLK edge after \overline{CS} is low. Output data changes on the rising edge of SCLK. This is typically used for a microcontroller with an SPI interface, although it can also be used for a DSP. The microcontroller SPI interface should be programmed for CPOL = 0 (serial clock referenced to ground) and CPHA = 1 (data is valid on the falling edge of the serial clock). At least one falling edge transition on SCLK is needed whenever \overline{CS} is brought high.
- Control via FS (\overline{CS} is tied/held low)—The MSB is presented after the rising edge of FS. The falling edge of FS is the start of the cycle. The MSB should be read on the first falling edge of SCLK after FS is low. This is the typical configuration when the ADC is the only device on the DSP serial port.

control and timing (continued)

- Control via both \overline{CS} and FS—The MSB is presented after the falling edge of \overline{CS} . The falling edge of FS is the start of the sampling cycle. The MSB should be read on the first falling SCLK edge after FS is low. Output data changes on the rising edge of SCLK. This configuration is typically used for multiple devices connected to a TMS320 DSP.

TLV2542/5

All control is provided using \overline{CS} (pin 1) on the TLV2542 and TLV2545. The cycle is started on the falling edge transition provided by either a \overline{CS} signal from an SPI microcontroller or FS signal from a TMS320 DSP. Timing is similar to the TLV2541, with control via \overline{CS} only.

TLV2542 channel MUX reset cycle

The TLV2542 uses \overline{CS} to reset the analog input multiplexer. A short active \overline{CS} cycle (4 to 7 SCLKs) resets the MUX to AIN0. When the \overline{CS} cycle time is greater than 7 SCLKs in duration, as in the case for a complete conversion cycle (\overline{CS} is low for 16 SCLKs plus maximum conversion time), the MUX toggles to the next channel (see Figure 4 for timing). One dummy conversion cycle is recommended after power up before attempting to reset the MUX.

sampling

The converter sample time is 12 SCLKs in duration, beginning on the fifth SCLK received after the converter has received a high-to-low \overline{CS} transition (or a high-to-low FS transition for the TLV2541).

conversion

The TLV2541, TLV2542, and TLV2545 complete conversions in the following manner. The conversion is started after the 16th SCLK falling edge and takes $3.5\ \mu s$ to complete. Enough time (for conversion) should be allowed before a rising \overline{CS} or FS edge so that no conversion is terminated prematurely.

TLV2542 input channel selection is toggled on each rising \overline{CS} edge. The MUX channel can be reset to AIN0 via \overline{CS} as described in the earlier section and in Figure 4. The input is sampled for 12 SCLKs, converted, and the result is presented on SDO during the next cycle. Care should also be taken to allow enough time between samples to avoid prematurely terminating the cycle, which occurs on a rising \overline{CS} transition if the conversion is not complete.

The SDO data presented during a cycle is the result of the conversion of the sample taken during the previous cycle.

timing diagrams/conversion cycles

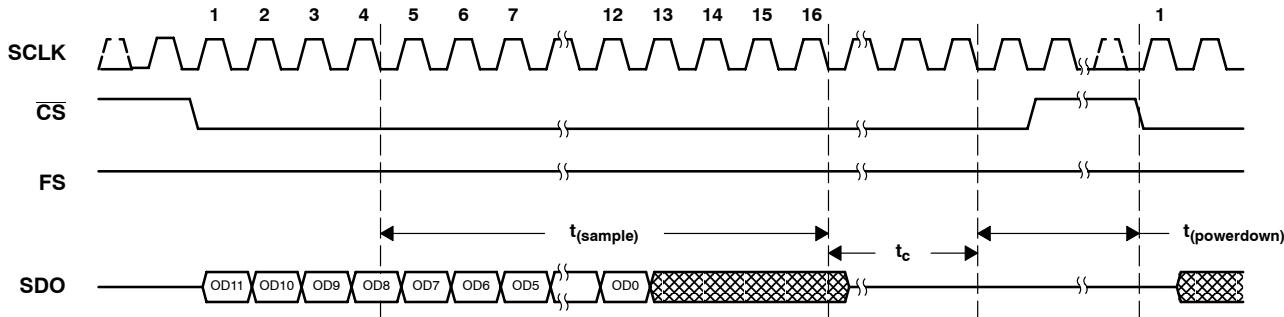


Figure 2. TLV2541 Timing: Control via \overline{CS} (FS = 1)

timing diagrams/conversion cycles (continued)

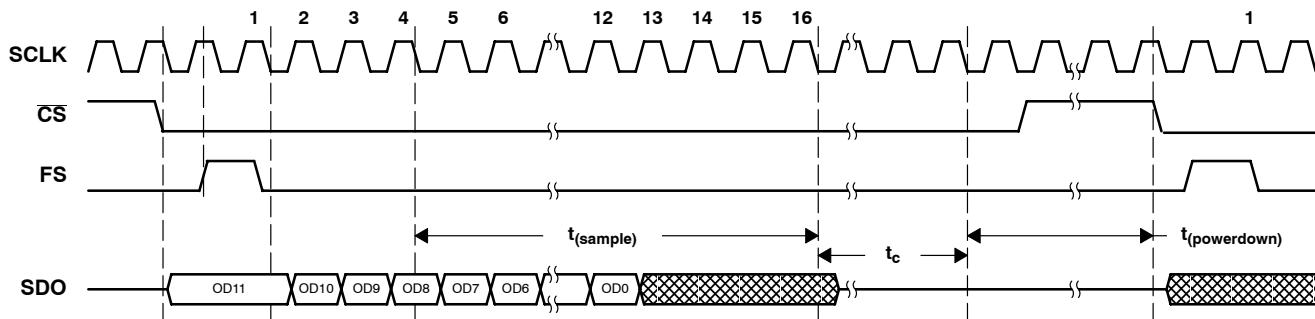
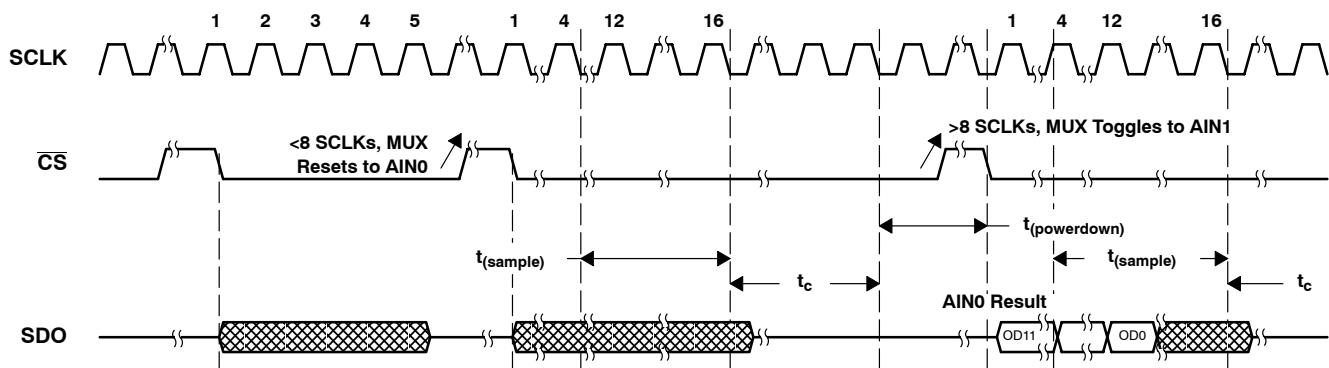
Figure 3. TLV2541 Timing: Control via \overline{CS} and FS or FS Only

Figure 4. TLV2542 Reset Timing

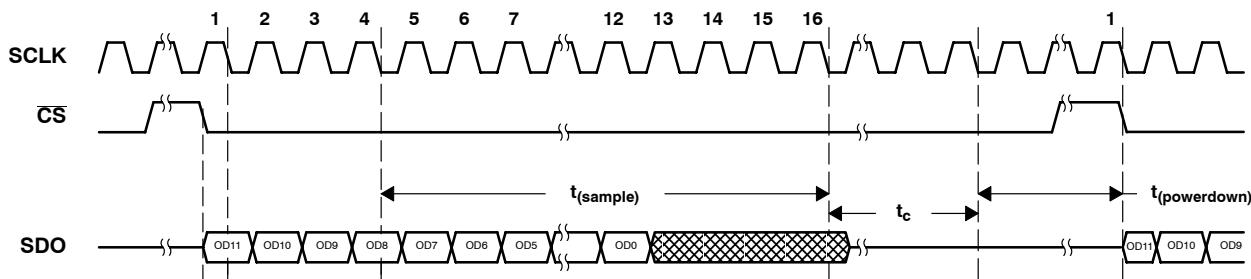


Figure 5. TLV2542 and TLV2545 Timing

using \overline{CS} as the FS input

When interfacing the TLV2541 with the TMS320 DSP, the FSR signal from the DSP may be connected to the \overline{CS} input if this is the only device on the serial port. This saves one output terminal from the DSP. (Output data changes on the falling edge of SCLK. This is the default configuration for the TLV2542 and TLV2545.)

using \overline{CS} as the FS input (continued)

SCLK and conversion speed

The input frequency of SCLK can range from 100 kHz to 20 MHz maximum. The ADC conversion uses a separate internal oscillator with a minimum frequency of 4 MHz. The conversion cycle takes 14 internal oscillator clocks to complete. This leads to a 3.5- μ s conversion time. For a 20-MHz SCLK, the minimum total cycle time is given by: $16x(1/20M)+14x(1/4M)+\text{one SCLK} = 4.35 \mu\text{s}$. An additional SCLK is added to account for the required \overline{CS} and/or FS high time. These times specify the minimum cycle time for an active \overline{CS} or FS signal. If violated, the conversion terminates, invalidating the next data output cycle. Table 1 gives the maximum SCLK frequency for a given supply voltage and operational mode.

control via pin 1 (\overline{CS} , SPI interface)

All devices are compatible with this mode operation. A falling \overline{CS} initiates the cycle (for TLV2541, the FS input is tied to V_{DD}). \overline{CS} remains low for the entire cycle time (sample+convert+one SCLK) and can then be released.

NOTE:

IMPORTANT: A single SCLK is required whenever \overline{CS} is high.

control via pin 1 (\overline{CS} , DSP interface)

All devices are compatible with this mode of operation. The FS signal from a DSP is connected directly to the \overline{CS} input of the ADC. A falling edge on the \overline{CS} input initiates the cycle. (For the TLV2541, the FS input can be tied to V_{DD} , although better performance can be achieved when using the FS input for control. Refer to the next section.) The \overline{CS} input should remain low for the entire cycle time (sample+convert+one SCLK) and can then be released.

NOTE:

IMPORTANT: A single SCLK is required whenever \overline{CS} is high. This should be of little consequence, since SCLK is normally always present when interfacing with a DSP.

control via pin 1 and pin 7 (\overline{CS} and FS or FS only, DSP interface)

Only the TLV2541 is compatible with this mode of operation. The \overline{CS} input to the ADC can be controlled via a general-purpose I/O pin from the DSP. The FS signal from the DSP is connected directly to the FS input of the ADC. A falling edge on \overline{CS} , if used, releases the MSB on the SDO output. When \overline{CS} is not used, the rising FS edge releases the MSB. The falling edge on the FS input while SCLK is high initiates the cycle. The \overline{CS} and FS inputs should remain low for the entire cycle time (sample+convert+one SCLK) and can then be released.

reference voltage

An external reference is applied via V_{REF} . The voltage level applied to this pin establishes the upper limit of the analog inputs to produce a full-scale reading. The value of V_{REF} and the analog input should not exceed the positive supply or be less than GND, consistent with the specified absolute maximum ratings. The digital output is at full scale when the input signal is equal to or higher than V_{REF} and at zero when the input signal is equal to or lower than GND.

power down and power up

Autopower down is built into these devices in order to reduce power consumption. The actual power savings depends on the inactive time between cycles and the power supply (loading) decoupling/storage capacitors. *Power-down takes effect immediately after the conversion is complete.* This is fast enough to provide some power savings between cycles with longer than 1 SCLK inactive time. *The device power goes down to 5 μ A within 0.5 μ s.* To achieve the lowest power-down current (*deep powerdown*) of 1 μ A requires 2-ms inactive time between cycles. The power-down state is initiated at the end of conversion. These devices wake up *immediately* at the next falling edge of \overline{CS} or the rising edge of FS.

TLV2541, TLV2542, TLV2545 2.7-V TO 5.5-V, LOW-POWER, 12-BIT, 140/200 KSPS, SERIAL ANALOG-TO-DIGITAL CONVERTERS WITH AUTOPOWER DOWN

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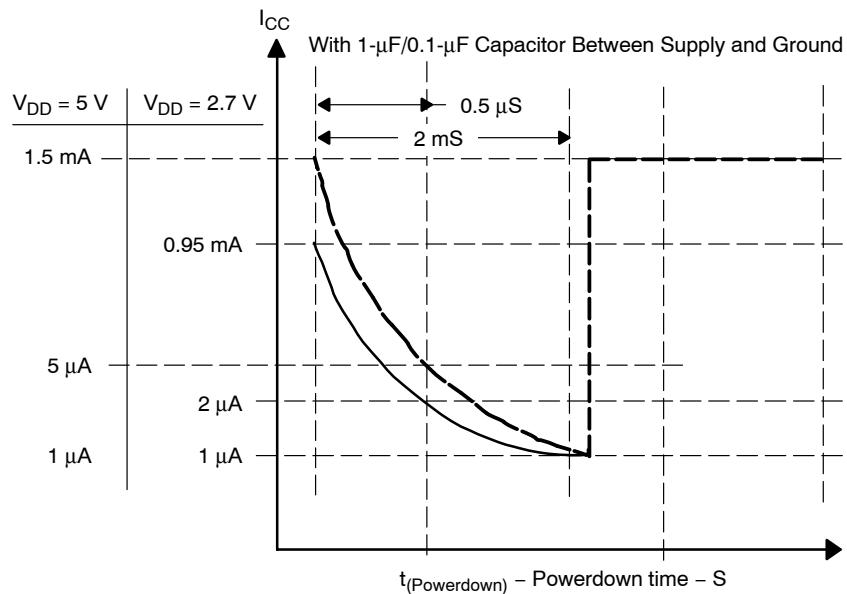


Table 1. Modes of Operation and Data Throughput

| CONTROL PIN(s)/DEVICE | MAX SCLK (MHz) (50/50 duty cycle) | | APPROXIMATE CONVERSION THROUGHPUT (ksps) | |
|---|--------------------------------------|-------------------------|---|-------------------------|
| | V _{DD} = 2.7 V | V _{DD} = 4.5 V | V _{DD} = 2.7 V | V _{DD} = 4.5 V |
| CS control only (TLV2541 only) | | | | |
| For SPI interface [†] | 10 | 15 | 175 | 200 |
| For DSP interface (Use CS as FS) [‡] | 5 | 8 | 140 | 175 |
| CS and FS control (TLV2541 only) [§] | | | | |
| DSP interface | 15 | 20 | 200 | 200 |

[†] See Figure 29(a).

[‡] See Figure 29(b).

§ See Figure 29(c).

absolute maximum ratings over operating free-air temperature (unless otherwise noted)¹

¹ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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SERIAL ANALOG-TO-DIGITAL CONVERTERS WITH AUTOPOWER DOWN

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recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---|--|-------|----------|--------------------|
| Supply voltage, V_{DD} | 2.7 | 3.3 | 5.5 | V |
| Positive external reference voltage input, V_{REFP} (see Note 1) | 2 | | V_{DD} | V |
| Analog input voltage (see Note 1) | 0 | | V_{DD} | V |
| High level control input voltage, V_{IH} | 2.1 | | | V |
| Low-level control input voltage, V_{IL} | | | 0.6 | V |
| Setup time, \bar{CS} falling edge before first SCLK falling edge, $t_{su}(CSL-SCLKL)$ | $V_{DD} = REF = 4.5\text{ V}$ | 40 | | ns |
| | $V_{DD} = REF = 2.7\text{ V}$ | 70 | | |
| Hold time, \bar{CS} falling edge after SCLK falling edge, $t_h(SCLKL-CSL)$ | | 5 | | ns |
| Delay time, delay from \bar{CS} falling edge to FS rising edge, $t_d(CSL-FSH)$ (TLV2541 only) | 0.5 | 7 | | SCLKs |
| Setup time, FS rising edge before SCLK falling edge, $t_{su}(FSH-SCLKL)$ (TLV2541 only) | 0.35 | | | SCLKs |
| Hold time, FS high after SCLK falling edge, $t_h(SCLKL-FSL)$ (TLV2541 only) | | 0.65 | | SCLKs |
| Pulse width \bar{CS} high time, $t_w(H_CS)$ | 100 | | | ns |
| Pulse width FS high time, $t_w(H_FS)$ (TLV2541 only) | 0.75 | | | SCLKs |
| SCLK cycle time, $V_{DD} = 3.6\text{ V}$ to 2.7 V , $t_c(SCLK)$ (maximum tolerance of 40/60 duty cycle) | 90 | 10000 | | ns |
| SCLK cycle time, $V_{DD} = 5.5\text{ V}$ to 4.5 V , $t_c(SCLK)$ (maximum tolerance of 40/60 duty cycle) | 50 | 10000 | | ns |
| Pulse width low time, $t_w(L_SCLK)$ | 0.4 | 0.6 | | SCLK |
| Pulse width high time, $t_w(H_SCLK)$ | 0.4 | 0.6 | | SCLK |
| Hold time, hold from end of conversion to \bar{CS} high, $t_h(EOC-CSH)$ (EOC is internal, indicates end of conversion time, t_c) | | 0.05 | | μs |
| Active \bar{CS} cycle time to reset internal MUX to AIN0, $t_{reset\ cycle}$ (TLV2542 only) | 4 | 7 | | SCLKs |
| Delay time, delay from \bar{CS} falling edge to SDO valid, $t_d(CSL-SDOV)$ | $V_{DD} = REF = 4.5\text{ V}$, 25-pF load | 40 | | ns |
| | $V_{DD} = REF = 2.7\text{ V}$, 25-pF load | 70 | | |
| Delay time, delay from FS falling edge to SDO valid, $t_d(FSL-SDOV)$ (TLV2541 only) | $V_{DD} = REF = 4.5\text{ V}$, 25-pF load | 1 | | ns |
| | $V_{DD} = REF = 2.7\text{ V}$, 25-pF load | 1 | | |
| Delay time, delay from SCLK rising edge to SDO valid, $t_d(SCLKH-SDOV)$ | $V_{DD} = REF = 4.5\text{ V}$, 25-pF load | 11 | | ns |
| | $V_{DD} = REF = 2.7\text{ V}$, 25-pF load | 21 | | |
| Delay time, delay from 17th SCLK rising edge to SDO 3-state, $t_d(SCLK17H-SDOZ)$ | $V_{DD} = REF = 4.5\text{ V}$, 25-pF load | 30 | | ns |
| | $V_{DD} = REF = 2.7\text{ V}$, 25-pF load | 60 | | |
| Conversion time, t_c | Conversion clock = internal oscillator | 2.1 | 2.6 | μs |
| Sampling time, $t_{(sample)}$ | See Note 2 | 300 | | ns |
| Operating free-air temperature, T_A | TLV2541/2/5C | 0 | 70 | $^{\circ}\text{C}$ |
| | TLV2541/2/5I | -40 | 85 | |

NOTES: 1. Analog input voltages greater than that applied to V_{REF} convert as all ones (111111111111), while input voltages less than that applied to GND convert as all zeros(000000000000).
2. Minimal $t_{(sample)}$ is given by $0.9 \times 50\text{ pF} \times (R_S + 0.5\text{ k}\Omega)$, where R_S is the source output impedance.



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electrical characteristics over recommended operating free-air temperature range,

 $V_{DD} = V_{REF} = 2.7 \text{ V to } 5.5 \text{ V}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP [†] | MAX | UNIT | |
|--|---|---|--|-------|------------------|----------------|---------------|--|
| V_{OH} | High-level output voltage | $V_{DD} = 5.5 \text{ V}, I_{OH} = -0.2 \text{ mA}$ at 30-pF load | | 2.4 | | $V_{DD} - 0.2$ | V | |
| | | $V_{DD} = 2.7 \text{ V}, I_{OH} = -20 \mu\text{A}$ at 30-pF load | | | | | | |
| V_{OL} | Low-level output voltage | $V_{DD} = 5.5 \text{ V}, I_{OL} = 0.8 \text{ mA}$ at 30-pF load | | 0.4 | | 0.1 | V | |
| | | $V_{DD} = 2.7 \text{ V}, I_{OL} = 20 \mu\text{A}$ at 30-pF load | | | | | | |
| I_{OZ} | Off-state output current (high-impedance-state) | $V_O = V_{DD}$ | $CS = V_{DD}$ | 1 | | 2.5 | μA | |
| | | $V_O = 0$ | | -1 | | -2.5 | | |
| I_{IH} | High-level input current | $V_I = V_{DD}$ | | 0.005 | | 2.5 | μA | |
| I_{IL} | Low-level input current | $V_I = 0 \text{ V}$ | | -0.00 | | 5 | μA | |
| I_{CC} | Operating supply current | CS at 0 V | $V_{DD} = 4.5 \text{ V to } 5.5 \text{ V}$ | 1.3 | | 1.5 | mA | |
| | | | $V_{DD} = 2.7 \text{ V to } 3.3 \text{ V}$ | 0.85 | | 0.95 | | |
| $I_{CC(\text{AUTOPWDN})}$ | Autopower-down current $t_{(\text{powerdown})} \geq 0.5 \mu\text{s}$ | For all digital inputs, $0 \leq V_I \leq 0.3 \text{ V}$ or $V_I \geq V_{DD} - 0.3 \text{ V}$, $SCLK = 0, V_{DD} = 4.5 \text{ V to } 5.5 \text{ V}$, Ext ref | | 5 | | μA | | |
| | | $V_{DD} = 2.7 \text{ V to } 3.3 \text{ V}$, Ext ref | | 2 | | | | |
| | Deep autopower-down current $t_{(\text{powerdown})} \geq 2 \text{ ms}$ | For all digital inputs, $0 \leq V_I \leq 0.3 \text{ V}$ or $V_I \geq V_{DD} - 0.3 \text{ V}$, $SCLK = 0, V_{DD} = 4.5 \text{ V to } 5.5 \text{ V}$, Ext ref | | 1 | | μA | | |
| | | $V_{DD} = 2.7 \text{ V to } 3.3 \text{ V}$ | | 1 | | | | |
| Selected analog input channel leakage current | | Selected channel at V_{DD} | | 1 | | μA | | |
| | | Selected channel at 0 V | | -1 | | | | |
| C_i | Input capacitance | Analog inputs | | 20 | 45 | 50 | pF | |
| | | Control Inputs | | 5 | | 25 | | |
| Input on resistance | | $V_{DD} = 5.5 \text{ V}$ | | 500 | | Ω | | |
| | | $V_{DD} = 2.7 \text{ V}$ | | 600 | | | | |
| Autopower down | | | | 0.5 | | SCLK | | |

[†] All typical values are at $V_{DD} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

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SLAS245E –MARCH 2000 – REVISED APRIL 2010

ac specifications ($f_i = 20$ kHz)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------|-----------------------------------|--------------------------------------|-----|------|-----|------|
| SINAD | Signal-to-noise ratio +distortion | 200 KSPS, $V_{DD} = V_{REF} = 5.5$ V | 70 | 72 | | dB |
| | | 150 KSPS, $V_{DD} = V_{REF} = 2.7$ V | 68 | 71 | | |
| THD | Total harmonic distortion | 200 KSPS, $V_{DD} = V_{REF} = 5.5$ V | | -84 | -80 | dB |
| | | 150 KSPS, $V_{DD} = V_{REF} = 2.7$ V | | -84 | -80 | |
| ENOB | Effective number of bits | 200 KSPS, $V_{DD} = V_{REF} = 5.5$ V | | 11.8 | | Bits |
| | | 150 KSPS, $V_{DD} = V_{REF} = 2.7$ V | | 11.6 | | |
| SFDR | Spurious free dynamic range | 200 KSPS, $V_{DD} = V_{REF} = 5.5$ V | | -84 | -80 | dB |
| | | 150 KSPS, $V_{DD} = V_{REF} = 2.7$ V | | -84 | -80 | |
| Analog Input | | | | | | |
| Full-power bandwidth, -3 dB | | | | 1 | | MHz |
| Full-power bandwidth, -1 dB | | | | 500 | | kHz |

external reference specifications

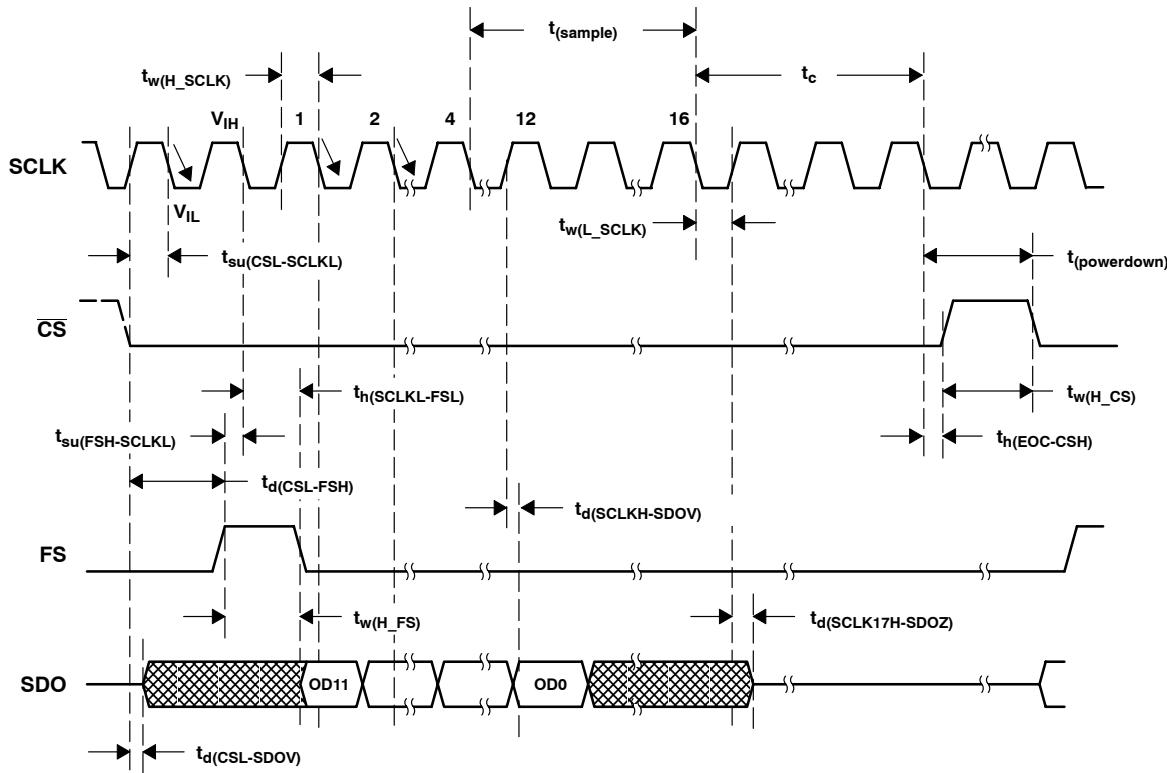
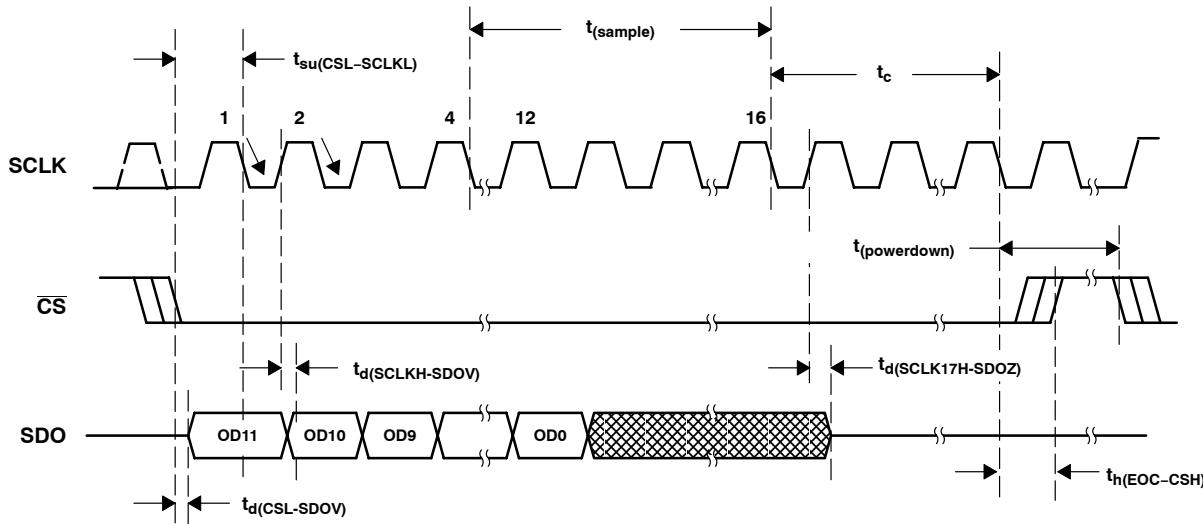
| PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|-----------------------------|-----------------------------|-------------------------------------|-----|-----|----------|-----------|
| Reference input voltage | $V_{DD} = 2.7$ V to 5.5 V | | 2 | | V_{DD} | V |
| Reference input impedance | $V_{DD} = 5.5$ V | $\overline{CS} = 1$, SCLK = 0 | 100 | | | $M\Omega$ |
| | | $\overline{CS} = 0$, SCLK = 20 MHz | 20 | 25 | | $k\Omega$ |
| | $V_{DD} = 2.7$ V | $\overline{CS} = 1$, SCLK = 0 | 100 | | | $M\Omega$ |
| | | $\overline{CS} = 0$, SCLK = 20 MHz | 20 | 25 | | $k\Omega$ |
| Reference current | $V_{DD} = V_{REF} = 5.5$ V, | $\overline{CS} = 0$, SCLK = 20 MHz | | 100 | 400 | μA |
| | $V_{DD} = V_{REF} = 2.7$ V, | $\overline{CS} = 0$, SCLK = 20 MHz | | 50 | 200 | |
| Reference input capacitance | $V_{DD} = V_{REF} = 5.5$ V | $\overline{CS} = 1$, SCLK = 0 | 5 | 15 | | pF |
| | | $\overline{CS} = 0$, SCLK = 20 MHz | 20 | 45 | 50 | |
| | $V_{DD} = V_{REF} = 2.7$ V | $\overline{CS} = 1$, SCLK = 0 | 5 | 15 | | |
| | | $\overline{CS} = 0$, SCLK = 20 MHz | 20 | 45 | 50 | |
| V_{REF} | Reference voltage | $V_{DD} = 2.7$ V to 5.5 V | | | V_{DD} | V |

dc specification, $V_{DD} = V_{REF} = 2.7$ V to 5.5 V, SCLK frequency = 20 MHz at 5 V, 15 MHz at 3 V (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|-----------|---------------------------------------|------------|------------|-----------|-----------|------|
| INL | Integral linearity error (see Note 4) | | | ± 0.6 | ± 1 | LSB |
| DNL | Differential linearity error | | See Note 3 | ± 0.5 | ± 1 | LSB |
| E_O | Offset error (see Note 5) | See Note 3 | TLV2541/42 | | ± 1.5 | LSB |
| | | | TLV2545 | | ± 2.5 | |
| E_G | Gain error (see Note 5) | See Note 3 | TLV2541/42 | | ± 2 | LSB |
| | | | TLV2545 | | ± 5 | |
| E_t | Total unadjusted error (see Note 6) | See Note 3 | TLV2541/42 | | ± 2 | LSB |
| | | | TLV2545 | | ± 5 | |

- NOTES: 3. Analog input voltages greater than that applied to V_{REF} convert as all ones (111111111111).
 4. Linear error is the maximum deviation from the best straight line through the A/D transfer characteristics.
 5. Zero error is the difference between 000000000000 and the converted output for zero input voltage: full-scale error is the difference between 111111111111 and the converted output for full-scale input voltage.
 6. Total unadjusted error comprises linearity, zero, and full-scale errors.

PARAMETER MEASUREMENT INFORMATION

Figure 6. TLV2541 Critical Timing (Control via \overline{CS} and FS or FS only)Figure 7. TLV2541 Critical Timing (Control via \overline{CS} only, FS = 1)

PARAMETER MEASUREMENT INFORMATION

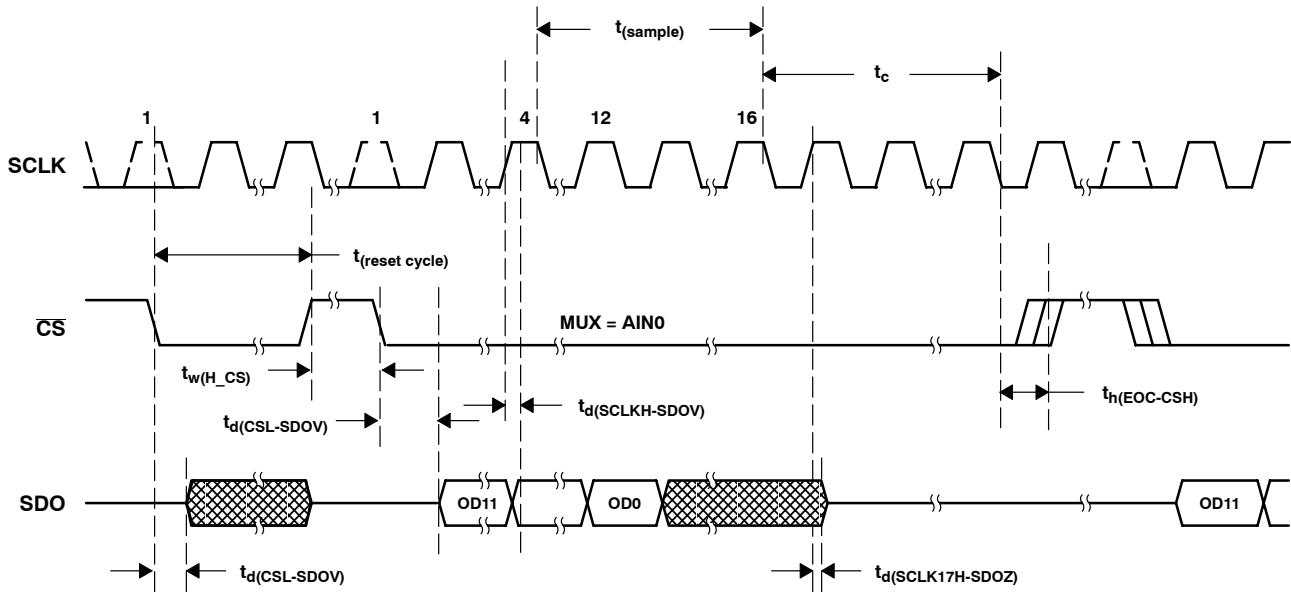


Figure 8. TLV2542 Reset Cycle Critical Timing

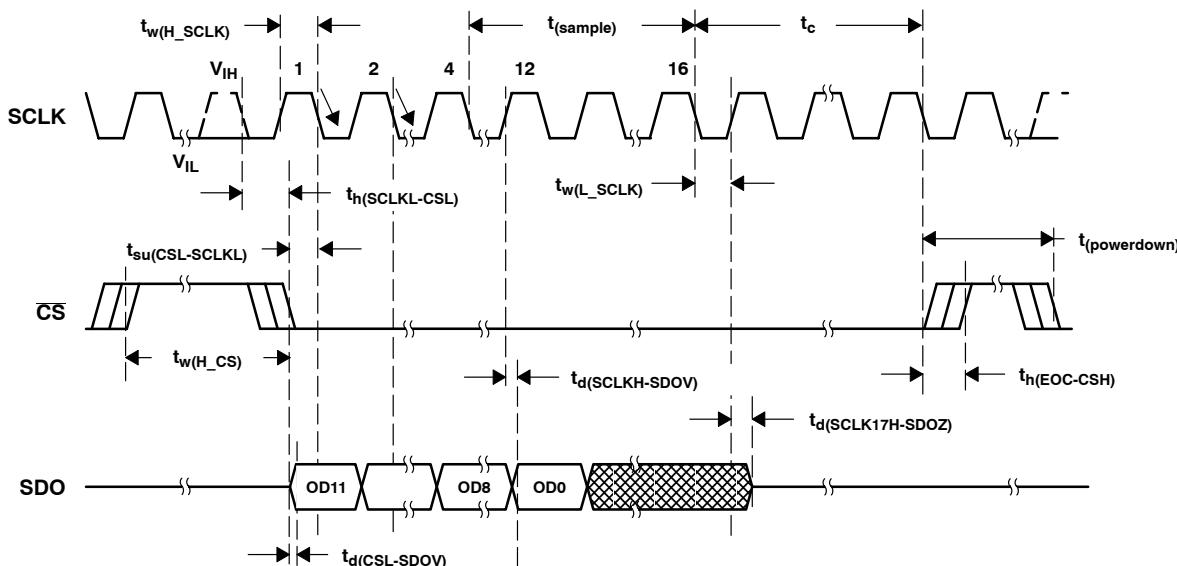


Figure 9. TLV2542 and TLV2545 Conversion Cycle Critical Timing

TYPICAL CHARACTERISTICS

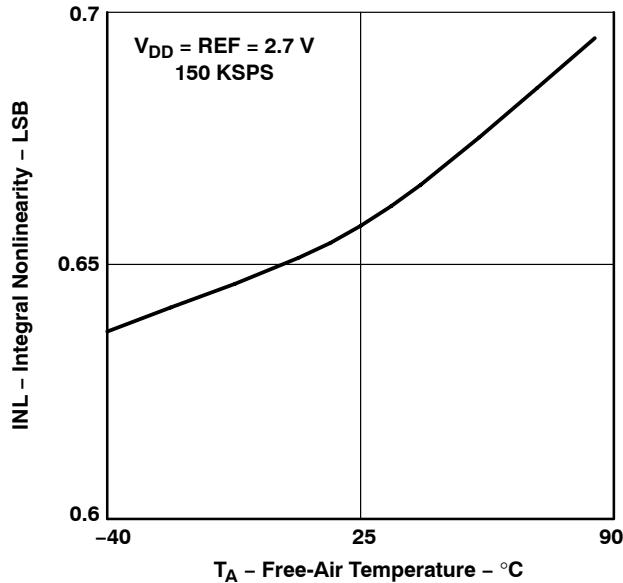
INTEGRAL NONLINEARITY
vs
FREE-AIR TEMPERATURE

Figure 10

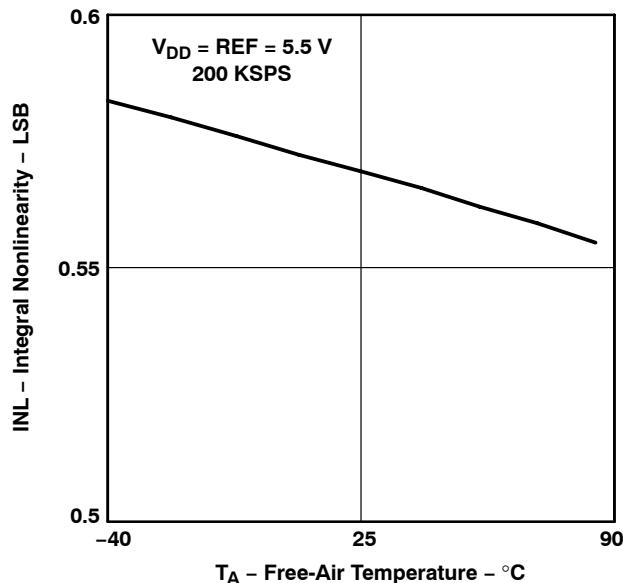
INTEGRAL NONLINEARITY
vs
FREE-AIR TEMPERATURE

Figure 11

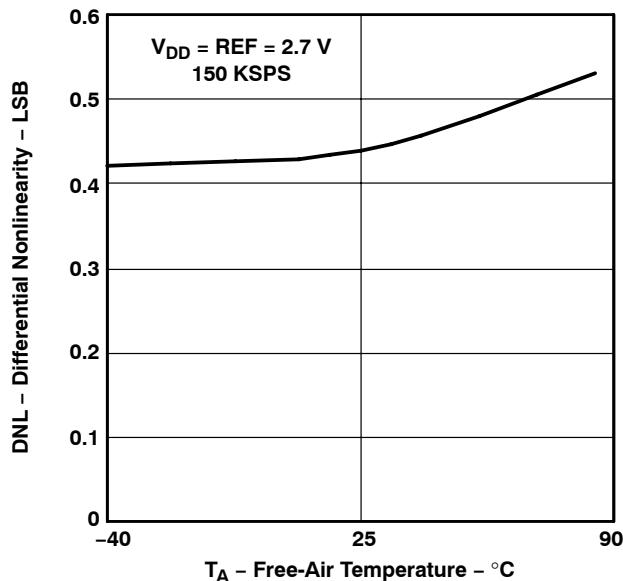
DIFFERENTIAL NONLINEARITY
vs
FREE-AIR TEMPERATURE

Figure 12

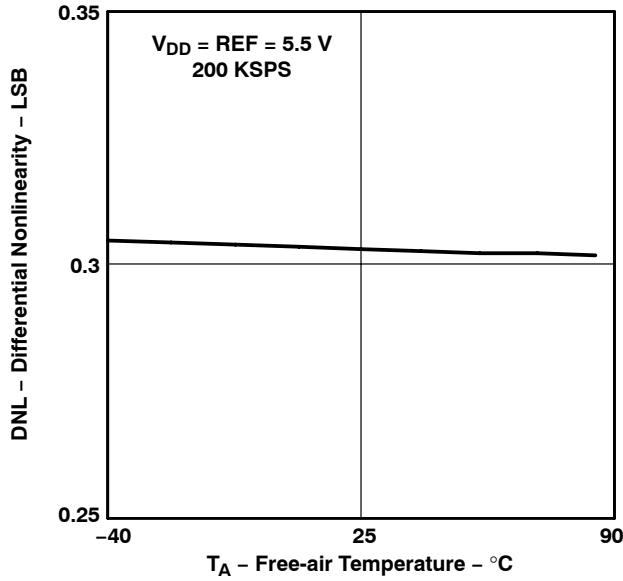
DIFFERENTIAL NONLINEARITY
vs
FREE-AIR TEMPERATURE

Figure 13

TYPICAL CHARACTERISTICS

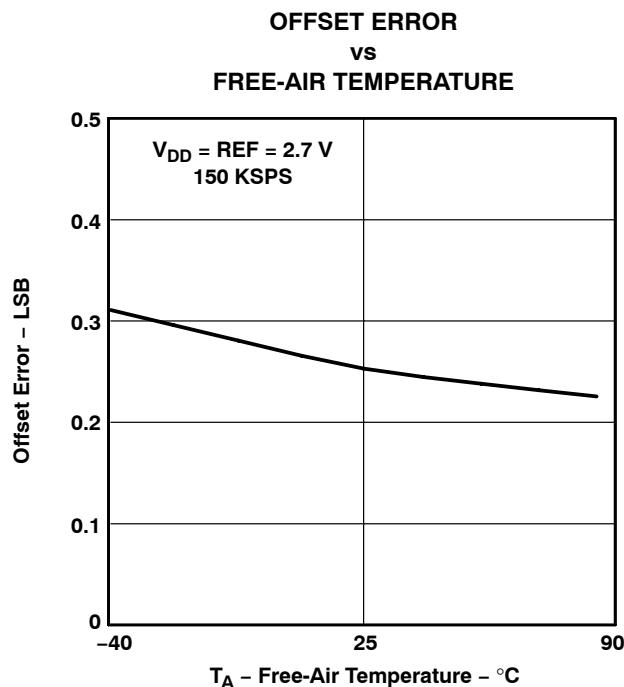


Figure 14

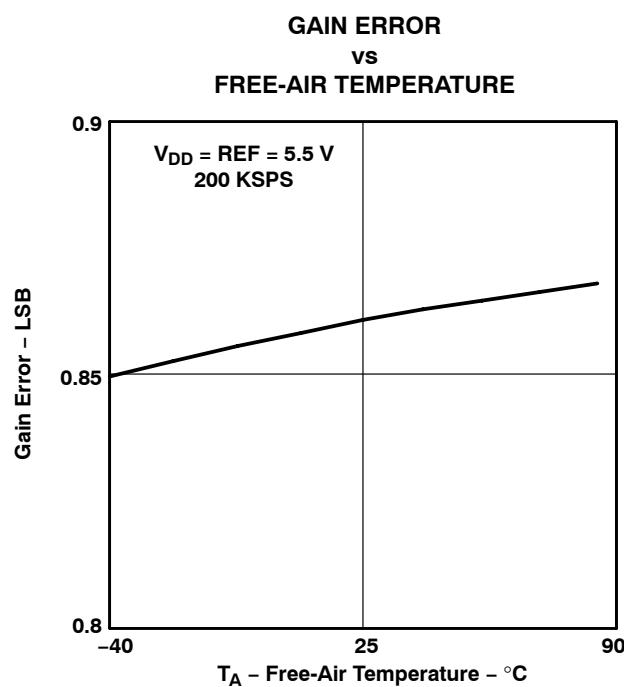


Figure 15

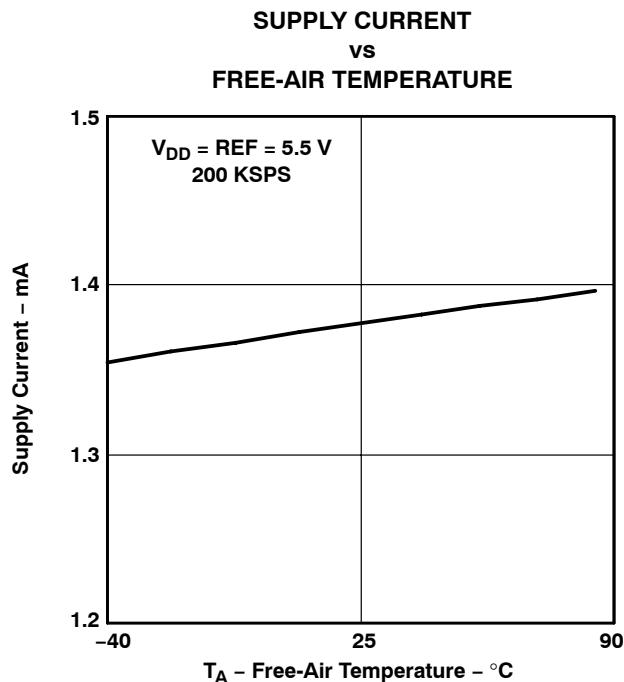


Figure 16

TYPICAL CHARACTERISTICS

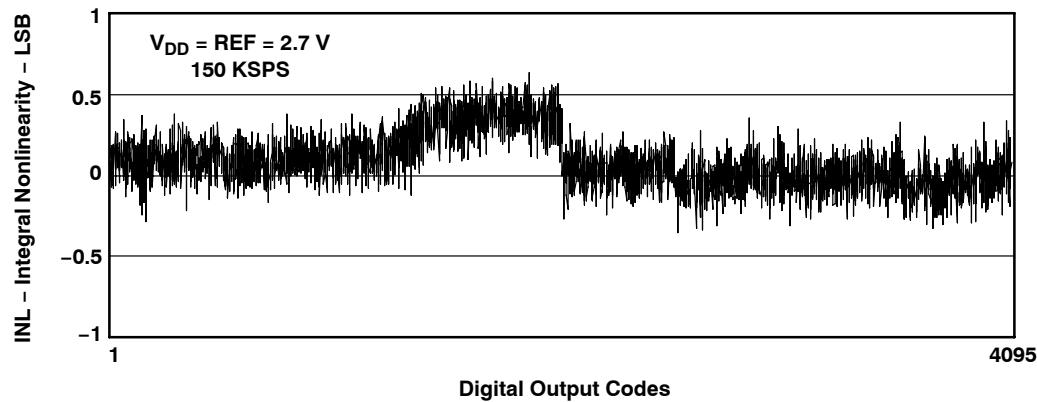
INTEGRAL NONLINEARITY ERROR
vs
DIGITAL OUTPUT CODES

Figure 17

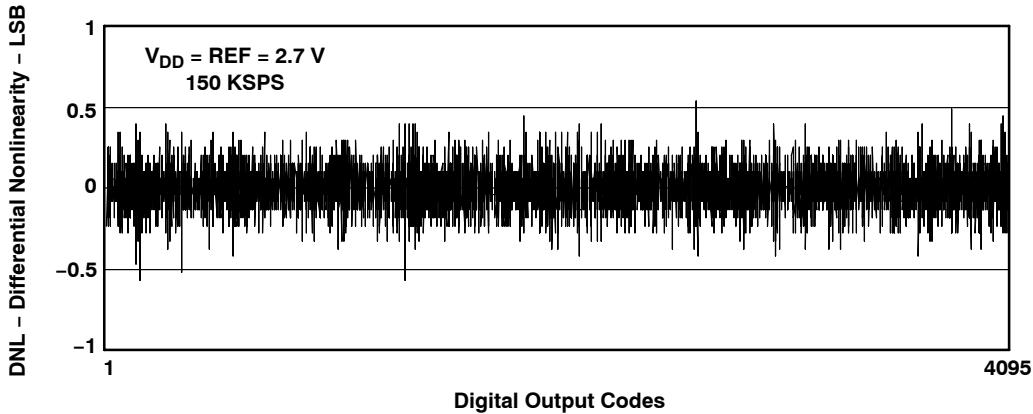
DIFFERENTIAL NONLINEARITY ERROR
vs
DIGITAL OUTPUT CODES

Figure 18

TYPICAL CHARACTERISTICS

INTEGRAL NONLINEARITY ERROR
vs
DIGITAL OUTPUT CODES

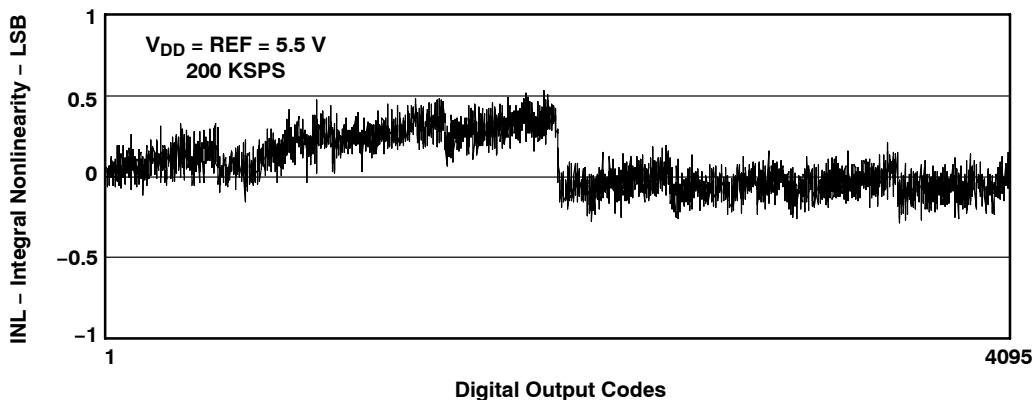


Figure 19

DIFFERENTIAL NONLINEARITY ERROR
vs
DIGITAL OUTPUT CODES

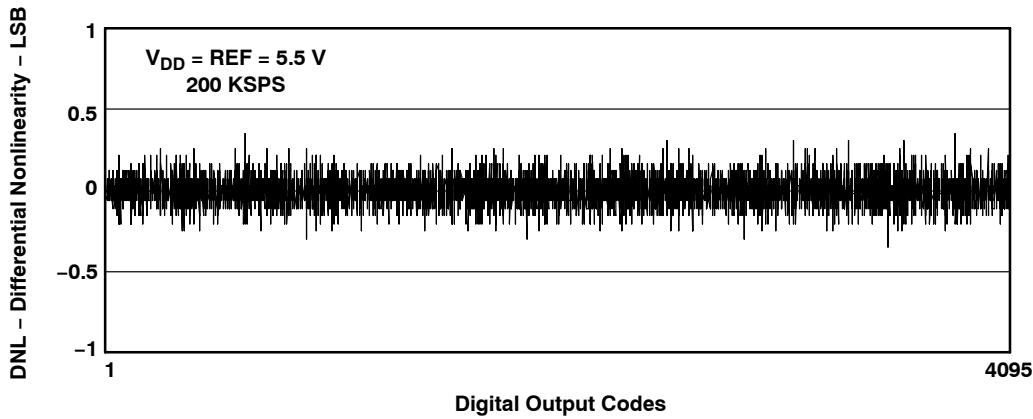


Figure 20

TYPICAL CHARACTERISTICS

2048 POINTS FAST FOURIER TRANSFORM (FFT)

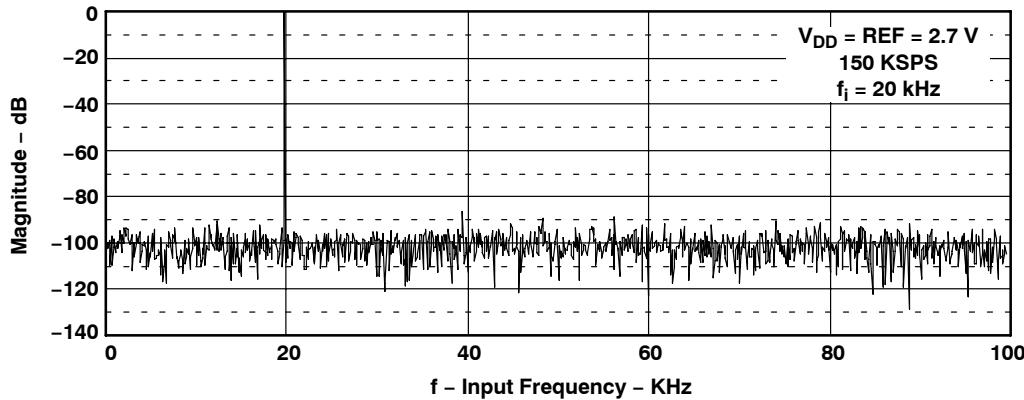


Figure 21

2048 POINTS FAST FOURIER TRANSFORM (FFT)

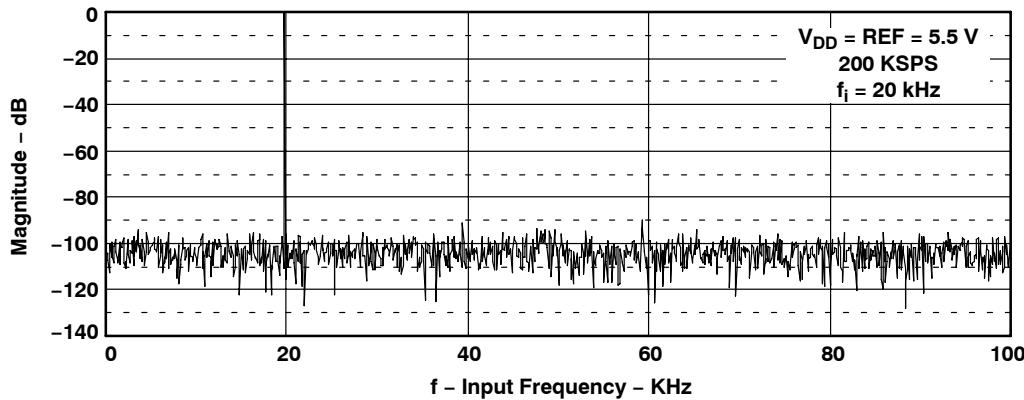


Figure 22

TYPICAL CHARACTERISTICS

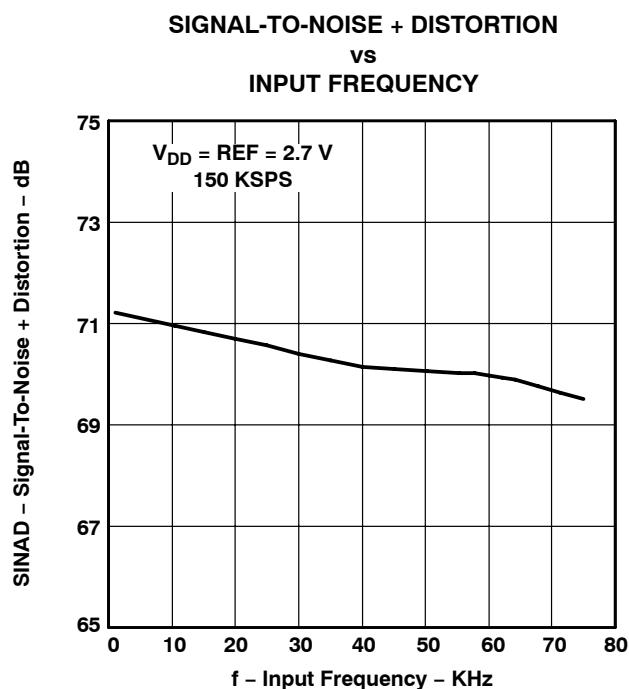


Figure 23

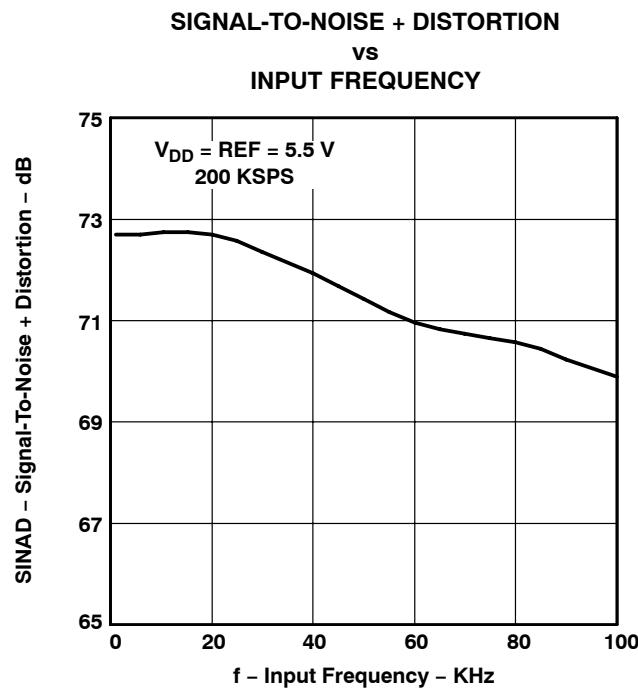


Figure 24

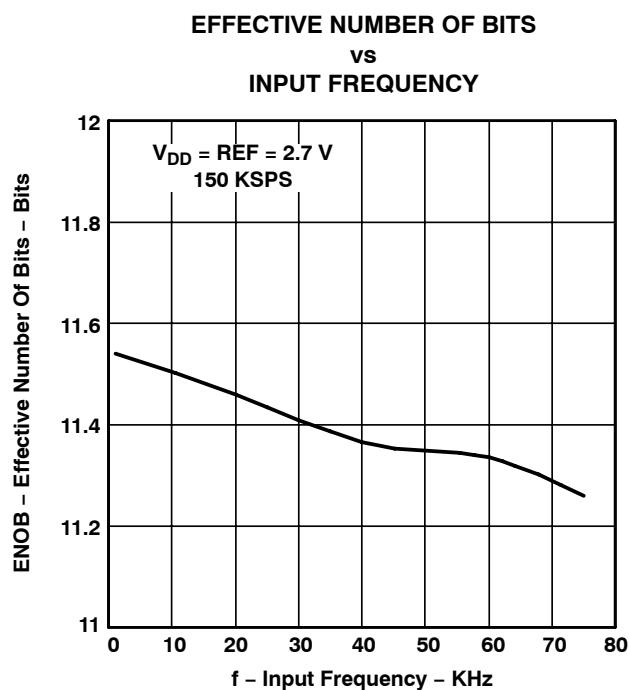


Figure 25

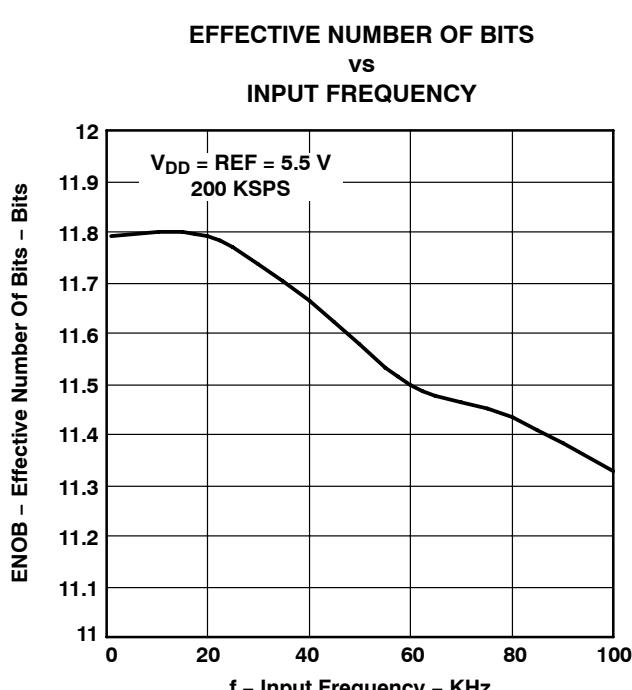


Figure 26

TYPICAL CHARACTERISTICS

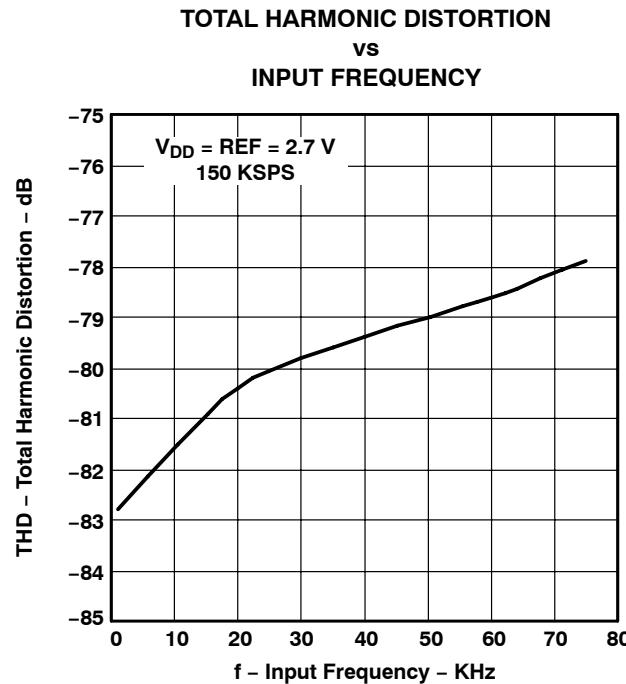


Figure 27

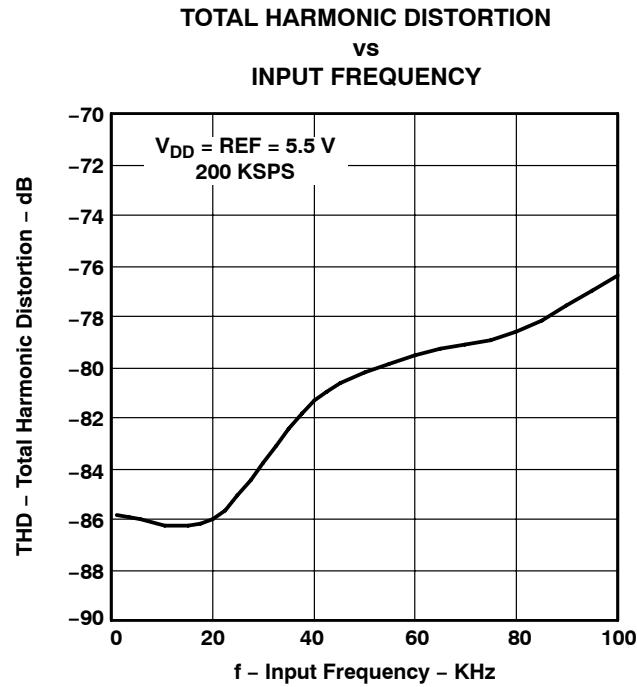


Figure 28

APPLICATION INFORMATION

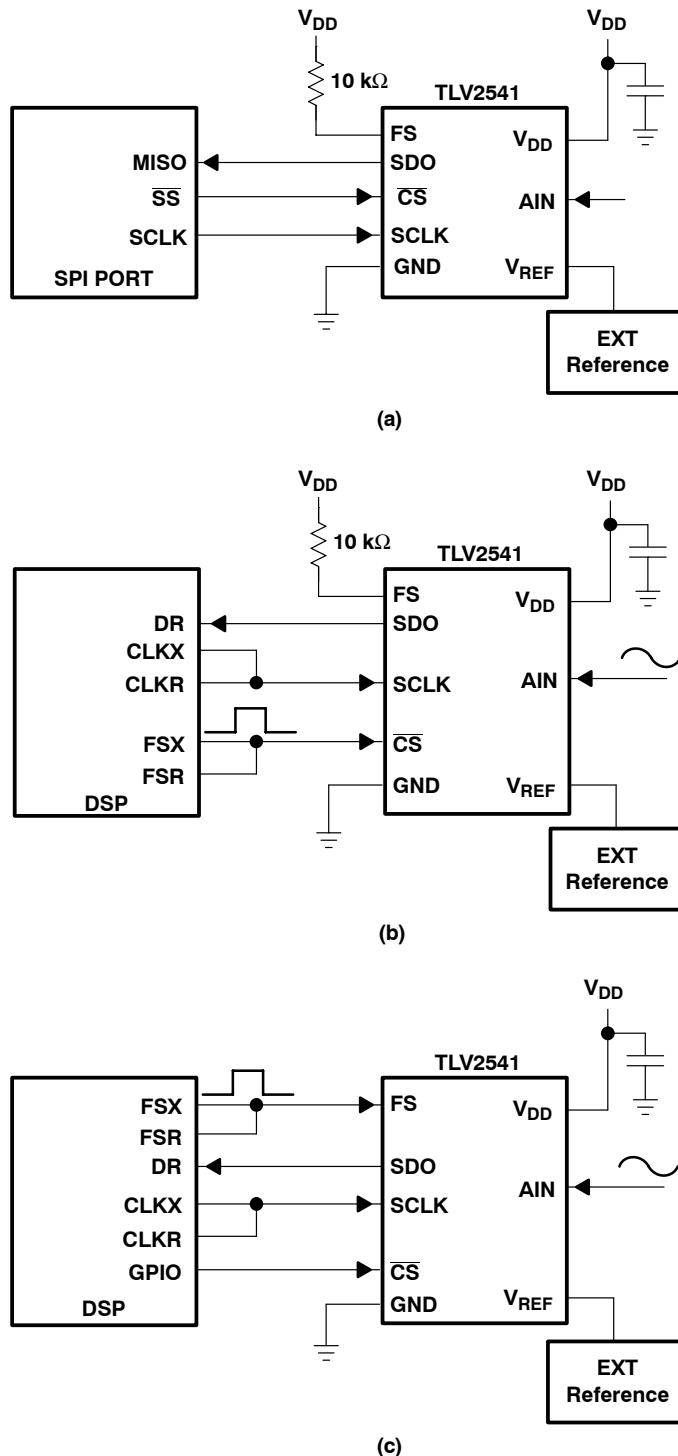
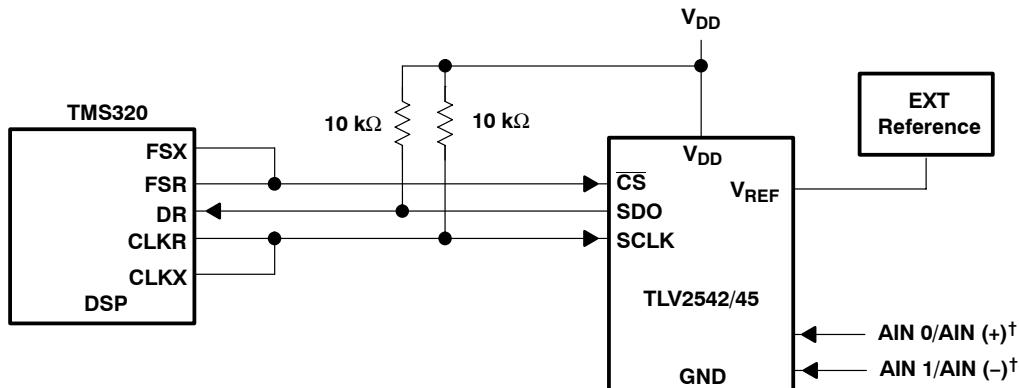


Figure 29. Typical TLV2541 Interface to a TMS320 DSP

APPLICATION INFORMATION



† For TLV2545 only

Figure 30. Typical TLV2542/45 Interface to a TMS320 DSP

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TLV2541CDGK | ACTIVE | VSSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-1-260C-UNLIM | 0 to 70 | AGZ | Samples |
| TLV2541CDGKG4 | ACTIVE | VSSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-1-260C-UNLIM | 0 to 70 | AGZ | Samples |
| TLV2541CDGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-1-260C-UNLIM | 0 to 70 | AGZ | Samples |
| TLV2541ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 2541I | Samples |
| TLV2541IDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 2541I | Samples |
| TLV2541IDGK | ACTIVE | VSSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | AHA | Samples |
| TLV2541IDGKG4 | ACTIVE | VSSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | AHA | Samples |
| TLV2541IDGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | AHA | Samples |
| TLV2541IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 2541I | Samples |
| TLV2542CDGK | ACTIVE | VSSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-1-260C-UNLIM | 0 to 70 | AHB | Samples |
| TLV2542CDGKG4 | ACTIVE | VSSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-1-260C-UNLIM | 0 to 70 | AHB | Samples |
| TLV2542CDGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-1-260C-UNLIM | 0 to 70 | AHB | Samples |
| TLV2542ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 2542I | Samples |
| TLV2542IDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 2542I | Samples |
| TLV2542IDGK | ACTIVE | VSSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | AHC | Samples |
| TLV2542IDGKG4 | ACTIVE | VSSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | AHC | Samples |
| TLV2542IDGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | AHC | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|---|
| TLV2542IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 2542I | Samples |
| TLV2545CDGK | ACTIVE | VSSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-1-260C-UNLIM | 0 to 70 | AHD | Samples |
| TLV2545ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 2545I | Samples |
| TLV2545IDGK | ACTIVE | VSSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | AHE | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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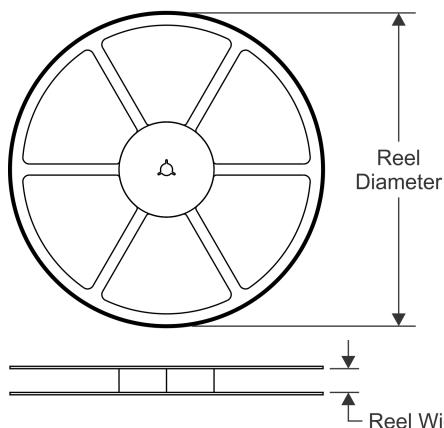
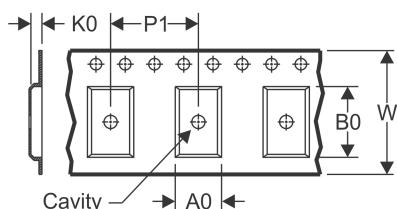
www.ti.com

PACKAGE OPTION ADDENDUM

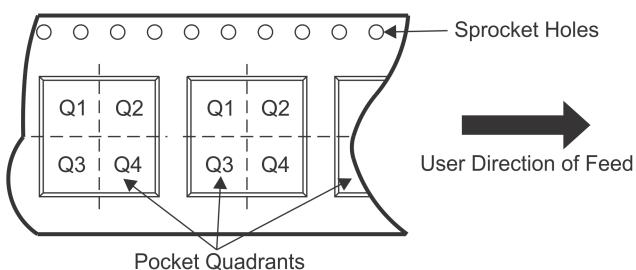
10-Jun-2014

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

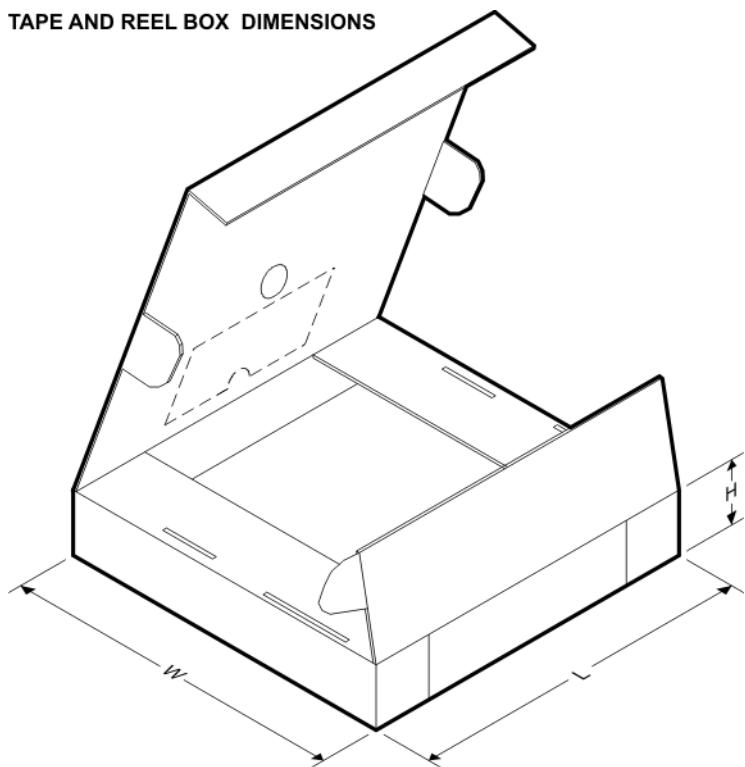
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLV2541CDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV2541IDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV2541IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV2542CDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV2542IDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV2542IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

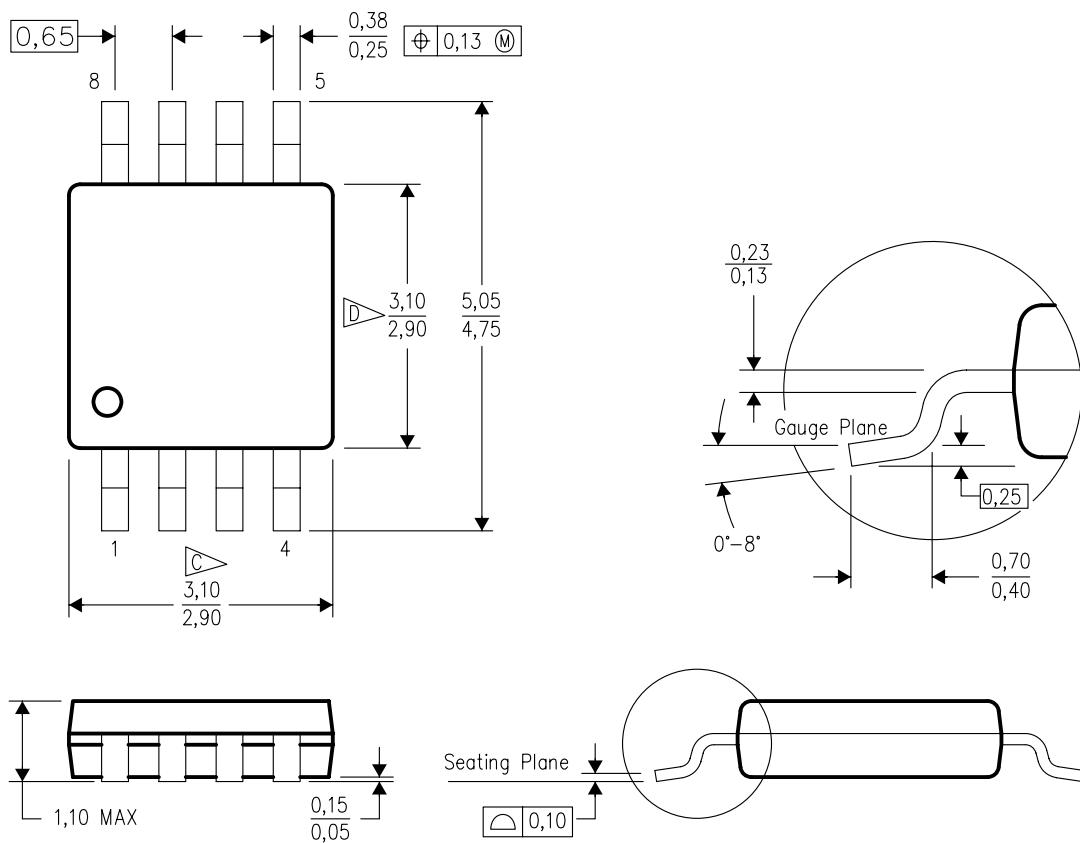
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TLV2541CDGKR | VSSOP | DGK | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| TLV2541IDGKR | VSSOP | DGK | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| TLV2541IDR | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| TLV2542CDGKR | VSSOP | DGK | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| TLV2542IDGKR | VSSOP | DGK | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| TLV2542IDR | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



4073329/E 05/06

NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

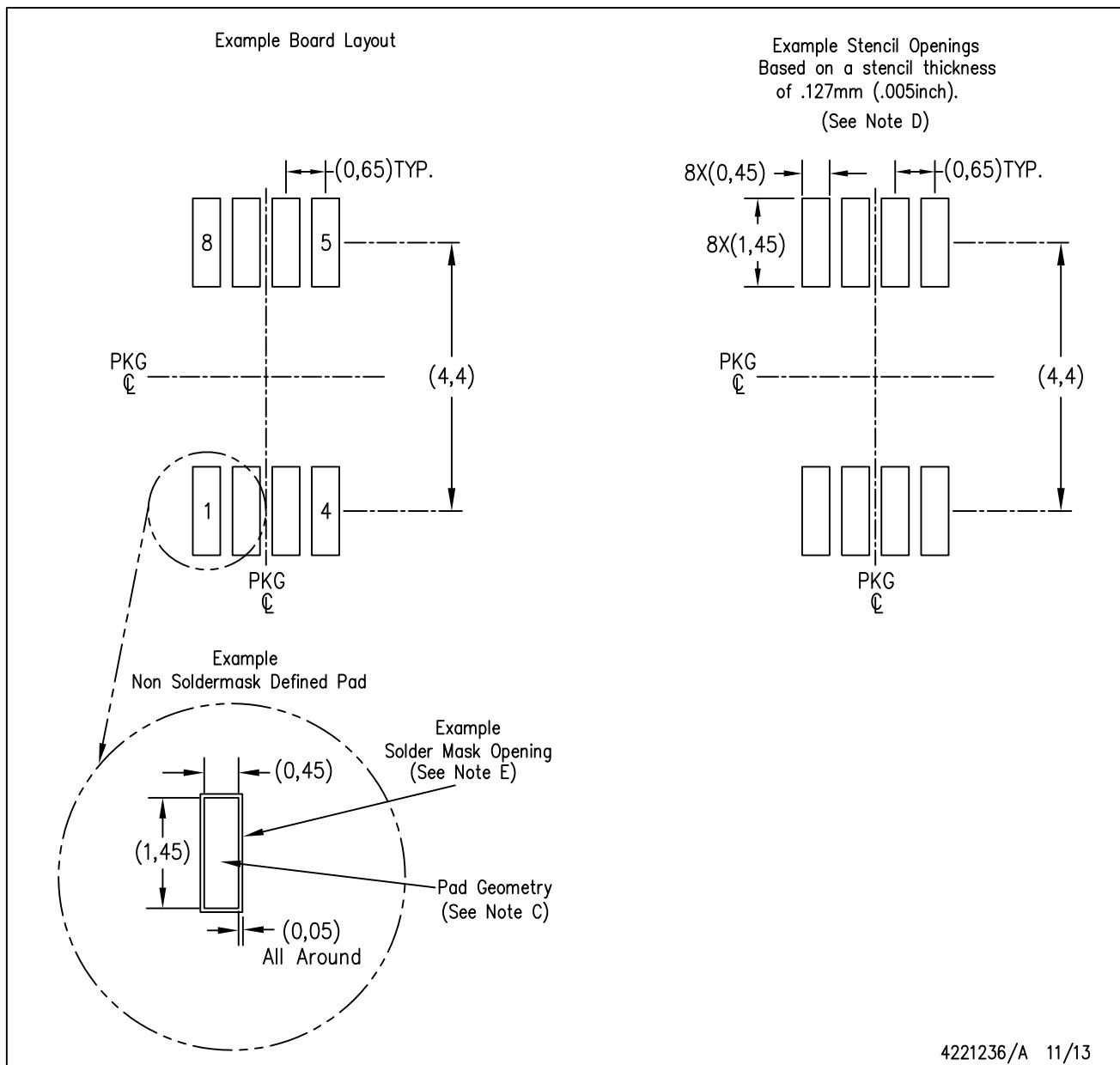
 Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.

 Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.

E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S-PDSO-G8)

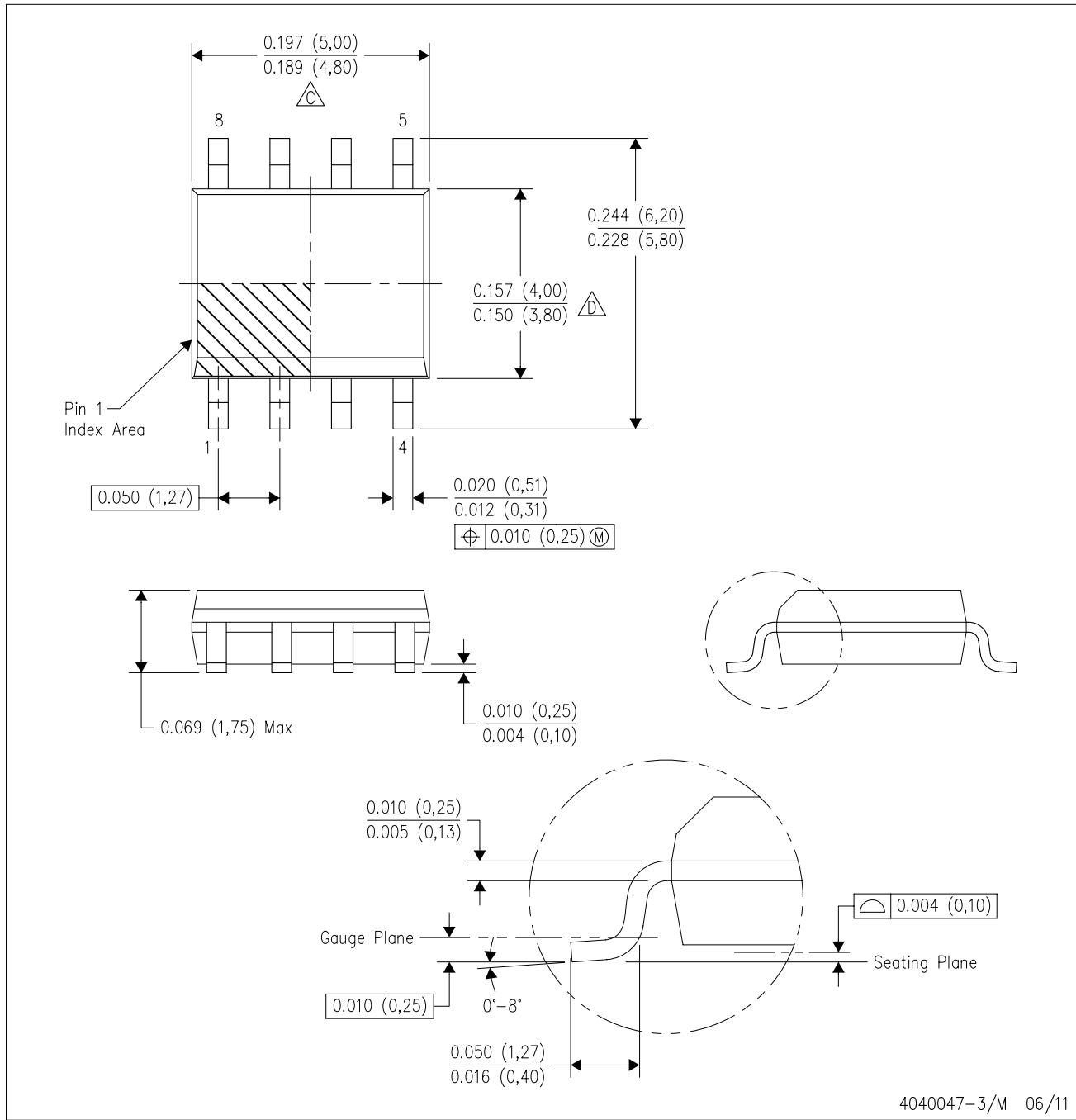
PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

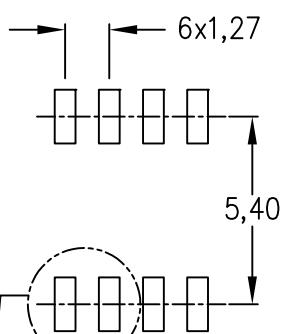
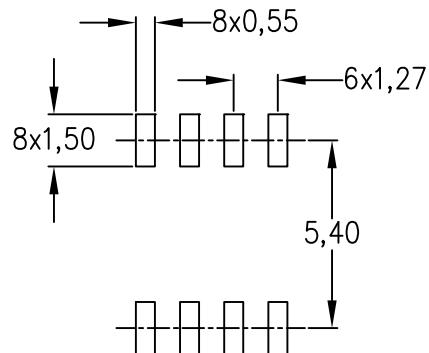
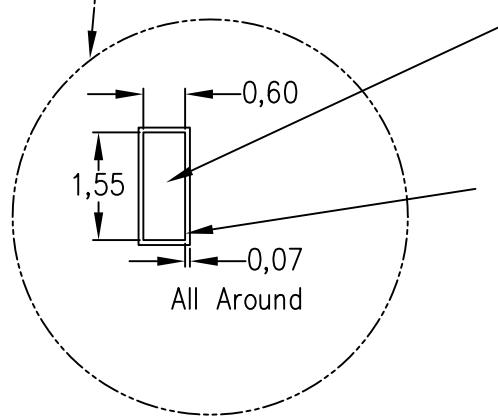
△C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.

△D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.

E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)Example
Non Soldermask Defined PadExample
Pad Geometry
(See Note C)Example
Solder Mask Opening
(See Note E)

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- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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