**Engineered Components Company** a division of Cornucopia Tool & Plastics, Inc.
1198 Farroll Road, Suite 4, Grover Beach, California 93433 / Phone: (805)473-1217 Fax: (805)473-2378

Date: October 28, 2009

# SMDDPGM-TTL-102 Part Description

This special part is similar to the MDFDPGM-TTL-XX-XXX product. The brochure for that product line is on our website at:

www.cornucopiaplastics.com/ec2/products/digital_modules/pulse_generator_modules/MDFDPGM_TTL_XX_XXX.htm

The SMDDPGM-TTL-102 has a Pulse Delay of 12+/-1nS, and a Pulse Width of 25+/-1nS. These specifications are set with a 20MHz, square-wave input. The lead type is "F" or thru-hole leads. All else is the same as the MDFDPGM-TTL-XX-XXX product line.

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EC²


*low profile*

# T²L COMPATIBLE LOGIC DELAY MODULE

## (LOW POWER SCHOTTKY)

- T²L input and outputs
- Delays stable and precise
- 14-pin DIP package (.250 high)
- Available in delays from 50 to 500ns
- 20% taps — each isolated and with 20 low power Schottky T²L fan-out capacity
- Rise time 8ns maximum

# design notes

The "DIP Series" Low Power Schottky Logic Delay Modules developed by Engineered Components Company have been designed to provide precise tapped delays with required driving and pick-off circuitry contained in a single 14-pin DIP package. These logic delay modules are of hybrid construction utilizing the proven technologies of active integrated circuitry and of passive networks utilizing capacitive, inductive and resistive elements. The ICs utilized in these modules are burned-in to Level B of MIL-STD-883 to ensure a high MTBF. The MTBF on these modules, when calculated per MIL-HDBK-217B for a 50°C ground fixed environment, is in excess of 3 million hours. Module design includes compensation for propagation delays and incorporates internal termination at the output; no additional external components are needed to obtain the desired delay.

The LPSLDM is offered in 22 delays from 50ns to 500ns with each module incorporating taps at 20% increments of total delay. Delay tolerances are maintained as shown in the accompanying part number table, when tested under the "Test Conditions" shown. Delay time is measured at the +1.3V level on the leading edge. Rise time for all modules is 8ns maximum when measured from 0.8V to 2.0V. Temperature coefficient of delay is approximately +500ppm/°C over the operating temperature range of 0 to +70°C.

These modules accept either logic "1" or logic "0" inputs and reproduce the logic at the selected output tap without inversion. The delay modules are intended primarily for use with positive going pulses and are calibrated to the tolerances shown in the table on rising edge delay; where best accuracy is desired in applications using falling edge timing, it is recommended that a special unit be calibrated for the specific application. Each module has the capability of driving up to 20 low power Schottky loads at each tap.

These "DIP Series" modules are packaged in a 14-pin DIP housing, molded of flame-proof Diallyl Phthalate per MIL-M-14, type SDG-F, and are fully encapsulated in epoxy resin. Flat metal leads meet the solderability requirements of MIL-STD-202, Method 208. Leads provide positive standoff from the printed circuit board to permit solder-fillet formation and flush cleaning of solder-flux residues for improved reliability.

EC² **engineered components company**

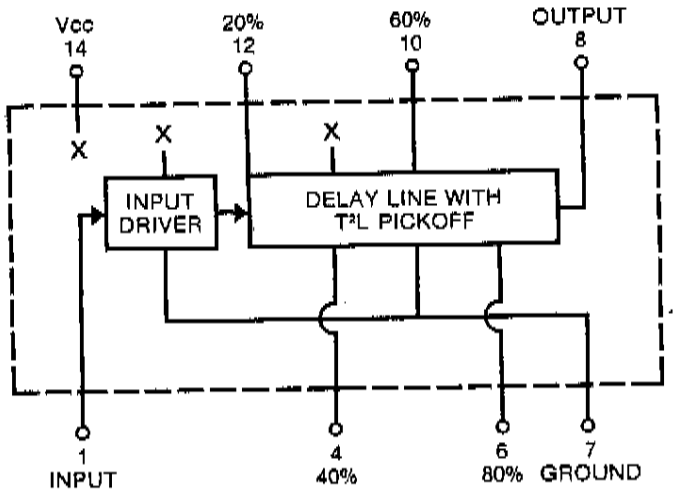
3580 Sacramento Drive, P. O. Box 8121, San Luis Obispo, CA 93403-8121

Phone: (805) 544-3800

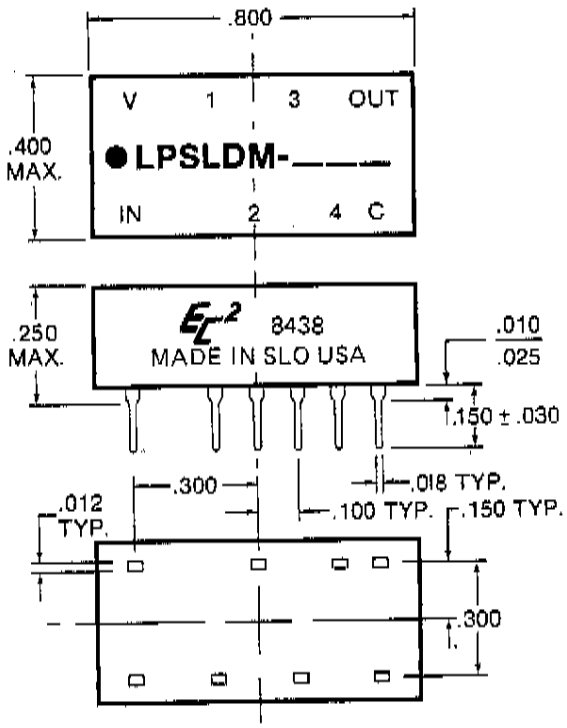
## DESIGN NOTES (continued)

Marking consists of manufacturer's name, logo (EC2), part number, terminal identification and date code of manufacture. All marking is applied by silk screen process using white epoxy paint in accordance with MIL-STD-130, to meet the permanency of identification required by MIL-STD-202, Method 215.

### BLOCK DIAGRAM IS SHOWN BELOW




### MECHANICAL DETAIL IS SHOWN BELOW




## TEST CONDITIONS

1. All measurements are made at 25°C.
2. $V_{cc}$ supply voltage is maintained at 5.0V DC.
3. All units are tested using a low power Schottky toggle-type positive input pulse and one low power Schottky $T^2L$ load at the output being tested.

$\phi$ 4. Input pulse width used is 5 to 10ns longer than full delay of module under test; spacing between pulses (falling edge to rising edge) is three times the pulse width used.

## OPERATING SPECIFICATIONS

* $V_{cc}$ supply voltage: . . . . . 4.75 to 5.25V DC

$V_{cc}$ supply current:

- Constant "0" in . . . . . 16ma typical
- Constant "1" in . . . . . 3ma typical

Logic 1 input:

- Voltage . . . . . 2V min.; 5.5V max.
- Current . . . . . 2.4V = 20ua max.
  5.5V = .1ma max.

Logic 0 input:

- Voltage . . . . . .8V max.
- Current . . . . . −.4ma max. (@.4V in)

Logic 1 Voltage out: . . . . . 2.7V min.

Logic 0 Voltage out: . . . . . .5V max.

Operating temperature range: . . . . . 0 to 70°C.

Storage temperature: . . . . . −55 to +125°C.

* Delays increase or decrease approximately 2% for a respective increase or decrease of 5% in supply voltage.

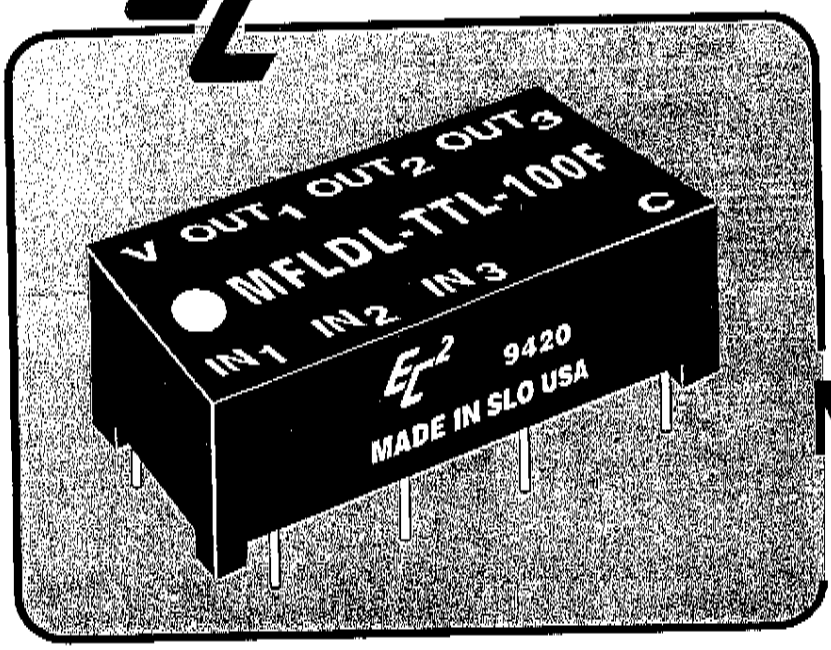
## PART NUMBER TABLE

| $\phi$ DELAYS AND TOLERANCES (in ns) | | | | | |
|---|---|---|---|---|---|
| PART NO. | Tap 1 | Tap 2 | Tap 3 | Tap 4 | OUTPUT |
| LPSLDM-50 | 10 ±1 | 20 ±1 | 30 ±1.5 | 40 ±2 | 50 ±2 |
| LPSLDM-55 | 11 ±1 | 22 ±1 | 33 ±1.5 | 44 ±2 | 55 ±2 |
| LPSLDM-60 | 12 ±1 | 24 ±1.5 | 36 ±1.5 | 48 ±2 | 60 ±2 |
| LPSLDM-65 | 13 ±1 | 26 ±1.5 | 39 ±1.5 | 52 ±2 | 65 ±2 |
| LPSLDM-70 | 14 ±1 | 28 ±1.5 | 42 ±2 | 56 ±2 | 70 ±2.5 |
| LPSLDM-75 | 15 ±1 | 30 ±1.5 | 45 ±2 | 60 ±2 | 75 ±2.5 |
| LPSLDM-80 | 16 ±1 | 32 ±1.5 | 48 ±2 | 64 ±2 | 80 ±2.5 |
| LPSLDM-85 | 17 ±1 | 34 ±1.5 | 51 ±2 | 68 ±2 | 85 ±2.5 |
| LPSLDM-90 | 18 ±1 | 36 ±1.5 | 54 ±2 | 72 ±2.5 | 90 ±3 |
| LPSLDM-95 | 19 ±1 | 38 ±1.5 | 57 ±2 | 76 ±2.5 | 95 ±3 |
| LPSLDM-100 | 20 ±1 | 40 ±1.5 | 60 ±2 | 80 ±3 | 100 ±3 |
| LPSLDM-125 | 25 ±1 | 50 ±2 | 75 ±2.5 | 100 ±3 | 125 ±4 |
| LPSLDM-150 | 30 ±1.5 | 60 ±2 | 90 ±3 | 120 ±4 | 150 ±5 |
| LPSLDM-175 | 35 ±1.5 | 70 ±2.5 | 105 ±4 | 140 ±5 | 175 ±5 |
| LPSLDM-200 | 40 ±1.5 | 80 ±2.5 | 120 ±4 | 160 ±5 | 200 ±6 |
| LPSLDM-225 | 45 ±2 | 90 ±3 | 135 ±4 | 180 ±6 | 225 ±7 |
| LPSLDM-250 | 50 ±2 | 100 ±3 | 150 ±4.5 | 200 ±6 | 250 ±8 |
| LPSLDM-300 | 60 ±2 | 120 ±4 | 180 ±5 | 240 ±7 | 300 ±9 |
| LPSLDM-350 | 70 ±2 | 140 ±4.5 | 210 ±7 | 280 ±9 | 350 ±11 |
| LPSLDM-400 | 80 ±3 | 160 ±5 | 240 ±7 | 320 ±10 | 400 ±12 |
| LPSLDM-450 | 90 ±3 | 180 ±6 | 270 ±8 | 360 ±11 | 450 ±14 |
| LPSLDM-500 | 100 ±3 | 200 ±6 | 300 ±9 | 400 ±12 | 500 ±15 |

$\phi$ All modules can be operated with a minimum input pulse width of 40% of full delay and pulse period approaching square wave; since delay accuracies may be somewhat degraded, it is suggested that the module be evaluated under the intended specific operating conditions. Special modules can be readily manufactured to improve accuracies and/or provide customer specified random delay times for specific applications.

Replacement for MTTLDL

EC²




*low profile*

# T²L COMPATIBLE MULTI-LOGIC DELAY LINE

- **T²L FAST Inputs and outputs**
- **Delays stable and precise**
- **14-pin DIP package**
- **Leads — thru-hole, J, Gull Wing or Tucked**
- **Available in delays from 5 to 250ns — each isolated and with 10 T²L fan-out capacity**
- **Rise time 4ns maximum**

# design notes

The "DIP Series" Multiple Logic Delay Lines developed by Engineered Components Company have been designed to provide precise delays with required driving and pick-off circuitry contained in a single 14-pin DIP package compatible with FAST T²L circuits. These logic delay lines are of hybrid construction utilizing the proven technologies of active integrated circuitry and of passive networks utilizing capacitive, inductive and resistive elements. The MTBF on these modules, when calculated per MIL-HDBK-217 for a 50° C ground fixed environment, is in excess of 2 million hours. Module design includes compensation for propagation delays and incorporates internal termination at the output; no additional external components are needed to obtain the desired delay.

The MFLDL-TTL is offered in 42 delays from 5 to 250ns. Each module includes three (3) separate delay lines, each isolated and fully buffered. Delay tolerances are maintained, as shown in the accompanying Part Number Table, when tested under the "Test Conditions" shown. Delay time is measured at the +1.5V level on the leading edge. Rise time for all modules is 4ns maximum, when measured from 0.75V to 2.4V. Temperature coefficient of delay is approximately +1200 ppm/°C over the operating temperature range of 0 to +70°C.

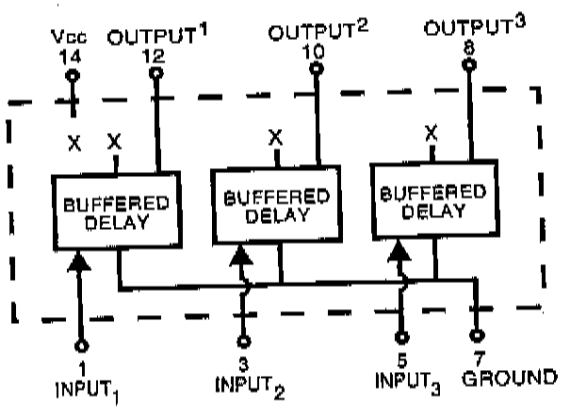
These modules accept either logic "1" or logic "0" inputs and reproduce the logic at the output without inversion. The delay modules are intended primarily for use with positive going pulses and are calibrated to the tolerances shown in the table on rising edge delay; where best accuracy is desired in applications using falling edge timing, it is recommended that a special unit be calibrated for the specific application. Each individual delay line has the capability of driving up to 10 T²L loads.

These "DIP Series" modules are packaged in a 14-pin DIP housing, molded of flame-proof Diallyl Phthalate per MIL-M-14, Type SDG-F, and are fully encapsulated in epoxy resin. Leads meet the solderability requirements of MIL-STD-202, Method 208. Corner standoffs on the housing of the thru-hole lead version and the lead design of the surface mount versions provide positive standoff from the printed circuit board to permit solder-fillet formation and flush cleaning of solder-flux residues for improved reliability.

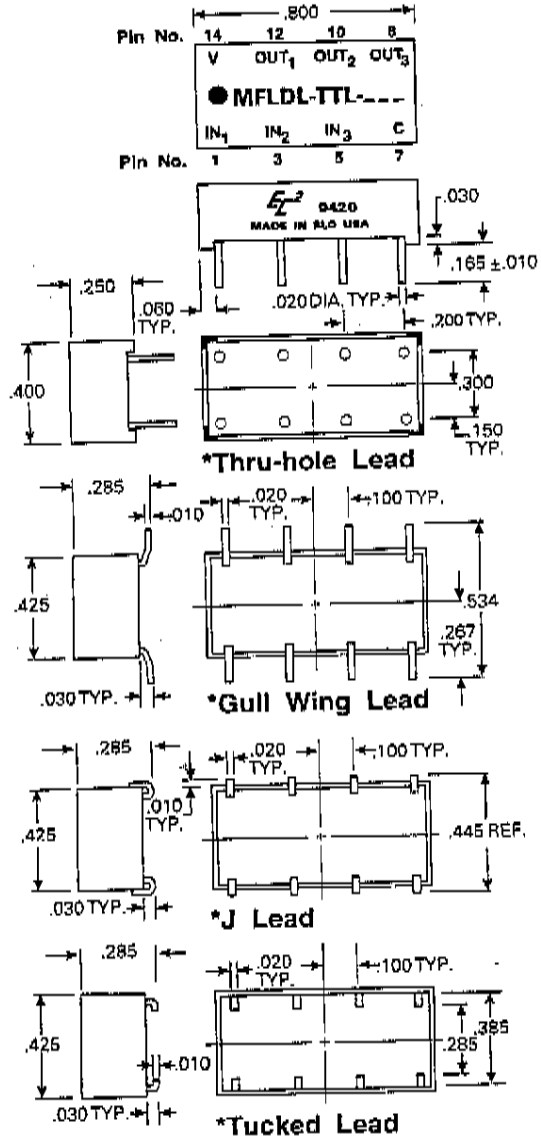
Marking consists of manufacturer's name, logo (EC²), part number, terminal identification and date code of manufacture. All marking is applied by silk screen process using white epoxy paint in accordance with MIL-STD-130, to meet the permanency of identification required by MIL-STD-202, Method 215.

EC² **engineered components company**
3580 SACRAMENTO DRIVE • P.O. BOX 8121, SAN LUIS OBISPO, CA 93403-8121
(805) 544-3800 • OUTSIDE CALIFORNIA (800) 235-4144 • FAX (805) 544-8091

## BLOCK DIAGRAM IS SHOWN BELOW




## MECHANICAL DETAIL IS SHOWN BELOW




## TEST CONDITIONS

1. All measurements are made at 25°C.
2. $V_{CC}$ supply voltage is maintained at 5.0V DC.
3. All units are tested using a FAST toggle-type positive input pulse and one FAST $T^2L$ load at the output.
4. Ø Input pulse width used is 100% longer than delay of module under test; spacing between pulses (falling edge to rising edge) is three times the pulse width used.

## OPERATING SPECIFICATIONS

| | |
|---|---|
| $V_{CC}$ supply voltage: | 4.75 to 5.25V DC |
| $V_{CC}$ supply current: | |
| Constant "0" in | 85mA typical |
| Constant "1" in | 5mA typical |
| Logic 1 Input: | |
| Voltage | 2V min.; $V_{CC}$ max. |
| Current | 2.7V = 20uA max. 5.5V = 1mA max. |
| Logic 0 Input: | |
| Voltage | .8V max. |
| Current | –.6mA max. |
| Logic 1 Voltage out: | 2.7V min. |
| Logic 0 Voltage out: | .5V max. |
| Operating temperature range: | 0 to +70°C |
| Storage temperature: | –55 to +125°C. |

Delays increase or decrease approximately 4% for a respective increase or decrease of 5% in supply voltage.

## PART NUMBER TABLE

*** Suffix Part Number with G (for Gull Wing Lead), J (for J Lead), F (for Thru-hole Lead) or T (for Tucked Lead). Examples: MFLDL-TTL-10G (Gull Wing), MFLDL-TTL-25J (J Lead), MFLDL-TTL-75F (Thru-hole Lead) or MFLDL-TTL-80T (Tucked Lead).**

| Ø DELAYS AND TOLERANCES (in ns) | | | |
|---|---|---|---|
| PART NO. | OUTPUT | PART NO. | OUTPUT |
| MFLDL-TTL-5 | 5 ± 1 | MFLDL-TTL-30 | 30 ± 1.5 |
| MFLDL-TTL-6 | 6 ± 1 | MFLDL-TTL-35 | 35 ± 1.5 |
| MFLDL-TTL-7 | 7 ± 1 | MFLDL-TTL-40 | 40 ± 1.5 |
| MFLDL-TTL-8 | 8 ± 1 | MFLDL-TTL-45 | 45 ± 2 |
| MFLDL-TTL-9 | 9 ± 1 | MFLDL-TTL-50 | 50 ± 2 |
| MFLDL-TTL-10 | 10 ± 1 | MFLDL-TTL-55 | 55 ± 2 |
| MFLDL-TTL-11 | 11 ± 1 | MFLDL-TTL-60 | 60 ± 2 |
| MFLDL-TTL-12 | 12 ± 1 | MFLDL-TTL-65 | 65 ± 2.5 |
| MFLDL-TTL-13 | 13 ± 1 | MFLDL-TTL-70 | 70 ± 2.5 |
| MFLDL-TTL-14 | 14 ± 1 | MFLDL-TTL-75 | 75 ± 2.5 |
| MFLDL-TTL-15 | 15 ± 1 | MFLDL-TTL-80 | 80 ± 2.5 |
| MFLDL-TTL-16 | 16 ± 1 | MFLDL-TTL-85 | 85 ± 3 |
| MFLDL-TTL-17 | 17 ± 1 | MFLDL-TTL-90 | 90 ± 3 |
| MFLDL-TTL-18 | 18 ± 1 | MFLDL-TTL-95 | 95 ± 3 |
| MFLDL-TTL-19 | 19 ± 1 | MFLDL-TTL-100 | 100 ± 3 |
| MFLDL-TTL-20 | 20 ± 1 | MFLDL-TTL-125 | 125 ± 4 |
| MFLDL-TTL-21 | 21 ± 1 | MFLDL-TTL-150 | 150 ± 4.5 |
| MFLDL-TTL-22 | 22 ± 1 | MFLDL-TTL-175 | 175 ± 5 |
| MFLDL-TTL-23 | 23 ± 1 | MFLDL-TTL-200 | 200 ± 6 |
| MFLDL-TTL-24 | 24 ± 1 | MFLDL-TTL-225 | 225 ± 7 |
| MFLDL-TTL-25 | 25 ± 1 | MFLDL-TTL-250 | 250 ± 8 |

Ø All modules can be operated with a minimum input pulse width of 100% of full delay and pulse period approaching square wave; since delay accuracies may be somewhat degraded, it is suggested that the module be evaluated under the intended specific operating conditions. Special modules can be readily manufactured to improve accuracies and/or provide customer specified random delay times for specific applications.