



LC87F2H08A

CMOS IC

8K-byte FROM and 256-byte RAM integrated

8-bit 1-chip Microcontroller

ON Semiconductor®

<http://onsemi.com>

Overview

The LC87F2H08A is an 8-bit microcomputer that, centered around a CPU running at a minimum bus cycle time of 83.3ns, integrates on a single chip a number of hardware features such as 8K-byte flash ROM (On-board-programmable), 256-byte RAM, an On-chip-debugger, sophisticated 16-bit timers/counters (may be divided into 8-bit timers), a 16-bit timer/counter (may be divided into 8-bit timers/counters or 8-bit PWMs), two 8-bit timers with a prescaler, a base timer serving as a time-of-day clock, a high-speed clock counter, a synchronous SIO interface, an asynchronous/synchronous SIO interface, a UART interface (full duplex), two 12-bit PWM channels, a 12/8-bit 9-channel AD converter, a system clock frequency divider, an internal reset and a 20-source 10-vector interrupt feature.

Features

■Flash ROM

- Capable of on-board programming with a wide range (2.2 to 5.5V) of voltage source.
- Block-erasable in 128 byte units
- Writable in 2-byte units
- 8192×8 bits

■RAM

- 256×9 bits

■Minimum Bus Cycle

- 83.3ns (12MHz at $V_{DD}=2.7V$ to 5.5V)
- 100ns (10MHz at $V_{DD}=2.2V$ to 5.5V)
- 250ns (4MHz at $V_{DD}=1.8V$ to 5.5V)

Note: The bus cycle time here refers to the ROM read speed.

* This product is licensed from Silicon Storage Technology, Inc. (USA).

■Minimum Instruction Cycle Time

- 250ns (12MHz at VDD=2.7V to 5.5V)
- 300ns (10MHz at VDD=2.2V to 5.5V)
- 750ns (4MHz at VDD=1.8V to 5.5V)

■Ports

- Normal withstand voltage I/O ports

Ports whose I/O direction can be designated in 1-bit units 16 (Pin, P20, P21, P30, P31, P70 to P73)

Ports whose I/O direction can be designated in 4-bit units 8 (P0n)

- Dedicated oscillator ports/input ports

2 (CF1/XT1, CF2/XT2)

- Reset pin

1 (RES)

- Power pins

3 (VSS1, VSS2, VDD1)

■Timers

- Timer 0: 16-bit timer/counter with a capture register.

Mode 0: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) × 2 channels

Mode 1: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register)

+ 8-bit counter (with an 8-bit capture register)

Mode 2: 16-bit timer with an 8-bit programmable prescaler (with a 16-bit capture register)

Mode 3: 16-bit counter (with a 16-bit capture register)

- Timer 1: 16-bit timer/counter that supports PWM/toggle outputs

Mode 0: 8-bit timer with an 8-bit prescaler (with toggle outputs) + 8-bit timer/
counter with an 8-bit prescaler (with toggle outputs)

Mode 1: 8-bit PWM with an 8-bit prescaler × 2 channels

Mode 2: 16-bit timer/counter with an 8-bit prescaler (with toggle outputs)
(toggle outputs also possible from the lower-order 8 bits)

Mode 3: 16-bit timer with an 8-bit prescaler (with toggle outputs)

(The lower-order 8 bits can be used as PWM)

- Timer 6: 8-bit timer with a 6-bit prescaler (with toggle outputs)

- Timer 7: 8-bit timer with a 6-bit prescaler (with toggle outputs)

- Base timer

1) The clock is selectable from the subclock (32.768kHz crystal oscillation), system clock, and timer 0 prescaler output.

2) Interrupts are programmable in 5 different time schemes

■High-Speed Clock Counter

- Can count clocks with a maximum clock rate of 20MHz (at a main clock of 10MHz).

- Can generate output real time.

■SIO

- SIO0: 8-bit Synchronous serial interface

1) LSB first/MSB first mode selectable

2) Built-in 8-bit baudrate generator (maximum transfer clock cycle=4/3tCYC)

- SIO1: 8-bit asynchronous/synchronous serial interface

Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)

Mode 1: Asynchronous serial I/O (half-duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrates)

Mode 2: Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clocks)

Mode 3: Bus mode 2 (start detect, 8 data bits, stop detect)

■UART

- Full Duplex

- 7/8/9 bit data bits selectable

- 1 Stop bit (2 bits in continuous data transmission)

- Built-in baudrate generator

■AD Converter: 12 bits/8 bits × 9 channels

- 12/8 bits AD converter resolution selectable

■ PWM: Multifrequency 12-bit PWM × 2 channels

■ Remote Control Receiver Circuit (sharing pins with P73, INT3, and T0IN)

- Noise rejection function (noise filter time constant selectable from 1 tCYC/32 tCYC/128 tCYC)

■ Clock Output Function

- Can generate clock outputs with a frequency of 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64 of the source clock selected as the system clock.
- Can generate the source clock for the subclock

■ Watchdog Timer

- External RC watchdog timer
- Interrupt and reset signals selectable

■ Interrupts

- 20 sources, 10 vector addresses

- 1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
- 2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4
4	0001BH	H or L	INT3/INT5/base timer
5	00023H	H or L	T0H
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	SIO0/UART1 receive
8	0003BH	H or L	SIO1/UART1 transmit
9	00043H	H or L	ADC/T6/T7/PWM4, PWM5
10	0004BH	H or L	Port 0

- Priority levels X > H > L
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

■ Subroutine Stack Levels: 128levels (The stack is allocated in RAM.)

■ High-speed Multiplication/Division Instructions

- 16 bits × 8 bits (5 tCYC execution time)
- 24 bits × 16 bits (12 tCYC execution time)
- 16 bits ÷ 8 bits (8 tCYC execution time)
- 24 bits ÷ 16 bits (12 tCYC execution time)

■ Oscillation Circuits

- Internal oscillation circuits

Low-speed RC oscillation circuit : For system clock (100kHz)

Medium-speed RC oscillation circuit : For system clock (1MHz)

Multifrequency RC oscillation circuit : For system clock (8MHz)

- External oscillation circuits

Hi-speed CF oscillation circuit: For system clock, with internal Rf

Low speed crystal oscillation circuit: For low-speed system clock, with internal Rf

1) The CF and crystal oscillation circuits share the same pins. The active circuit is selected under program control.

2) Both the CF and crystal oscillator circuits stop operation on a system reset. When the reset is released, only the CF oscillation circuit resumes operation.

■ System Clock Divider Function

- Can run on low current.
- The minimum instruction cycle selectable from 300ns, 600ns, 1.2μs, 2.4μs, 4.8μs, 9.6μs, 19.2μs, 38.4μs, and 76.8μs (at a main clock rate of 10MHz).

■ Internal reset function

- Power-on reset (POR) function
 - 1) POR reset is generated only at power-on time.
 - 2) The POR release level can be selected from 8 levels (1.67V, 1.97V, 2.07V, 2.37V, 2.57V, 2.87V, 3.86V, and 4.35V) through option configuration.
- Low-voltage detection reset (LVD) function
 - 1) LVD and POR functions are combined to generate resets when power is turned on and when power voltage falls below a certain level.
 - 2) The use/disuse of the LVD function and the low voltage threshold level (7 levels: 1.91V, 2.01V, 2.31V, 2.51V, 2.81V, 3.79V, 4.28V).

■ Standby Function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
 - 1) Oscillation is not halted automatically.
 - 2) There are three ways of resetting the HALT mode.
 - (1) Setting the reset pin to the low level
 - (2) System resetting by watchdog timer or low-voltage detection
 - (3) Occurrence of an interrupt
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
 - 1) The CF, RC and crystal oscillators automatically stop operation.
 - 2) There are four ways of resetting the HOLD mode.
 - (1) Setting the reset pin to the lower level.
 - (2) System resetting by watchdog timer or low-voltage detection
 - (3) Having an interrupt source established at either INT0, INT1, INT2, INT4 or INT5
* INT0 and INT1 HOLD mode reset is available only when level detection is set.
 - (4) Having an interrupt source established at port 0.
- X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer.
 - 1) The CF and RC oscillator automatically stop operation.
 - 2) The state of crystal oscillation established when the X'tal HOLD mode is entered is retained.
 - 3) There are five ways of resetting the X'tal HOLD mode.
 - (1) Setting the reset pin to the low level.
 - (2) System resetting by watchdog timer or low-voltage detection.
 - (3) Having an interrupt source established at either INT0, INT1, INT2, INT4 or INT5
* INT0 and INT1 HOLD mode reset is available only when level detection is set.
 - (4) Having an interrupt source established at port 0.
 - (5) Having an interrupt source established in the base timer circuit.

Note: Available only when X'tal oscillation is selected.

■ Onchip Debugger

- Supports software debugging with the IC mounted on the target board.
- Two channels of on-chip debugger pins are available to be compatible with small pin count devices.
DBG0 (P0), DBG1 (P1)

■ Data Security Function (flash versions only)

- Protects the program data stored in flash memory from unauthorized read or copy.
Note: This data security function does not necessarily provide absolute data security.

■ Package Form

- QFP36 (7×7): Lead-free type

■ Development Tools

- On-chip debugger: TCB87 type B + LC87F2H08A

■Programming Boards

Package	Programming boards
QFP36(7×7)	W87F24Q

■Flash ROM Programmer

Maker		Model	Supported version	Device
Flash Support Group, Inc. (FSG)	Single Programmer	AF9708 AF9709/AF9709B/AF9709C (Including Ando Electric Co., Ltd. models)	Rev 02.72 or later	LC87F2H08A
	Gang Programmer	AF9723/AF9723B(Main body) (Including Ando Electric Co., Ltd. models)	-	-
		AF9833(Unit) (Including Ando Electric Co., Ltd. models)	-	-
Flash Support Group, Inc. (FSG) + Our company (Note 1)	In-circuit Programmer	AF9101/AF9103(Main body) (FSG models)	(Note 2)	LC87F2H08A
		SIB87(Inter Face Driver) (Our company model)		
Our company	Single/Gang Programmer	SKK/SKK Type B (SANYO FWS)	Application Version 1.04 or later Chip Data Version 2.10 or later	LC87F2H08A
	In-circuit/Gang Programmer	SKK-DBG Type B (SANYO FWS)		

For information about AF-Series:

Flash Support Group, Inc.

TEL: +81-53-459-1050

E-mail: sales@j-fsg.co.jp

Note1: On-board-programmer from FSG (AF9101/AF9103) and serial interface driver from Our company (SIB87) together

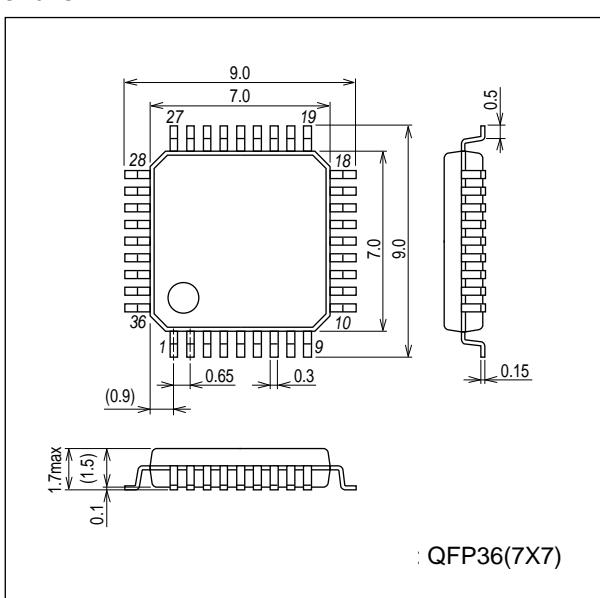
can give a PC-less, standalone on-board-programming capabilities.

Note2: It needs a special programming devices and applications depending on the use of programming environment.
Please ask FSG or Our company for the information.

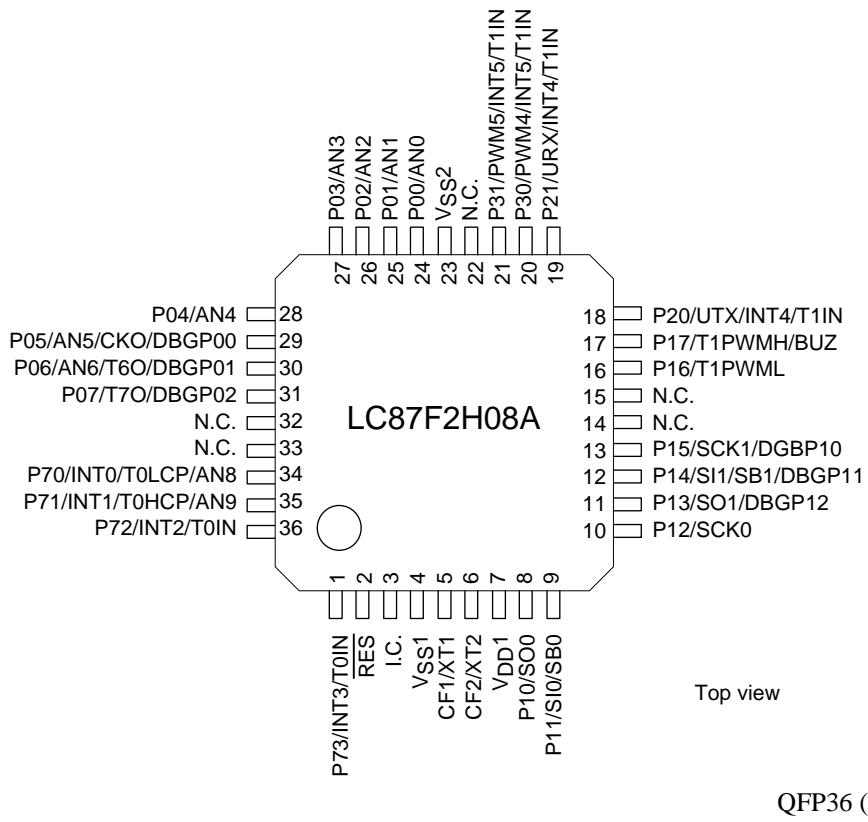
Package Dimensions

unit : mm (typ)

3162C



Pin Assignment

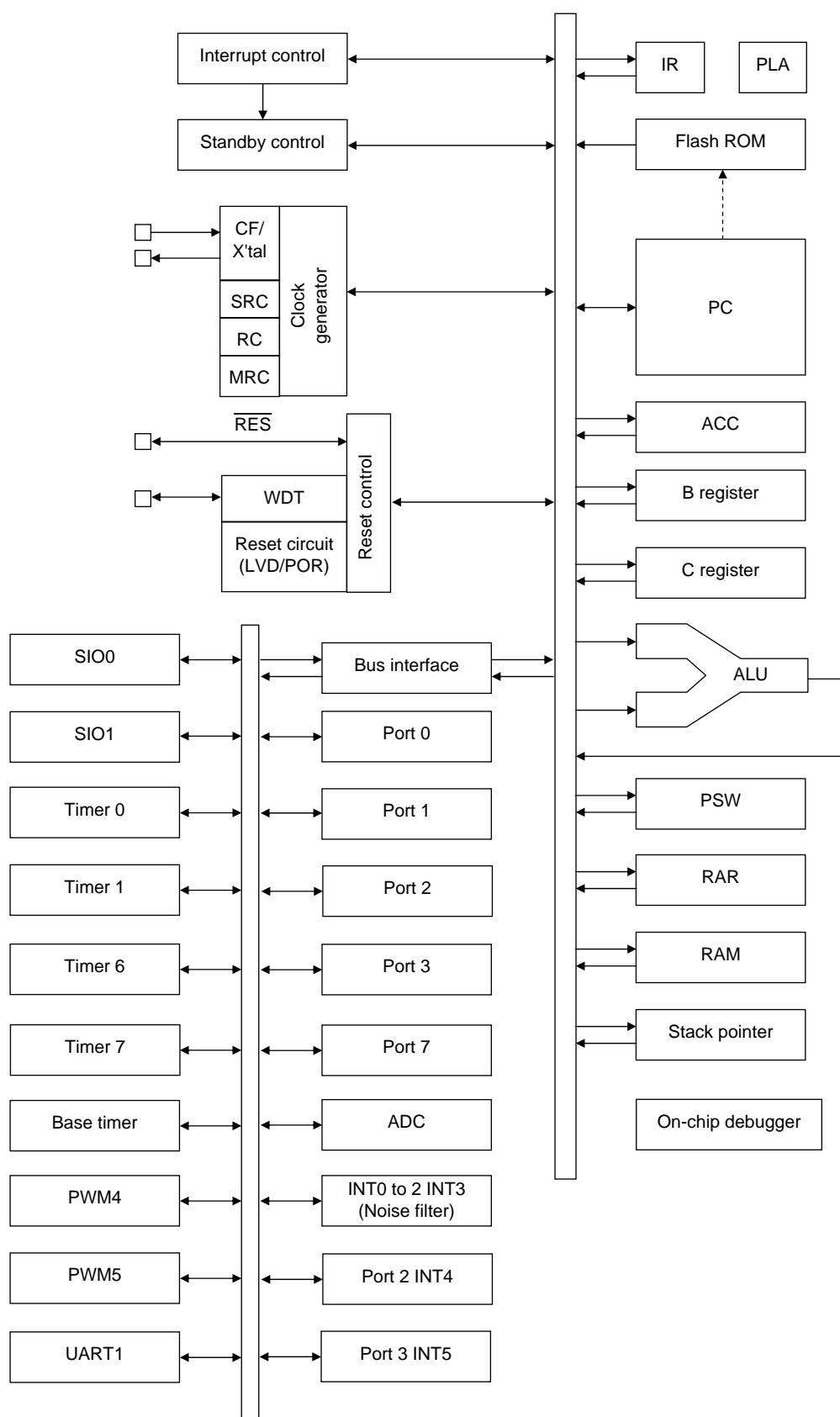


QFP36	NAME
1	P73/INT3/T0IN
2	RES
3	I.C.
4	VSS1
5	CF1/XT1
6	CF2/XT2
7	VDD1
8	P10/SO0
9	P11/SI0/SB0
10	P12/SCK0
11	P13/SO1/DBGP12
12	P14/SI1/SB1/DBGP11
13	P15/SCK1/DBGP10
14	N.C.
15	N.C.
16	P16/T1PWML
17	P17/T1PWMH/BUZ
18	P20/UTX/INT4/T1IN

QFP36	NAME
19	P21/URX/INT4/T1IN
20	P30/PWM4/INT5/T1IN
21	P31/PWM5/INT5/T1IN
22	N.C.
23	VSS2
24	P00/AN0
25	P01/AN1
26	P02/AN2
27	P03/AN3
28	P04/AN4
29	P05/AN5/CKO/DBGPO0
30	P06/AN6/T6O/DBGPO1
31	P07/T7O/DBGPO2
32	N.C.
33	N.C.
34	P70/INT0/T0LCP/AN8
35	P71/INT1/T0HCP/AN9
36	P72/INT2/T0IN

Note I.C. and N.C. pins must be held open (disconnected).

System Block Diagram



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Pin Description

Pin Name	I/O	Description	Option												
V _{SS1} ,V _{SS2}	-	- power supply pins	No												
V _{DD1}	-	+ power supply pin	No												
Port 0	I/O	<ul style="list-style-type: none"> • 8-bit I/O port • I/O specifiable in 4-bit units • Pull-up resistors can be turned on and off in 4-bit units. • HOLD reset input • Port 0 interrupt input • Pin functions P05: System clock output P06: Timer 6 toggle output P07: Timer 7 toggle output P00(AN0) to P06(AN6):AD converter input P05(DBGP00) to P07(DBGP02):On-chip debugger 0 port	Yes												
Port 1	I/O	<ul style="list-style-type: none"> • 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1-bit units. • Pin functions P10: SIO0 data output P11: SIO0 data input/bus I/O P12: SIO0 clock I/O P13: SIO1 data output P14: SIO1 data input/bus I/O P15: SIO1 clock I/O P16: Timer 1 PWML output P17: Timer 1 PWMH output/beeper output P15(DBGP10) to P13(DBGP12):On-chip debugger 1 port	Yes												
Port 2	I/O	<ul style="list-style-type: none"> • 2-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1-bit units. • Pin functions P20: UART transmit P21: UART receive P20 to P21: INT4 input/HOLD reset input/timer 1 event input/timer 0L capture input/timer 0H capture input Interrupt acknowledge types <table border="1"> <tr> <td></td><td>Rising</td><td>Falling</td><td>Rising & Falling</td><td>H level</td><td>L level</td></tr> <tr> <td>INT4</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr> </table>		Rising	Falling	Rising & Falling	H level	L level	INT4	enable	enable	enable	disable	disable	Yes
	Rising	Falling	Rising & Falling	H level	L level										
INT4	enable	enable	enable	disable	disable										
Port 3	I/O	<ul style="list-style-type: none"> • 2-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1-bit units. • Pin functions P30: PWM4 output P31: PWM5 output P30 to P31: INT5 input/HOLD reset input/timer 1 event input/timer 0L capture input/timer 0H capture input Interrupt acknowledge types <table border="1"> <tr> <td></td><td>Rising</td><td>Falling</td><td>Rising & Falling</td><td>H level</td><td>L level</td></tr> <tr> <td>INT5</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr> </table>		Rising	Falling	Rising & Falling	H level	L level	INT5	enable	enable	enable	disable	disable	Yes
	Rising	Falling	Rising & Falling	H level	L level										
INT5	enable	enable	enable	disable	disable										

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Pin Name	I/O	Description					Option																													
Port 7	I/O	<ul style="list-style-type: none"> • 4-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1-bit units. • Pin functions 																																		
P70 to P73		<ul style="list-style-type: none"> P70: INT0 input/HOLD reset input/timer 0L capture input/watchdog timer output P71: INT1 input/HOLD reset input/timer 0H capture input P72: INT2 input/HOLD reset input/timer 0 event input/timer 0L capture input P73: INT3 input (input with noise filter)/timer 0 event input/timer 0H capture input P70(AN8),P71(AN9) : AD converter input 					No																													
		Interrupt acknowledge types																																		
		<table border="1"> <thead> <tr> <th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr> </thead> <tbody> <tr> <td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr> <tr> <td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr> <tr> <td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr> <tr> <td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr> </tbody> </table>						Rising	Falling	Rising & Falling	H level	L level	INT0	enable	enable	disable	enable	enable	INT1	enable	enable	disable	enable	enable	INT2	enable	enable	enable	disable	disable	INT3	enable	enable	enable	disable	disable
	Rising	Falling	Rising & Falling	H level	L level																															
INT0	enable	enable	disable	enable	enable																															
INT1	enable	enable	disable	enable	enable																															
INT2	enable	enable	enable	disable	disable																															
INT3	enable	enable	enable	disable	disable																															
<u>RES</u>	I/O	External reset Input/internal reset output					No																													
CF1/XT1	I	<ul style="list-style-type: none"> • Ceramic resonator or 32.768kHz crystal oscillator input pin • Pin function 					No																													
CF2/XT2	I/O	<ul style="list-style-type: none"> • Ceramic resonator or 32.768kHz crystal oscillator output pin • Pin function 					No																													

Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.

Data can be read into any input port even if it is in the output mode.

Port Name	Option selected in units of	Option type	Output type	Pull-up resistor
P00 to P07	1 bit	1	CMOS	Programmable (Note 1)
		2	Nch-open drain	No
P10 to P17	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P20 to P21	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P30 to P31	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P70	-	No	Nch-open drain	Programmable
P71 to P73	-	No	CMOS	Programmable

Note 1: The control of the presence or absence of the programmable pull-up resistors for port 0 and the switching between low-and high-impedance pull-up connection is exercised in nibble (4-bit) units (P00 to 03 or P04 to 07).

Note: Be sure to electrically short-circuit between the VSS1 and VSS2 pins.

User Option Table

Option Name	Option to be Applied on	Flash-ROM Version	Option Selected in Units of	Option Selection
Port output type	P00 to P07	<input type="radio"/>	1 bit	CMOS
				Nch-open drain
	P10 to P17	<input type="radio"/>	1 bit	CMOS
				Nch-open drain
	P20 to P21	<input type="radio"/>	1 bit	CMOS
				Nch-open drain
	P30 to P31	<input type="radio"/>	1 bit	CMOS
				Nch-open drain
Program start address	-	<input type="radio"/>	-	00000h
				01E00h
Low-voltage detection reset function	Detect function	<input type="radio"/>	-	Enable:Use
				Disable:Not Used
Power-on reset function	Power-On reset level	<input type="radio"/>	-	7-level
			-	8-level

Recommended Unused Pin Connections

Port Name	Recommended Unused Pin Connections	
	Board	Software
P00 to P07	Open	Output low
P10 to P17	Open	Output low
P20 to P21	Open	Output low
P30 to P31	Open	Output low
P70 to P73	Open	Output low
CF1/XT1	Pulled low with a 100kΩ resistor or less	General-purpose input port
CF2/XT2	Pulled low with a 100kΩ resistor or less	General-purpose input port

On-chip Debugger pin connection requirements

For the treatment of the on-chip debugger pins, refer to the separately available documents entitled "RD87 on-chip debugger installation manual" and "LC872000 series on-chip debugger pin connection requirements"

Note: Be sure to electrically short-circuit between the V_{SS}1 and V_{SS}2 pins.

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Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$, $V_{SS1} = V_{SS2} = 0\text{V}$

Parameter	Symbol	Pin/Remarks	Conditions	Specification				unit
				$V_{DD}[\text{V}]$	min	typ	max	
Maximum supply voltage	V_{DD} max	V_{DD1}			-0.3		+6.5	V
Input voltage	V_I	CF1, CF2			-0.3		$V_{DD} + 0.3$	
Input/output voltage	V_{IO}	Ports 0, 1, 2, 3 Port 7			-0.3		$V_{DD} + 0.3$	
High level output current	Peak output current	IOPH(1)	Ports 0, 1, 2, 3	CMOS output select Per 1 applicable pin		-10		mA
		IOPH(2)	P71 to P73	Per 1 applicable pin		-5		
	Mean output current (Note 1-1)	IOMH(1)	Ports 0, 1, 2, 3	CMOS output select Per 1 applicable pin		-7.5		
		IOMH(2)	P71 to P73	Per 1 applicable pin		-3		
	Total output current	$\Sigma I_{OAH}(1)$	P71 to P73	Total of all applicable pins		-10		
		$\Sigma I_{OAH}(2)$	P10 to P14	Total of all applicable pins		-20		
		$\Sigma I_{OAH}(3)$	P15 to P17 Ports 0, 2, 3	Total of all applicable pins		-20		
		$\Sigma I_{OAH}(4)$	Ports 0, 1, 2, 3	Total of all applicable pins		-25		
	Peak output current	IOPL(1)	P02 to P07 Ports 1, 2, 3	Per 1 applicable pin			20	
		IOPL(2)	P00, P01	Per 1 applicable pin			30	
Low level output current		IOPL(3)	Port 7	Per 1 applicable pin			10	mW
	Mean output current (Note 1-1)	IOML(1)	P02 to P07 Ports 1, 2, 3	Per 1 applicable pin			15	
		IOML(2)	P00, P01	Per 1 applicable pin			20	
		IOML(3)	Port 7	Per 1 applicable pin			7.5	
	Total output current	$\Sigma I_{OAL}(1)$	Port 7	Total of all applicable pins			15	
		$\Sigma I_{OAL}(2)$	Port 0	Total of all applicable pins			40	
		$\Sigma I_{OAL}(3)$	P10 to P14	Total of all applicable pins			35	
		$\Sigma I_{OAL}(4)$	Ports 1, 2, 3	Total of all applicable pins			40	
		$\Sigma I_{OAL}(5)$	Ports 0, 1, 2, 3	Total of all applicable pins			70	
	Power Dissipation	Pd max(1)	QFP36(7x7)	Ta=-40 to +85°C Package only			120	mW
		Pd max(2)		Ta=-40 to +85°C Package with thermal resistance board (Note 1-2)			275	
Operating ambient Temperature	T_{opr}				-40		+85	°C
Storage ambient temperature	T_{stg}				-55		+125	

Note 1-1: The mean output current is a mean value measured over 100ms.

Note 1-2: SEMI standards thermal resistance board (size: 76.1×114.3×1.6mm, glass epoxy) is used.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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Allowable Operating Conditions at $T_a = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{SS1} = V_{SS2} = 0\text{V}$

Parameter	Symbol	Pin/Remarks	Conditions	Specification				unit
				$V_{DD}[\text{V}]$	min	typ	max	
Operating supply voltage (Note 2-1)	$V_{DD}(1)$	V_{DD1}	$0.245\mu\text{s} \leq t_{CYC} \leq 200\mu\text{s}$		2.7		5.5	V
	$V_{DD}(2)$		$0.294\mu\text{s} \leq t_{CYC} \leq 200\mu\text{s}$		2.2		5.5	
	$V_{DD}(3)$		$0.735\mu\text{s} \leq t_{CYC} \leq 200\mu\text{s}$		1.8		5.5	
Memory sustaining supply voltage	V_{HD}	V_{DD1}	RAM and register contents sustained in HOLD mode.		1.6			
High level input voltage	$V_{IH}(1)$	Ports 1, 2, 3, P71 to P73 P70 port input/interrupt side		1.8 to 5.5	$0.3V_{DD}+0.7$			V_{DD}
	$V_{IH}(2)$	Ports 0		1.8 to 5.5	$0.3V_{DD}+0.7$			V_{DD}
	$V_{IH}(3)$	Port 70 watchdog timer side		1.8 to 5.5	$0.9V_{DD}$			V_{DD}
	$V_{IH}(4)$	CF1, \overline{RES}		1.8 to 5.5	$0.75V_{DD}$			V_{DD}
Low level input voltage	$V_{IL}(1)$	Ports 1, 2, 3, P71 to P73 P70 port input/interrupt side		4.0 to 5.5	V_{SS}		$0.1V_{DD}+0.4$	
				1.8 to 4.0	V_{SS}		$0.2V_{DD}$	
	$V_{IL}(2)$	Ports 0		4.0 to 5.5	V_{SS}		$0.15V_{DD}+0.4$	
				1.8 to 4.0	V_{SS}		$0.2V_{DD}$	
Instruction cycle time (Note 2-1)	t_{CYC} (Note 2-2)			1.8 to 5.5	V_{SS}		$0.8V_{DD}-1.0$	μs
				2.7 to 5.5	0.245		200	
				2.2 to 5.5	0.294		200	
				1.8 to 5.5	0.735		200	
External system clock frequency	FEXCF	CF1	<ul style="list-style-type: none"> CF2 pin open System clock frequency division ratio=1/1 External system clock duty=50±5% 	2.7 to 5.5	0.1		12	MHz
				1.8 to 5.5	0.1		4	
				3.0 to 5.5	0.2		24.4	
			<ul style="list-style-type: none"> CF2 pin open System clock frequency division ratio=1/2 External system clock duty=50±5% 	2.0 to 5.5	0.2		8	
Oscillation frequency range (Note 2-3)	FmCF(1)	CF1, CF2	12MHz ceramic oscillation See Fig. 1.	2.7 to 5.5		12		MHz
	FmCF(2)	CF1, CF2	10MHz ceramic oscillation See Fig. 1.	2.2 to 5.5		10		
	FmCF(3)	CF1, CF2	4MHz ceramic oscillation. CF oscillation normal amplifier size selected. See Fig. 1. (CFLAMP=0)	1.8 to 5.5		4		
			4MHz ceramic oscillation. CF oscillation low amplifier size selected. (CFLAMP=1) See Fig. 1.	2.2 to 5.5		4		
	FmMRC		Frequency variable RC oscillation. 1/2 frequency division ratio. (RCCTD=0) (Note 2-4)	2.7 to 5.5	7.44	8.0	8.56	
	FmRC		Internal medium-speed RC oscillation	1.8 to 5.5	0.5	1.0	2.0	
	FmSRC		Internal low-speed RC oscillation	1.8 to 5.5	50	100	200	
	FsX'tal	XT1, XT2	32.768kHz crystal oscillation See Fig. 2.	1.8 to 5.5		32.768		kHz

Note 2-1: V_{DD} must be held greater than or equal to 2.2V in the flash ROM onboard programming mode.

Note 2-2: Relationship between t_{CYC} and oscillation frequency is $3/F_{mCF}$ at a division ratio of 1/1 and $6/F_{mCF}$ at a division ratio of 1/2.

Note 2-3: See Tables 1 and 2 for the oscillation constants.

Note 2-4: When switching the system clock, allow an oscillation stabilization time of 100 μs or longer after the multifrequency RC oscillator circuit transmits from the "oscillation stopped" to "oscillation enabled" state.

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Electrical Characteristics at $T_a = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{SS1} = V_{SS2} = 0\text{V}$

Parameter	Symbol	Pin/Remarks	Conditions	Specification				μA
				$V_{DD}[\text{V}]$	min	typ	max	
High level input current	$I_{IH}(1)$	Ports 0, 1, 2, 3 Port 7 \overline{RES}	Output disabled Pull-up resistor off $V_{IN}=V_{DD}$ (Including output Tr's off leakage current)	1.8 to 5.5			1	μA
	$I_{IH}(2)$	CF1	$V_{IN}=V_{DD}$	1.8 to 5.5			15	
Low level input current	$I_{IL}(1)$	Ports 0, 1, 2, 3 Port 7 \overline{RES}	Output disabled Pull-up resistor off $V_{IN}=V_{SS}$ (Including output Tr's off leakage current)	1.8 to 5.5	-1			μA
	$I_{IL}(2)$	CF1	$V_{IN}=V_{SS}$	1.8 to 5.5	-15			
High level output voltage	$V_{OH}(1)$	Ports 0, 1, 2 P71 to P73	$I_{OH}=-1\text{mA}$	4.5 to 5.5	$V_{DD}-1$			V
	$V_{OH}(2)$		$I_{OH}=-0.35\text{mA}$	2.7 to 5.5	$V_{DD}-0.4$			
	$V_{OH}(3)$		$I_{OH}=-0.15\text{mA}$	1.8 to 5.5	$V_{DD}-0.4$			
	$V_{OH}(4)$	Port 3	$I_{OH}=-6\text{mA}$	4.5 to 5.5	$V_{DD}-1$			
	$V_{OH}(5)$		$I_{OH}=-1.4\text{mA}$	2.7 to 5.5	$V_{DD}-0.4$			
	$V_{OH}(6)$		$I_{OH}=-0.8\text{mA}$	1.8 to 5.5	$V_{DD}-0.4$			
Low level output voltage	$V_{OL}(1)$	Ports 0, 1, 2, 3	$I_{OL}=10\text{mA}$	4.5 to 5.5			1.5	V
	$V_{OL}(2)$		$I_{OL}=1.4\text{mA}$	2.7 to 5.5			0.4	
	$V_{OL}(3)$		$I_{OL}=0.8\text{mA}$	1.8 to 5.5			0.4	
	$V_{OL}(4)$	Port 7	$I_{OL}=1.4\text{mA}$	2.7 to 5.5			0.4	
	$V_{OL}(5)$		$I_{OL}=0.8\text{mA}$	1.8 to 5.5			0.4	
	$V_{OL}(6)$	P00, P01	$I_{OL}=25\text{mA}$	4.5 to 5.5			1.5	
	$V_{OL}(7)$		$I_{OL}=4\text{mA}$	2.7 to 5.5			0.4	
	$V_{OL}(8)$		$I_{OL}=2\text{mA}$	1.8 to 5.5			0.4	
Pull-up resistance	$R_{pu}(1)$	Ports 0, 1, 2, 3 Port 7	$V_{OH}=0.9V_{DD}$ When Port 0 selected low-impedance pull-up.	4.5 to 5.5	15	35	80	$\text{k}\Omega$
	$R_{pu}(2)$			1.8 to 4.5	18	50	230	
	$R_{pu}(3)$	Port 0	$V_{OH}=0.9V_{DD}$ When Port 0 selected high-impedance pull-up.	1.8 to 5.5	100	210	400	
Hysteresis voltage	$V_{HYS}(1)$	Ports 1, 2, 3, 7 \overline{RES}		2.7 to 5.5		$0.1V_{DD}$		V
	$V_{HYS}(2)$			1.8 to 2.7		$0.07V_{DD}$		
Pin capacitance	CP	All pins	For pins other than that under test: $V_{IN}=V_{SS}$ $f=1\text{MHz}$ $T_a=25^{\circ}\text{C}$	1.8 to 5.5		10		pF

Serial I/O Characteristics at $T_a = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{SS1} = V_{SS2} = 0\text{V}$

1. SIO0 Serial I/O Characteristics (Note 4-1-1)

Parameter			Symbol	Pin/ Remarks	Conditions	$V_{DD}[\text{V}]$	Specification				
Serial clock	Input clock	Frequency	tSCK(1)	SCK0(P12)	• See Fig. 5.		min	typ	max	unit	
		Low level pulse width	tSCKL(1)		1.8 to 5.5	2			tCYC		
		High level pulse width	tSCKH(1)			1					
	Output clock	Frequency	tSCK(2)	SCK0(P12)	• CMOS output selected • See Fig. 5.	1.8 to 5.5	4/3			tSCK	
		Low level pulse width	tSCKL(2)				1/2				
		High level pulse width	tSCKH(2)				1/2				
Serial input	Data setup time		tsDI(1)	SB0(P11), SI0(P11)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 5.	1.8 to 5.5	0.05			μs	
	Data hold time		thDI(1)				0.05				
Serial output	Input clock	Output delay time	tdD0(1)	SO0(P10), SB0(P11)	• Continuous data transmission/reception mode (Note 4-1-2) • Synchronous 8-bit mode (Note 4-1-2) (Note 4-1-2)	1.8 to 5.5			$(1/3)t\text{CYC} + 0.08$	μs	
			tdD0(2)						$1t\text{CYC} + 0.08$		
			tdD0(3)						$(1/3)t\text{CYC} + 0.08$		

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 5.

2. SIO1 Serial I/O Characteristics (Note 4-2-1)

Parameter			Symbol	Pin/ Remarks	Conditions	$V_{DD}[\text{V}]$	Specification				
Serial clock	Input clock	Frequency	tSCK(3)	SCK1(P15)	See Fig. 5.		2			tCYC	
		Low level pulse width	tSCKL(3)		1.8 to 5.5	1					
		High level pulse width	tSCKH(3)			1					
	Output clock	Frequency	tSCK(4)	SCK1(P15)	• CMOS output selected • See Fig. 5.	1.8 to 5.5	2			tSCK	
		Low level pulse width	tSCKL(4)				1/2				
		High level pulse width	tSCKH(4)				1/2				
Serial input	Data setup time		tsDI(2)	SB1(P14), SI1(P14)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 5.	1.8 to 5.5	0.05			μs	
	Data hold time		thDI(2)				0.05				
Serial output	Output delay time		tdD0(4)	SO1(P13), SB1(P14)	• Must be specified with respect to falling edge of SIOCLK. • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig. 5.	1.8 to 5.5			$(1/3)t\text{CYC} + 0.08$		

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

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Pulse Input Conditions at $T_a = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{SS1} = V_{SS2} = 0\text{V}$

Parameter	Symbol	Pin/Remarks	Conditions	Specification			
				$V_{DD}[\text{V}]$	min	typ	max
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71), INT2(P72), INT4(P20 to P21), INT5(P30 to P31)	<ul style="list-style-type: none"> • Interrupt source flag can be set. • Event inputs for timer 0 or 1 are enabled. 	1.8 to 5.5	1		
	tPIH(2) tPIL(2)	INT3(P73) when noise filter time constant is 1/1	<ul style="list-style-type: none"> • Interrupt source flag can be set. • Event inputs for timer 0 are enabled. 	1.8 to 5.5	2		
	tPIH(3) tPIL(3)	INT3(P73) when noise filter time constant is 1/32	<ul style="list-style-type: none"> • Interrupt source flag can be set. • Event inputs for timer 0 are enabled. 	1.8 to 5.5	64		
	tPIH(4) tPIL(4)	INT3(P73) when noise filter time constant is 1/128	<ul style="list-style-type: none"> • Interrupt source flag can be set. • Event inputs for timer 0 are enabled. 	1.8 to 5.5	256		
	tPIL(5)	$\overline{\text{RES}}$	• Resetting is enabled.	1.8 to 5.5	200		μs

AD Converter Characteristics at $V_{SS1} = V_{SS2} = 0V$

<12bits AD Converter Mode/Ta = -40°C to +85°C >

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD} [V]	min	typ	max	unit
Resolution	N	AN0(P00) to AN6(P06), AN8(P70), AN9(P71)	2.4 to 5.5			12		bit
Absolute accuracy	ET		(Note 6-1)	3.0 to 5.5			± 16	LSB
			(Note 6-1) • Ta=-10 to +50°C	2.4 to 3.6			± 20	
Conversion time	TCAD		• See Conversion time calculation formulas. (Note 6-2)	4.0 to 5.5	32		115	μs
				3.0 to 5.5	64		115	
Analog input voltage range	VAIN		• See Conversion time calculation formulas. (Note 6-2) • Ta=-10 to +50°C	2.4 to 3.6	410		425	μA
	IAINH			2.4 to 5.5	V_{SS}		V_{DD}	
Analog port input current	IAINL		VAIN= V_{DD}	2.4 to 5.5			1	μA
			VAIN= V_{SS}	2.4 to 5.5	-1			

<8bits AD Converter Mode/Ta = -40°C to +85°C >

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD} [V]	min	typ	max	unit
Resolution	N	AN0(P00) to AN6(P06), AN8(P70), AN9(P71)	2.4 to 5.5			8		bit
Absolute accuracy	ET		(Note 6-1)	2.4 to 5.5			± 1.5	LSB
			• See Conversion time calculation formulas. (Note 6-2)	4.0 to 5.5	20		90	
Conversion time	TCAD			3.0 to 5.5	40		90	μs
			• See Conversion time calculation formulas. (Note 6-2) • Ta=-10 to +50°C	2.4 to 3.6	250		265	
Analog input voltage range	VAIN			2.4 to 5.5	V_{SS}		V_{DD}	V
	IAINH		VAIN= V_{DD}	2.4 to 5.5			1	μA
Analog port input current	IAINL		VAIN= V_{SS}	2.4 to 5.5	-1			

Conversion time calculation formulas:

12bits AD Converter Mode: TCAD(Conversion time) = ((52/(AD division ratio))+2)×(1/3)×tCYC

8bits AD Converter Mode: TCAD(Conversion time) = ((32/(AD division ratio))+2)×(1/3)×tCYC

External oscillation (FmCF)	Operating supply voltage range (V_{DD})	System division ratio (SYSDIV)	Cycle time (tCYC)	AD division ratio (ADDIV)	AD conversion time (TCAD)	
					12bit AD	8bit AD
CF-12MHz	4.0V to 5.5V	1/1	250ns	1/8	34.8 μs	21.5 μs
	3.0V to 5.5V	1/1	250ns	1/16	69.5 μs	42.8 μs
CF-10MHz	4.0V to 5.5V	1/1	300ns	1/8	41.8 μs	25.8 μs
	3.0V to 5.5V	1/1	300ns	1/16	83.4 μs	51.4 μs
CF-4MHz	3.0V to 5.5V	1/1	750ns	1/8	104.5 μs	64.5 μs
	2.4V to 3.6V	1/1	750ns	1/32	416.5 μs	256.5 μs

Note 6-1: The quantization error ($\pm 1/2$ LSB) must be excluded from the absolute accuracy. The absolute accuracy must be measured in the microcontroller's state in which no I/O operations occur at the pins adjacent to the analog input channel.

Note 6-2: The conversion time refers to the period from the time an instruction for starting a conversion process till the time the conversion results register(s) are loaded with a complete digital conversion value corresponding to the analog input value.

The conversion time is 2 times the normal-time conversion time when:

- The first AD conversion is performed in the 12-bit AD conversion mode after a system reset.
- The first AD conversion is performed after the AD conversion mode is switched from 8-bit to 12-bit conversion mode.

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Power-on Reset (POR) Characteristics at $T_a = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{SS1}=V_{SS2}=0\text{V}$

Parameter	Symbol	Pin/Remarks	Conditions	Specification			
				Option selected voltage	min	typ	max
POR release voltage	PORRL		• Select from option. (Note 7-1)	1.67V	1.55	1.67	1.79
				1.97V	1.85	1.97	2.09
				2.07V	1.95	2.07	2.19
				2.37V	2.25	2.37	2.49
				2.57V	2.45	2.57	2.69
				2.87V	2.75	2.87	2.99
				3.86V	3.73	3.86	3.99
				4.35V	4.21	4.35	4.49
Detection voltage unknown state	POUKS		• See Fig. 7. (Note 7-2)			0.7	0.95
Power supply rise time	PORIS		• Power supply rise time from 0V to 1.6V.			100	ms

Note7-1: The POR release level can be selected out of 8 levels only when the LVD reset function is disabled.

Note7-2: POR is in an unknown state before transistors start operation.

Low Voltage Detection Reset (LVD) Characteristics at $T_a = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{SS1}=V_{SS2}=0\text{V}$

Parameter	Symbol	Pin/Remarks	Conditions	Specification			
				Option selected voltage	min	typ	max
LVD reset Voltage (Note 8-2)	LVDET		• Select from option. (Note 8-1) (Note 8-3) • See Fig. 8.	1.91V	1.81	1.91	2.01
				2.01V	1.91	2.01	2.11
				2.31V	2.21	2.31	2.41
				2.51V	2.41	2.51	2.61
				2.81V	2.71	2.81	2.91
				3.79V	3.69	3.79	3.89
				4.28V	4.18	4.28	4.38
LVD hysteresys width	LVHYS			1.91V		55	
				2.01V		55	
				2.31V		55	
				2.51V		55	
				2.81V		60	
				3.79V		65	
				4.28V		65	
Detection voltage unknown state	LVUKS		• See Fig. 8. (Note 8-4)			0.7	0.95
Low voltage detection minimum Width (Reply sensitivity)	TLVDW		• LVDET-0.5V • See Fig. 9.		0.2		

Note8-1: The LVD reset level can be selected out of 7 levels only when the LVD reset function is enabled.

Note8-2: LVD reset voltage specification values do not include hysteresis voltage.

Note8-3: LVD reset voltage may exceed its specification values when port output state changes and/or when a large current flows through port.

Note8-4: LVD is in an unknown state before transistors start operation.

Consumption Current Characteristics at $T_a = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{SS1} = V_{SS2} = 0\text{V}$

Parameter	Symbol	Pin/ Remarks	Conditions	Specification					
				$V_{DD}[\text{V}]$	min	typ	max	unit	
Normal mode consumption current (Note 9-1) (Note 9-2)	IDDOP(1)	V _{DD1}	<ul style="list-style-type: none"> • FmCF=12MHz ceramic oscillation mode • System clock set to 12MHz side • Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio 	2.7 to 5.5		7.4	13.0	mA	
				2.7 to 3.6		4.4	8.1		
	IDDOP(2)		<ul style="list-style-type: none"> • CF1=24MHz external clock • System clock set to CF1 side • Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio 	3.0 to 5.5		9.7	16.2		
				3.0 to 3.6		5.3	8.7		
	IDDOP(3)		<ul style="list-style-type: none"> • FmCF=10MHz ceramic oscillation mode • System clock set to 10MHz side • Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio 	2.2 to 5.5		6.6	11.9		
				2.2 to 3.6		4.0	7.4		
	IDDOP(4)		<ul style="list-style-type: none"> • FmCF=4MHz ceramic oscillation mode • System clock set to 4MHz side • Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio 	1.8 to 5.5		2.9	6.5		
				1.8 to 3.6		2.2	4.2		
	IDDOP(5)		<ul style="list-style-type: none"> • CF oscillation low amplifier size selected. (CFLAMP=1) • FmCF=4MHz ceramic oscillation mode • System clock set to 4MHz side • Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/4 frequency division ratio 	2.2 to 5.5		1.1	2.5		
				2.2 to 3.6		0.6	1.3		
	IDDOP(6)		<ul style="list-style-type: none"> • FsX'tal=32.768kHz crystal oscillation mode • Internal low speed RC oscillation stopped. • System clock set to internal medium speed RC oscillation. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio 	1.8 to 5.5		0.6	1.7	μA	
				1.8 to 3.6		0.3	0.9		
	IDDOP(7)		<ul style="list-style-type: none"> • FsX'tal=32.768kHz crystal oscillation mode • Internal low speed and medium speed RC oscillation stopped. • System clock set to 8MHz with frequency variable RC oscillation • 1/1 frequency division ratio 	2.7 to 5.5		5.0	9.1		
				2.7 to 3.6		3.6	5.8		
	IDDOP(8)		<ul style="list-style-type: none"> • External FsX'tal and FmCF oscillation stopped. • System clock set to internal low speed RC oscillation. • Internal medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio 	1.8 to 5.5		75	370		
				1.8 to 3.6		46	192		
	IDDOP(9)		<ul style="list-style-type: none"> • External FsX'tal and FmCF oscillation stopped. • System clock set to internal low speed RC oscillation. • Internal medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio • $T_a = -10$ to $+50^{\circ}\text{C}$ 	5.0		75	176		
				3.3		46	115		
				2.5		35	85		

Note9-1: Values of the consumption current do not include current that flows into the output transistors and internal pull-up resistors.

Note9-2: The consumption current values do not include operational current of LVD function if not specified.

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Parameter	Symbol	Pin/ Remarks	Conditions	Specification					
				V _{DD} [V]	min	typ	max		
Normal mode consumption current (Note 9-1) (Note 9-2)	IDDOP(10)	V _{DD} 1	<ul style="list-style-type: none"> • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio 	1.8 to 5.5		38	139	μA	
				1.8 to 3.6		15	66		
	IDDOP(11)		<ul style="list-style-type: none"> • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio • Ta=-10 to +50°C 	5.0		38	101		
				3.3		15	46		
				2.5		9.0	28		
	HALT mode consumption current (Note 9-1) (Note 9-2)		<ul style="list-style-type: none"> • HALT mode • FmCF=12MHz ceramic oscillation mode • System clock set to 12MHz side • Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio 	2.7 to 5.5		3.1	5.6	mA	
				2.7 to 3.6		1.6	2.9		
				3.0 to 5.5		4.9	8.6		
	IDDHALT(2)		<ul style="list-style-type: none"> • HALT mode • CF1=24MHz external clock • System clock set to CF1 side • Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio 	3.0 to 3.6		2.3	3.8		
				2.2 to 5.5		2.7	5.3		
				2.2 to 3.6		1.4	2.6		
	IDDHALT(3)		<ul style="list-style-type: none"> • HALT mode • FmCF=10MHz ceramic oscillation mode • System clock set to 10MHz side • Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio 	1.8 to 5.5		1.4	3.5		
				1.8 to 3.6		0.7	1.3		
	IDDHALT(4)		<ul style="list-style-type: none"> • HALT mode • FmCF=4MHz ceramic oscillation mode • System clock set to 4MHz side • Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio 	2.2 to 5.5		0.7	1.8		
				2.2 to 3.6		0.3	0.7		
	IDDHALT(5)		<ul style="list-style-type: none"> • HALT mode • CF oscillation low amplifier size selected. (CFLAMP=1) • FmCF=4MHz ceramic oscillation mode • System clock set to 4MHz side • Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/4 frequency division ratio 	1.8 to 5.5		0.4	1.1		
				1.8 to 3.6		0.2	0.5		
	IDDHALT(6)								

Note9-1: Values of the consumption current do not include current that flows into the output transistors and internal pull-up resistors.

Note9-2: The consumption current values do not include operational current of LVD function if not specified.

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Parameter	Symbol	Pin/ remarks	Conditions	Specification					
				V _{DD} [V]	min	typ	max		
HALT mode consumption current (Note 9-1) (Note 9-2)	IDDHALT(7)	V _{DD} 1	<ul style="list-style-type: none"> • HALT mode • FsX'tal=32.768kHz crystal oscillation mode • Internal low speed and medium speed RC oscillation stopped. • System clock set to 8MHz with frequency variable RC oscillation • 1/1 frequency division ratio 	2.7 to 5.5		1.8	3.5	μA	
				2.7 to 3.6		1.1	2.0		
	IDDHALT(8)		<ul style="list-style-type: none"> • HALT mode • External FsX'tal and FmCF oscillation stopped. • System clock set to internal low speed RC oscillation. • Internal medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio 	1.8 to 5.5		23	260		
				1.8 to 3.6		13	119		
	IDDHALT(9)		<ul style="list-style-type: none"> • HALT mode • External FsX'tal and FmCF oscillation stopped. • System clock set to internal low speed RC oscillation. • Internal medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio • Ta=-10 to +50°C 	5.0		23	65		
				3.3		13	35		
				2.5		9.2	25		
	IDDHALT(10)		<ul style="list-style-type: none"> • HALT mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio 	1.8 to 5.5		25	112		
				1.8 to 3.6		8.5	56		
	IDDHALT(11)		<ul style="list-style-type: none"> • HALT mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio • Ta=-10 to +50°C 	5.0		25	69		
				3.3		8.5	29		
				2.5		4.2	15		
HOLD mode consumption current (Note 9-1) (Note 9-2)	IDDHOLD(1)	V _{DD} 1	HOLD mode <ul style="list-style-type: none"> • CF1=V_{DD} or open (External clock mode) 	1.8 to 5.5		0.04	30	μA	
				1.8 to 3.6		0.02	21		
	IDDHOLD(2)		HOLD mode <ul style="list-style-type: none"> • CF1=V_{DD} or open (External clock mode) • Ta=-10 to +50°C 	5.0		0.04	2.3		
				3.3		0.02	1.5		
				2.5		0.017	1.2		
	IDDHOLD(3)		HOLD mode <ul style="list-style-type: none"> • CF1=V_{DD} or open (External clock mode) • LVD option selected 	1.8 to 5.5		3.2	35		
				1.8 to 3.6		2.7	24		
	IDDHOLD(4)		HOLD mode <ul style="list-style-type: none"> • CF1=V_{DD} or open (External clock mode) • Ta=-10 to +50°C • LVD option selected 	5.0		3.2	6.5		
				3.3		2.7	4.5		
				2.5		2.5	4.2		
Timer HOLD mode consumption current (Note 9-1) (Note 9-2)	IDDHOLD(5)	V _{DD} 1	Timer HOLD mode <ul style="list-style-type: none"> • FsX'tal=32.768 kHz crystal oscillation mode 	1.8 to 5.5		22	106	μA	
				1.8 to 3.6		7.5	45		
	IDDHOLD(6)		Timer HOLD mode <ul style="list-style-type: none"> • FsX'tal=32.768 kHz crystal oscillation mode • Ta=-10 to +50°C 	5.0		22	62		
				3.3		7.5	23		
				2.5		2.9	12		

Note9-1: Values of the consumption current do not include current that flows into the output transistors and internal pull-up resistors.

Note9-2: The consumption current values do not include operational current of LVD function if not specified.

F-ROM Programming Characteristics at $T_a = +10^{\circ}\text{C}$ to $+55^{\circ}\text{C}$, $V_{SS1} = V_{SS2} = 0\text{V}$

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				$V_{DD}[\text{V}]$	min	typ	max	
Onboard programming current	IDDFW(1)	V_{DD1}	• Only current of the Flash block.	2.2 to 5.5		5	10	mA
Programming time	tFW(1)		• Erasing time	2.2 to 5.5		20	30	ms
	tFW(2)		• Programming time			40	60	μs

UART (Full Duplex) Operating Conditions at $T_a = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{SS1} = V_{SS2} = 0\text{V}$

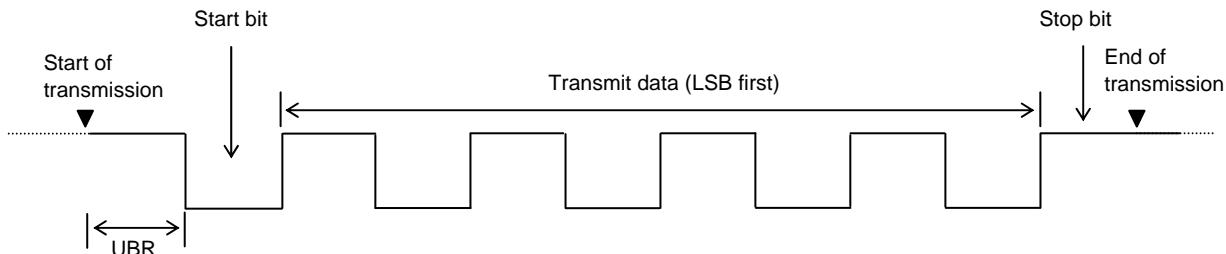
Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				$V_{DD}[\text{V}]$	min	typ	max	
Transfer rate	UBR	UTX(P20) URX(P21)		1.8 to 5.5	16/3		8192/3	tCYC

Data length: 7/8/9 bits (LSB first)

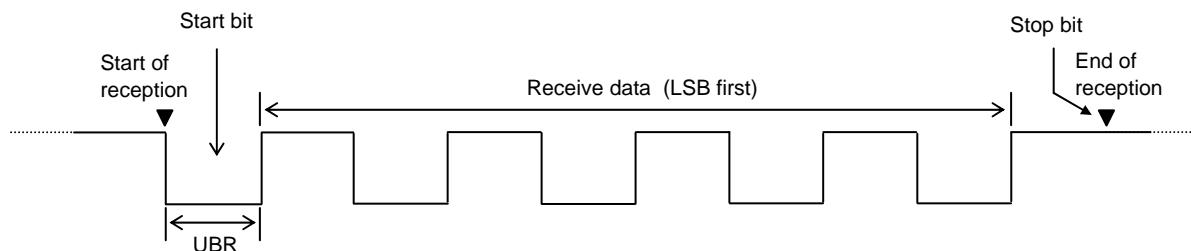
Stop bits: 1 bit (2-bit in continuous data transmission)

Parity bits: None

Example of Continuous 8-bit Data Transmission Mode Processing (First Transmit Data=55H)



Example of Continuous 8-bit Data Reception Mode Processing (First Receive Data=55H)



LC87F2H08A

Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator

- CF oscillation normal amplifier size selected (CFLAMP=0)

■MURATA

Nominal Frequency	Type	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf [Ω]	Rd [Ω]		typ [ms]	max [ms]	
12MHz	SMD	CSTCE12M0G52-R0	(10)	(10)	Open	1.0k	2.7 to 5.5	0.1	0.5	Internal C1,C2
10MHz	SMD	CSTCE10M0G52-R0	(10)	(10)	Open	680	2.2 to 3.6	0.1	0.5	
					Open	1.0k	2.3 to 5.5	0.1	0.5	
8MHz	LEAD	CSTLS10M0G53-B0	(15)	(15)	Open	1.0k	2.5 to 5.5	0.1	0.5	
					Open	1.5k	2.2 to 5.5	0.1	0.5	
6MHz	LEAD	CSTLS8M00G53-B0	(15)	(15)	Open	1.5k	2.2 to 5.5	0.1	0.5	
					Open	2.2k	2.2 to 5.5	0.1	0.5	
4MHz	SMD	CSTCR6M00G53-R0	(15)	(15)	Open	1.5k	1.8 to 2.7	0.2	0.6	
					Open	3.3k	1.9 to 5.5	0.2	0.6	
	LEAD	CSTLS4M00G53-B0	(15)	(15)	Open	3.3k	1.9 to 5.5	0.2	0.6	

- CF oscillation low amplifier size selected (CFLAMP=1)

■MURATA

Nominal Frequency	Type	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf [Ω]	Rd [Ω]		Typ [ms]	Max [ms]	
4MHz	SMD	CSTCR4M00G53-R0	(15)	(15)	Open	1.0k	2.1 to 2.7	0.2	0.6	Internal C1,C2
					Open	2.2k	2.5 to 5.5	0.2	0.6	
	LEAD	CSTCR4M00G53095-R0	(15)	(15)	Open	1.0k	1.9 to 2.7	0.2	0.7	
					Open	1.0k	2.2 to 2.7	0.2	0.6	
		CSTLS4M00G53-B0	(15)	(15)	Open	2.2k	2.5 to 5.5	0.2	0.6	
					Open	1.0k	2.0 to 2.7	0.2	0.7	

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after VDD goes above the operating voltage lower limit (see Figure 3).

Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Oscillator

■EPSON TOYOCOM

Nominal Frequency	Type	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf [Ω]	Rd [Ω]		typ [s]	max [s]	
32.768kHz	SMD	MC-306	9	9	Open	330k	1.8 to 5.5	1.4	4.0	Applicable CL value = 7.0pF

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillation circuit is executed and to the time interval that is required for the oscillation to get stabilized after the HOLD mode is reset (see Figure 3):

Note: The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

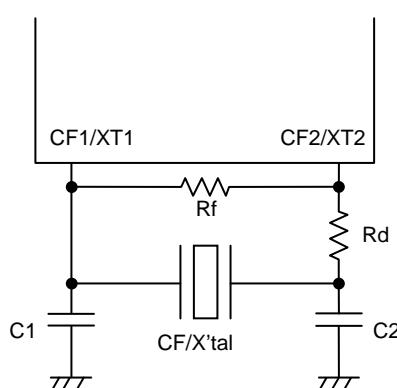


Figure 1 CF and XT Oscillator Circuit

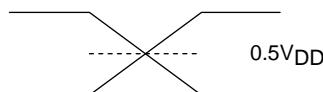
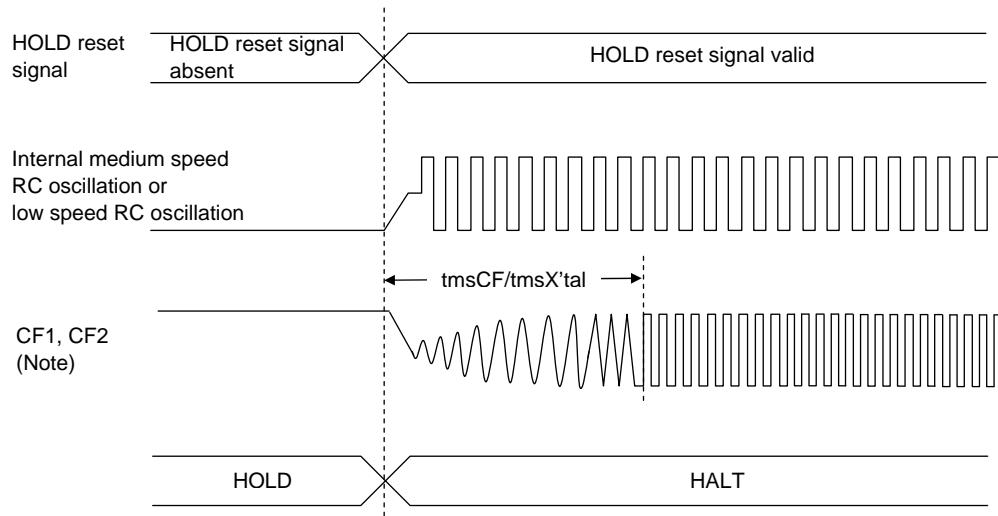
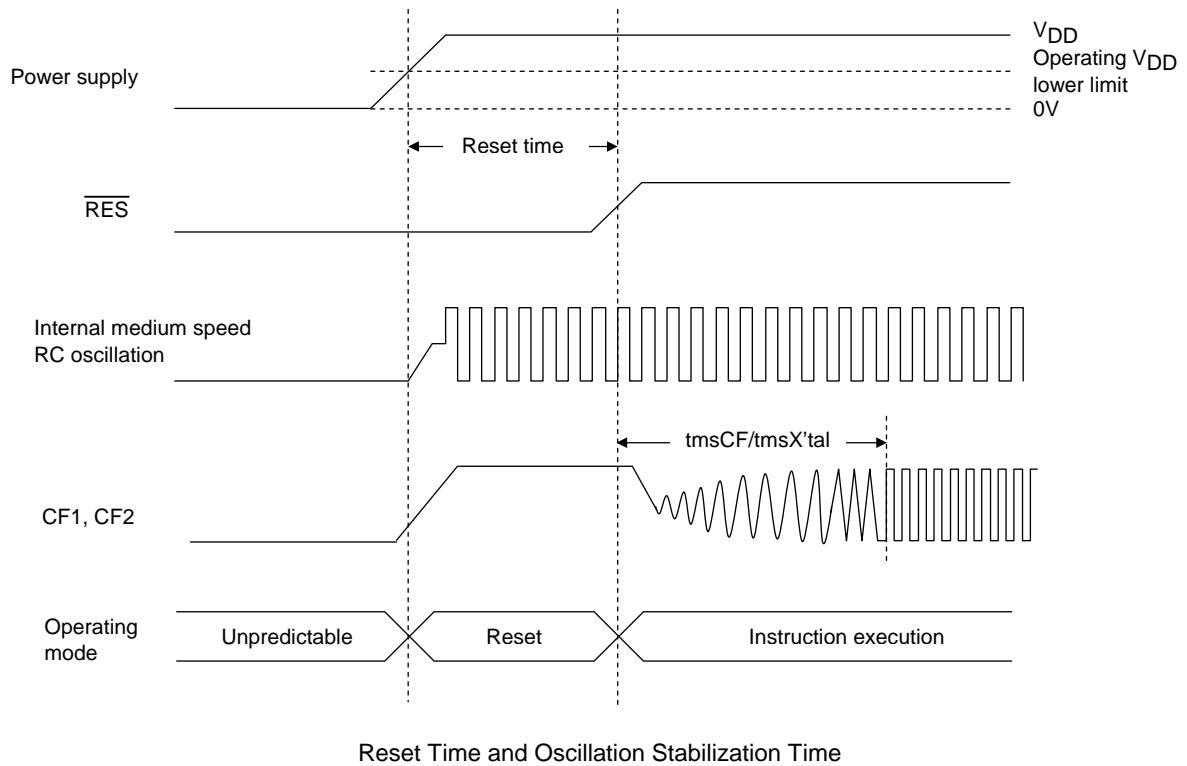


Figure 2 AC Timing Measurement Point



Note: External oscillation circuit is selected.

Figure 3 Oscillation Stabilization Times

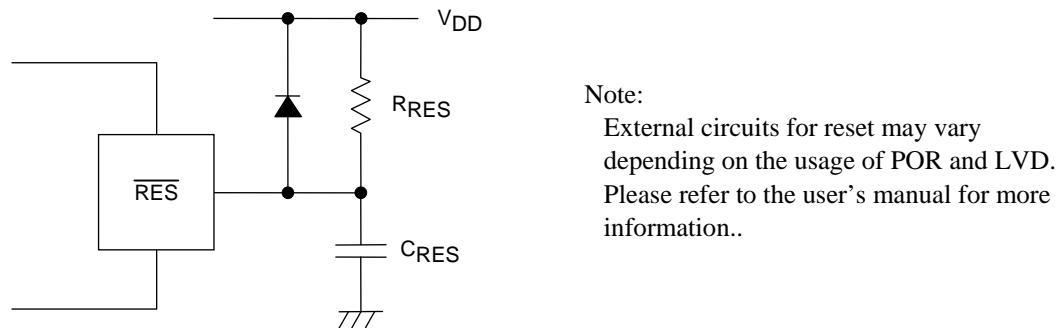


Figure 4 Reset Circuit

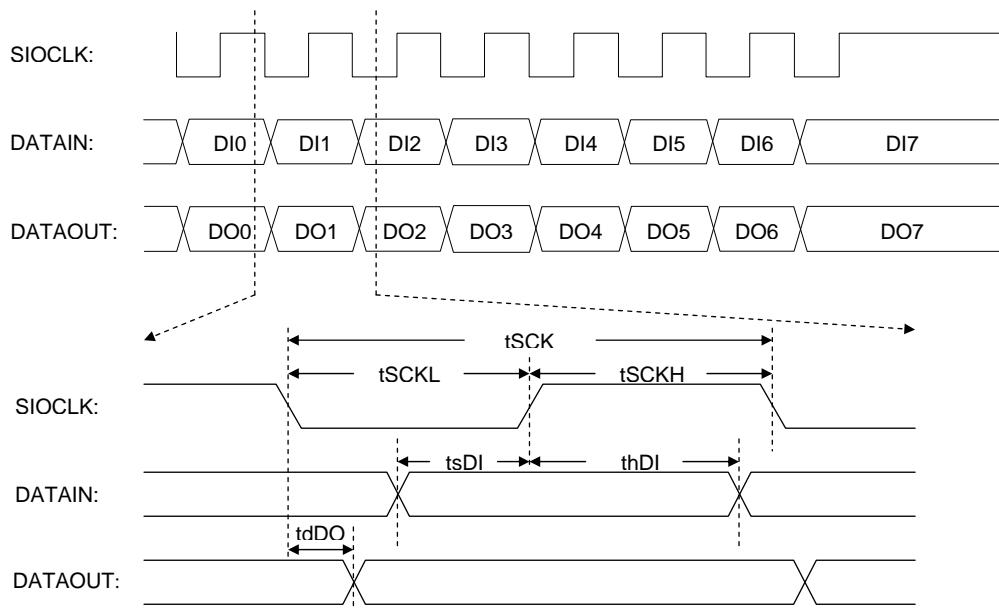


Figure 5 Serial I/O Output Waveforms

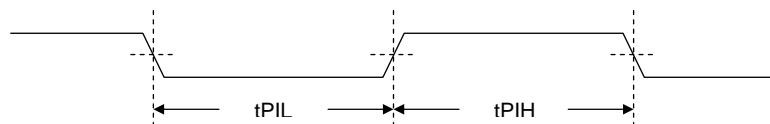


Figure 6 Pulse Input Timing Signal Waveform

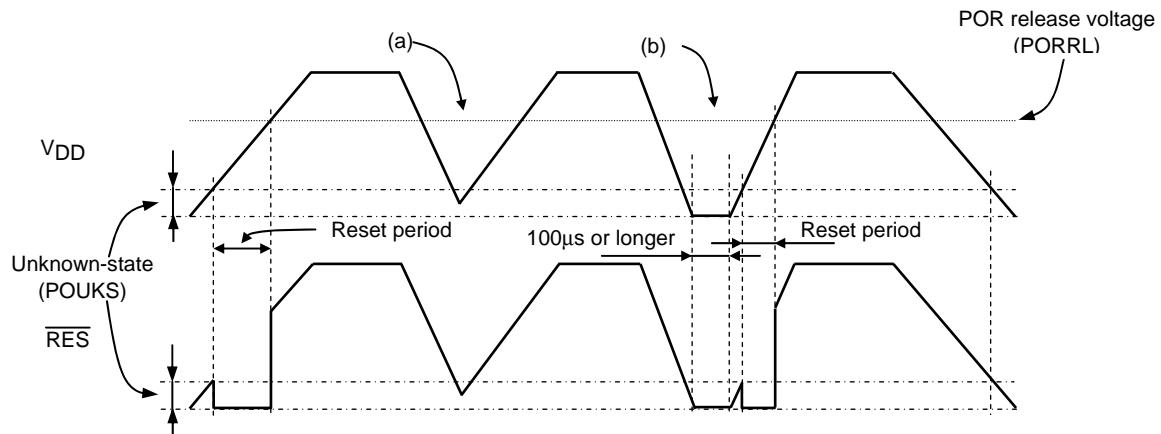


Figure 7 Waveform observed when only POR is used (LVD not used)
(RESET pin: Pull-up resistor RRES only)

- The POR function generates a reset only when power is turned on starting at the V_{SS} level.
- No stable reset will be generated if power is turned on again when the power level does not go down to the V_{SS} level as shown in (a). If such a case is anticipated, use the LVD function together with the POR function or implement an external reset circuit.
- A reset is generated only when the power level goes down to the V_{SS} level as shown in (b) and power is turned on again after this condition continues for 100µs or longer.

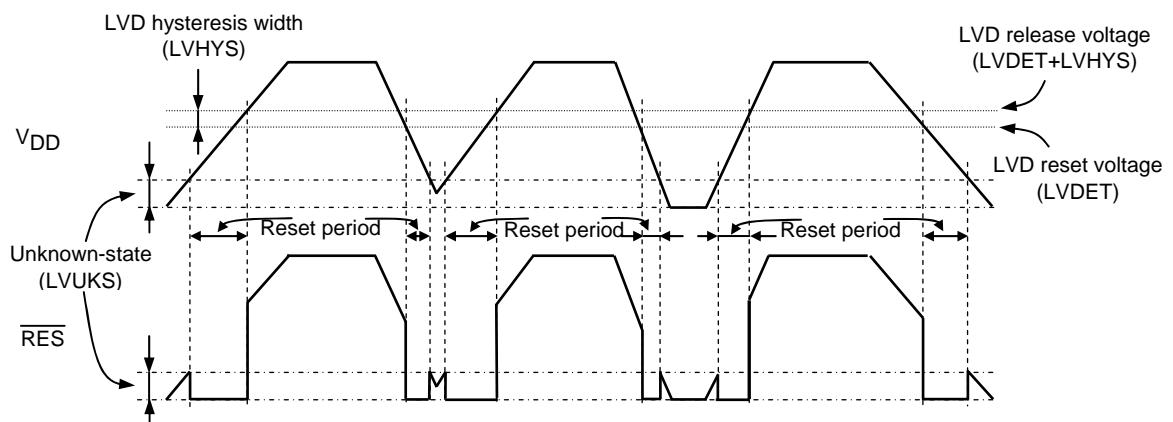


Figure 8 Waveform observed when both POR and LVD functions are used
(RESET pin: Pull-up resistor RRES only)

- Resets are generated both when power is turned on and when the power level lowers.
- A hysteresis width (LVHYS) is provided to prevent the repetitions of reset release and entry cycles near the detection level.

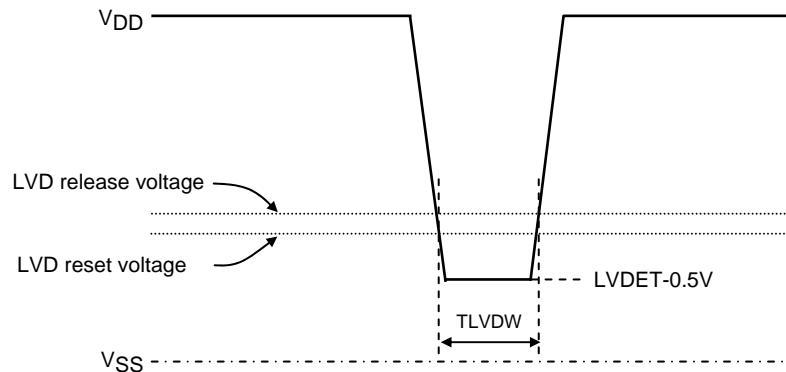


Figure 9 Low voltage detection minimum width
(Example of momentary power loss/Voltage variation waveform)

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