DS26303DK
3.3V, E1/T1/J1, Short-Haul, Octal LIU Design Kit

www.maxim-ic.com

GENERAL DESCRIPTION

The DS26303DK is a fully integrated design kit for the DS26303 3.3V, 8-port, E1/T1/J1 line interface unit (LIU). This design kit contains all the necessary circuitry to evaluate the DS26303 in all modes of operation. The design kit also includes an on-board microprocessor to run real-time code for further part evaluation.

DESIGN KIT CONTENTS

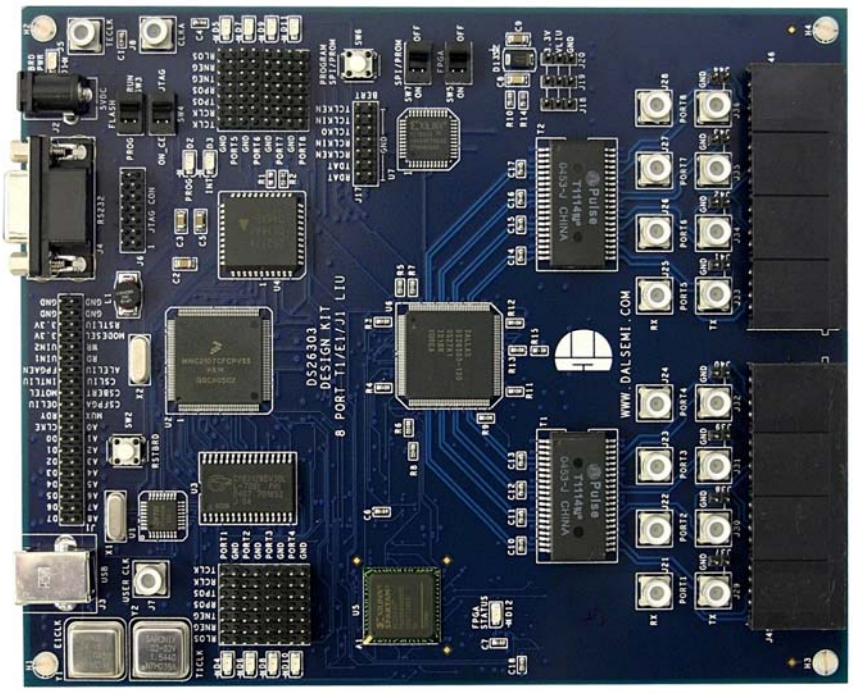
DS26303DK Board
5V AC/DC Adapter
3ft USB Cable
Download:
- ChipView Software
- DS26303DK.def Definition Files
- DS26303DK Data Sheet

ORDERING INFORMATION

PART	DESCRIPTION
DS26303DK	DS26303 Design Kit Board

FEATURES

- **Expedites New Designs by Eliminating First-Pass Prototyping**
- **Demonstrates Key Functions of the DS26303**
- **Includes DS26303 x 8-Port LIU, Transformers, 75Ω BNC Connectors, RJ-48 Connectors, and Termination Passives**
- **Communicates Directly with any PC with a USB or RS-232 Serial Interface**
- **High-Level Windows®-Based Software Provides Visual Access to All Registers**
- **Software-Controlled (Register) Mapped Configuration Switches Facilitate Real-Time Clock and Signal Routing**
- **Precision Test Points for All Clocks and Signals**
- **On-Board T1 and E1 Crystal Oscillators for Stable Clock Generation**
- **On-Board BERT for Testing and Pattern Generation**



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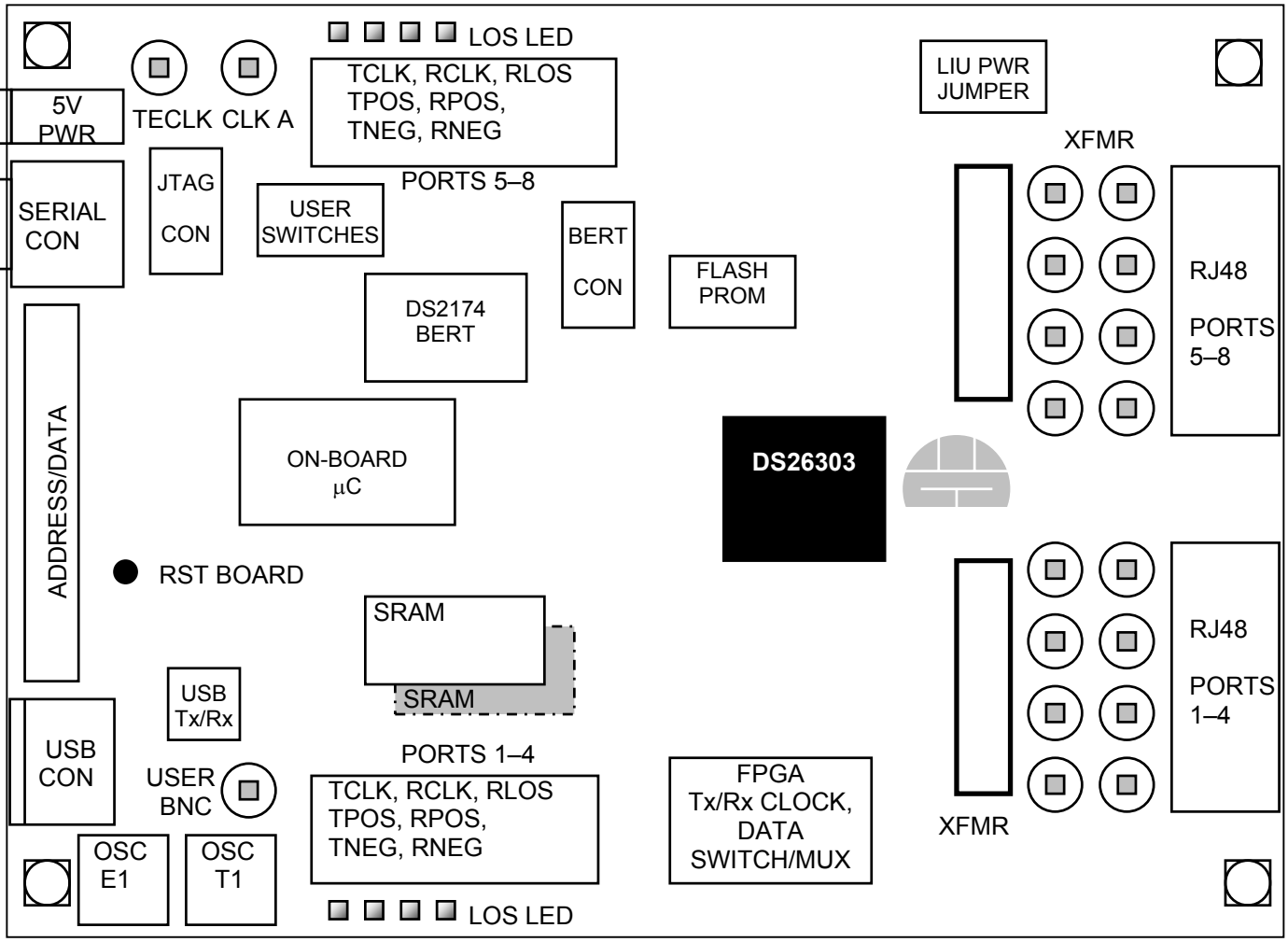
COMPONENT LIST

DESIGNATION	QTY	DESCRIPTION	SUPPLIER/ PART NUMBER
C1, C4, C6, C7, C18, C24, C26, C34, C36, C37, C38, C41, C43–C47, C49, C50, C51, C53–C59, C61–C83, C85, C86, C90	53	0.1µF ±20%, 16V X7R ceramic capacitors (0603)	AVX 0603YC104MAT
C2, C3, C22, C30, C35, C40, C42, C48, C52, C60, C84, C88, C89	13	1µF ±10%, 16V ceramic capacitors (1206)	Panasonic ECJ-3YB1C105K
C5, C9, C19, C21, C27, C28, C87	7	10µF ±20%, 10V ceramic capacitors (1206)	Panasonic ECJ-3YB1A106M
C8	1	6.8µF ±10%, 6.3V X5R ceramic capacitor (1206)	Panasonic ECJ-3YB0J685K
C10–C17	8	470pF ±10%, 100V ceramic capacitors (0603)	Panasonic ECJ-1VB2A471K
C20, C23, C25, C91, C92	5	68µF ±20%, 16V tantalum capacitors (D case)	Panasonic ECS-T1CD686R
C29, C31, C39	3	22pF ±5%, 25V ceramic capacitors (0603)	AVX 06033A220JAT
C32, C33	2	10pF ±5%, 50V ceramic capacitors (1206) (tall case)	Phycomp 1206CG100J9B200
D1, D12	2	Green LEDs (SMD)	Panasonic LN1351C
D2–D11	10	Red LEDs (SMD)	Panasonic LN1251C
D13, D14, D15	3	1A, 40V Schottky diodes	International Rectifier 10BQ040
H1–H4	4	KIT, 4-40 hardware 0.75 nylon standoff and 0.25 nylon screw	Not applicable 4-40KIT2
J1	1	40-pin terminal strip (dual row, vertical)	Samtec TSW-120-07-T-D
J2	1	2.1mm/5.5mm connector Power jack, right-angle PC board mount; closed frame, high current, 24V DC at 5A	CUI, Inc. PJ-002AH
J3	1	Black, single right angle (Type B)	Molex Not applicable
J4	1	DB9 right-angle connector (short case)	AMP 788750-2
J5, J7, J8, J21–J36	19	5-pin SMB connectors 50Ω, vertical, gold	AMP 413990-1
J6, J9–J17	10	14-pin headers (dual row, vertical)	Samtec TSW-107-14-T-D
J18, J19, J20	3	100-mil 3-position jumpers	Samtec Not applicable
J37–J44	8	2-pin headers, 0.100in centers (vertical)	Samtec TSW-102-07-T-S
J45, J46	2	8-pin 4-port RJ45 jacks (right angle)	Molex 43223-8140
L1	1	1.0µH ±20%, 2-pin SMT inductor	Coiltronics UP1B-1R0

DESIGNATION	QTY	DESCRIPTION	SUPPLIER/ PART NUMBER
R1, R58, R87	3	Resistors (0603) **DO NOT POPULATE**	—
R2, R14–R26, R28, R32–R43, R46–R50, R52, R54–R57, R63–R66, R68, R69, R71, R72, R73, R76, R77, R82, R85, R86, R88, R91, R93, R96, R97, R130	57	10kΩ ±5%, 1/16W resistors (0603)	Panasonic ERJ-3GEYJ103V
R3–R9, R11, R12, R13, R29, R31, R44, R45, R60, R61, R62, R78, R79, R94, R95, R98–R102, R104, R117, R120, R121, R124–R129	36	33Ω ±5%, 1/16W resistors (0603)	Panasonic ERJ-3GEYJ330V
R10	1	22kΩ ±5%, 1/16W resistor (0603)	Panasonic ERJ-3GEYJ223V
R27, R67, R70, R74, R75, R80, R81, R83, R84, R89, R90, R123	12	330Ω ±5%, 1/16W resistors (0603)	Panasonic ERJ-3GEYJ331V
R30, R59	2	15kΩ ±5%, 1/16W resistors (0603)	Panasonic ERJ-3GEYJ153V
R51	1	Resistor (1206) **DO NOT POPULATE**	—
R53	1	470Ω ±5%, 1/16W resistor (0603)	Panasonic ERJ-3GEYJ471V
R92	1	51Ω ±5%, 1/16W resistor (0603)	Panasonic ERJ-3GEYJ510V
R103, R105–R116, R118, R119, R122	16	60.4Ω ±1%, 1/16W resistors (0603)	Panasonic ERJ-3EKF60R4V
SW2, SW6	2	4-pin single-pole switch	Panasonic EVQPAE04M
SW3, SW4, SW5, SW7	4	6-pin slide switches (DPDT, through hole)	Tyco Electronics SSA22
T1, T2	2	Transformers (1:2 count transmitter/1:1 count receiver) (40-pin wide SO, -40°C to +85°C)	Pulse Engineering T1114
U1	1	8-bit FIFO USB UART (32-pin LQFP)	FTDI FT245BM
U2	1	MCORE Microcontroller (144-pin LQFP)	Motorola MMC2107PV
U3, U11	2	128k x 8 SRAM (32-pin SO)	Cypress CY62128VL-70SC
U4	1	DS2174 EBERT (44-pin PLCC, 0°C to +70°C)	Dallas Semiconductor DS2174Q
U5	1	Spartan-II 2.5V FPGA, 200k gate (256-pin BGA)	Xilinx XC2S200-5FG256C
U6	1	3.3V, E1/T1/J1 long-haul octal LIU (144-pin eLQFP, 0°C to +70°C)	Dallas Semiconductor DS26303L

DESIGNATION	QTY	DESCRIPTION	SUPPLIER/ PART NUMBER
U7	1	PROM for FPGA (44-pin TQFP)	Xilinx XC18V02VQ44C
U8	1	Dual RS-232 transmitter/receiver (150-mil, 16-pin SO)	Dallas Semiconductor DS232AR
U9, U12	2	High-speed buffers	Fairchild Semiconductor NC7SZ86
U10, U18	2	1.5W, 3.3V or adj, 1A linear regulators (16-pin TSSOP-EP)	Maxim MAX1793EUE-33
U13, U15	2	Hex inverters (14-pin SO)	Toshiba TC74HC04AFN
U14	1	Quad 2-input NAND gate (14-pin SO)	Toshiba TC74HC00AFN
U16	1	Switch debouncer (4-pin SOT143)	Maxim MAX6816EUS-T
U17	1	2.5V or adj linear regulator (8-pin μMAX/SO)	Maxim MAX1792EUA25
U19	1	Platform flash in-system programmable configuration PROM (2Mb, 20-pin TSSOP)	Xilinx XCF02SVO20C
X1	1	6.00MHz low-profile crystal	Pletronics LP49-26-6.00M
X2	1	8.000MHz low-profile crystal	Ecliptek Corp. EC1-8.000M
Y1	1	Oscillator, crystal clock 5V, 2.048MHz	SaRonix NTH039A-2.0480
Y2	1	Oscillator, crystal clock 5V, 1.544MHz	SaRonix NTH039A-1.5440

BOARD FLOORPLAN



BASIC OPERATION

This design kit relies upon several supporting files, which are available for downloading on our website at www.maxim-ic.com/DS26303DK.

The support files are used with an evaluation program called ChipView, which is available for download at www.maxim-ic.com/telecom.

HARDWARE CONFIGURATION

Quick Start (Hardware Settings—Single Power Supply)

- For single power-supply operation, short jumpers J18, J19, and J20 between the 3.3V pin and the VLIU pin. This connects VDD of the DS26303 to the 3.3V supply on the design kit.
- Ensure that the FLASH switch (SW3) is in the *RUN* position.
- Ensure that the FPGA switch (SW5) is in the *ON* position.
- Ensure that the SPI/PROM switch (SW7) is in the *OFF* position.
- If using the serial port, connect a RS-232 serial cable from DS26303DK (J4) to the PC.
- If using the USB port, connect a USB cable from DS26303DK (J3) to the PC.
- Connect AC/DC adapter with an AC power source and the DS26303DK (J2). PWR LED should be on.

JTAG Configuration

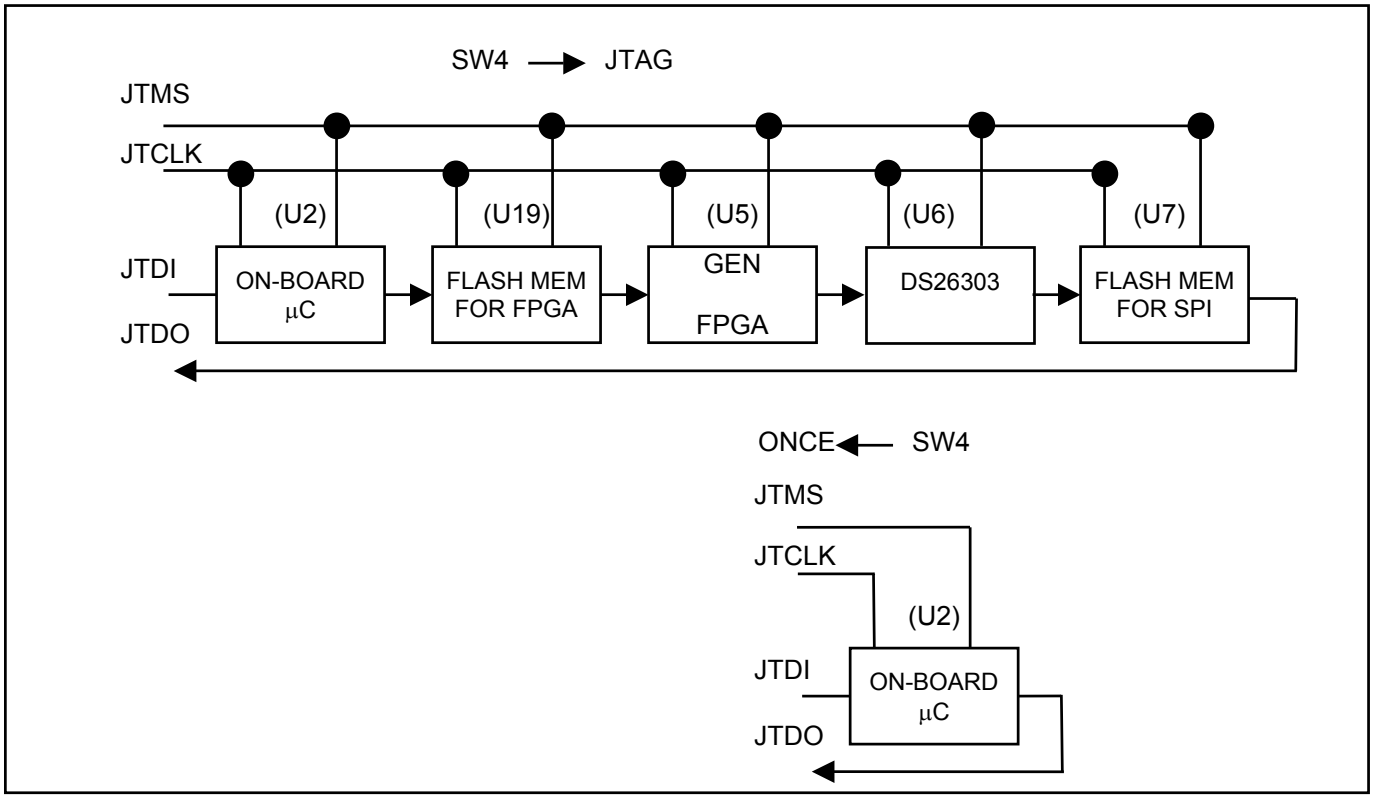
The JTAG chain is controlled by the connector JTAG CON (J6) and two on-board switches: FLASH (SW3) and ONCE/JTAG (SW4). Depending on the function, such as programming the internal microcontroller flash or performing boundary scan operations, the JTAG CON connector can be used and the switches can be configured to accomplish the desired task. For information on programming the internal flash of the on-board microcontroller, refer to the MMC2107 microcontroller user manual and board schematic.

For most purposes, having the complete JTAG chain is sufficient. Figure 1 shows the complete chain as well as what order the devices appear during boundary scan. Table 1 shows the pinout of the JTAG connector. Connect any JTAG cable to the connector to perform all operations. Note the JTAG chain changes depending on the switch SW4. The ONCE location of SW4 is used for programming the on-board microcontroller only.

Table 1. JTAG Connector (J6) Pinout

PIN	NAME
1	JTDI
2, 4, 6, 7	GND
3	JTDO
5	JTCLK
8	ALIGN KEY
9	BRD RST
10	JTMS
11	BRD V3.3
12	JDE
13	N.C.
14	JTRST

Figure 1. DS26303DK JTAG Chain



Address/Data Bus Connector

The DS26303DK has a connector (J1) to monitor all local bus activity for the design kit. All the signals can be captured with a high-impedance probe and displayed on an oscilloscope or logic analyzer. **Note:** If the FPGA switch (SW5) is in the "OFF" position, the on-board microcontroller will no longer drive any data onto the local bus. Therefore, the user can now connect the local bus of the DS26303 into another system without making any modifications to the hardware. See Table 2 for specific pin information for connector J1.

Table 2. Address/Data Connector Pinout

PIN	NAME	FUNCTION		PIN	NAME	FUNCTION
1	A8	Local Address Bit 8		2	D0	Local Data Bit 0
3	A7	Local Address Bit 7		4	D1	Local Data Bit 1
5	A6	Local Address Bit 6		6	D2	Local Data Bit 2
7	A5	Local Address Bit 5		8	D3	Local Data Bit 3
9	A4	Local Address Bit 4		10	D4	Local Data Bit 4
11	A3	Local Address Bit 3		12	D5	Local Data Bit 5
13	A2	Local Address Bit 2		14	D6	Local Data Bit 6
15	A1	Local Address Bit 1		16	D7	Local Data Bit 7
17	A0	Local Address Bit 0		18	CLKE	SPI Clock Edge Select
19	MUX	Mux		20	RDY	Ready Handshake from LIU
21	CSFPGA	Chip Select FPGA		22	OE	Output Enable LIU
23	CSBERT	Chip Select DS2174		24	MOTEL	Motorola/Intel Select
25	CSLIU	Chip Select DS26303		26	INT	Interrupt for DS26303
27	ALELIU	Address Latch Enable		28	FPGAEN	FPGA Enable Pin
29	RD	Read Signal		30	UIN1	User Input 1
31	WR	Write Signal		32	UIN2	User Input 2
33	MODESEL	Mode Select		34, 36	3.3V	Board 3.3V
35	—	Not Used		37–40	GND	Ground

Telecom Clock and Data Test Points

The DS26303DK has high-impedance test points for all the telecom signals that are related to the LIU. These signals are split up by port number and marked with easy to read silkscreen labels. Table 3 shows the telecom connector for port 1. The pinout for this connector is repeated for all 8 ports.

Table 3. Telecom Connector Pinout

PIN	NAME	FUNCTION
1	TCLK	Transmit Clock Input
2, 4, 6, 8, 10, 12, 14	GND	Ground
3	RCLK	Receive Clock Output
5	TPOS	Transmit Positive Data Input
7	RPOS	Receive Positive Data Output
9	TNEG	Transmit Negative Data Input
11	RNEG	Receive Positive Data Output
13	RLOS	Receive Loss-of-Signal Output

Note that the input signals in the telecom connector go from the connector to the on-board FPGA, then to the DS26303. The FPGA was designed to perform specific signal routing functions such as looping back RPOS to TPOS on a particular port or transferring data from the on-board BERT. If you are using user-defined data and drive the signal on the connector, be sure to tri-state the input signal in the FPGA. **FAILURE TO DO SO COULD CAUSE DAMAGE TO THE FPGA**!

On-Board Bit Error-Rate Tester (BERT)

The DS26303DK has an on-board bit error-rate tester (BERT) to generate and detect errors in either pseudorandom or user-defined patterns. The BERT on the DS26303DK is the DS2174. A header for the relevant signals related to the BERT is located on the board (J17). See Table 4 for the pinout of the BERT connector. The BERT signals are routed into the FPGA and can be muxed into any of the 8 DS26303 LIU ports under software control. For all questions concerning the operation of the on-board BERT, refer to the device data sheet available online at www.maxim-ic.com/telecom. If you are using user-defined data and driver the signal on the connector, be sure to tri-state the input signal in the FPGA. **FAILURE TO DO SO COULD CAUSE DAMAGE TO THE FPGA!**

Table 4. BERT Connector Pinout

PIN	NAME	FUNCTION
1	TCLK_EN	BERT TCLK Enable
2, 4, 6, 8, 10, 12, 14	GND	Ground
3	TCLKIN	BERT TCLK Input
5	TCLKO	BERT TCLK Output
7	RCLKIN	BERT RCLK Input
9	RCLKEN	BERT RCLK Enable
11	TDAT	BERT TDAT Output
13	RDAT	BERT RDAT Input

PROM SPI Configuration

In software mode, it is possible to configure the DS26303 using a parallel interface or a serial peripheral interface (SPI). Most advanced microcontrollers have both a parallel interface and SPI interface such as the microcontroller on the DS26303DK. The command you send to the microcontroller through either the USB or serial port determines if that data is placed on the parallel or SPI bus. Refer to the data sheet for Chipview on the particular commands required to switch data ports.

A unique feature with the SPI port is that a PROM can be used to provide the LIU with the specific data needed for configuration. If the data in the PROM is formatted a certain way, it can seem as the PROM is acting like a controller with a SPI interface in master mode.

The most common PROMs to use for this type of application are those with an internal address accumulator. This feature for the PROM is important because the device must automatically jump to the next available address in the configuration memory. The Xilinx XC18V00 device family is a byte-wide nonvolatile memory with an autoincrement address function. The family of devices is available in 1Mb, 2Mb, and 4Mb densities. The PROM is also useful because the device can perform in-circuit programming with the JTAG port. Refer the data sheet for the XC18V00 for the JTAG codes for programming the configuration memory.

Figure 2 shows a general relationship of the timing for a SPI bus. For this case, all data is clocked into the slave device on the rising edge of SCLK. This feature can be configurable on the DS26303.

Figure 2. SPI Timing Diagram

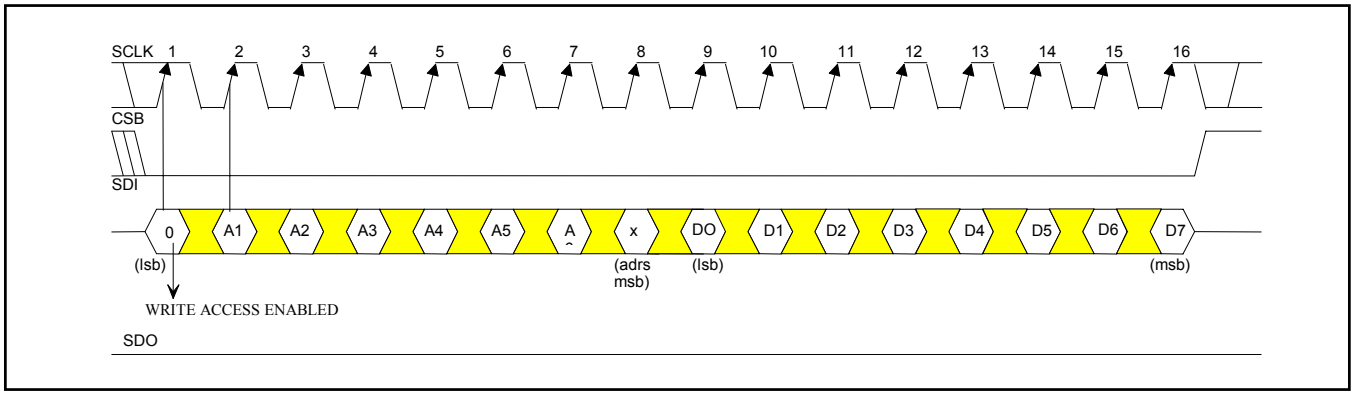


Figure 3 shows a simplified diagram of the XC18V00 device and the DS26303 in SPI (serial) mode. Notice a few key points about this diagram. First, the CLK for the XC18V00 is the MCLK for the LIU, but this is not the SCLK for the SPI interface. The SCLK can be programmed as needed. See Table 5 for an example of the memory map. Second, the programming for this device begins when OE on the XC18V00 goes high. Therefore, consideration must be taken if some delay is necessary. Generally, it is sufficient for the OE pin to be connected to some power-up delay device. The OE delay is not necessary on this DK.

Figure 3. SPI Configuration with PROM

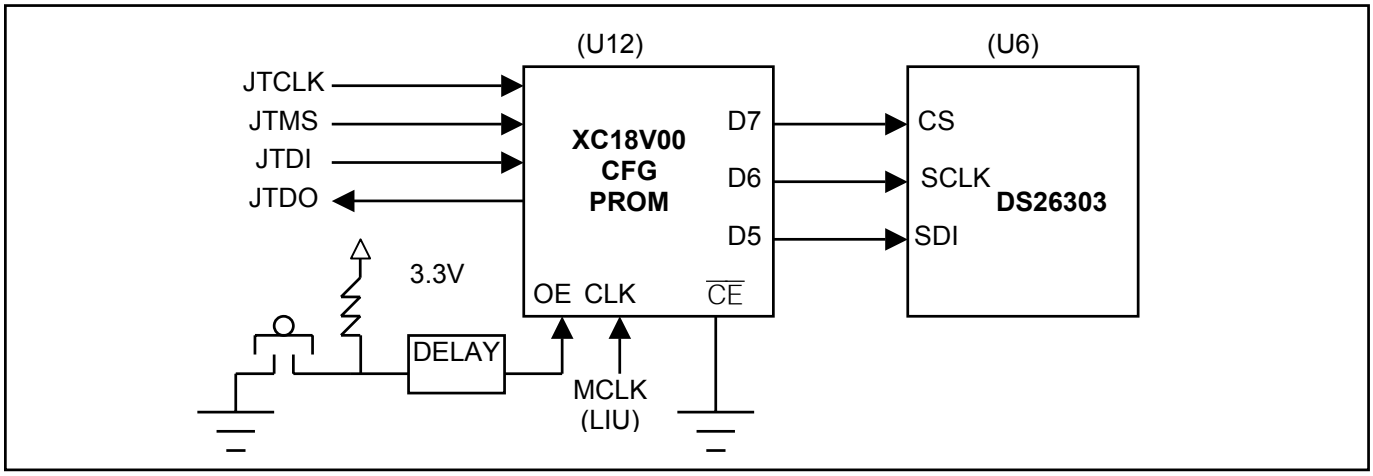


Table 5. Configuration Memory

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
	CSB	SCLK	SDI	X	X	X	X	X
0x00	1	0	0	Start of Write Cycle				
0x01	0	0	0	Bit A0 (Always a “0” for a write)				
0x02	0	1	0					
0x03	0	0	1	Bit A1				
0x04	0	1	1					
0x05	0	0	0	Bit A2				
0x06	0	1	0					
0x07	0	0	0	Bit A3				
0x08	0	1	0					
0x09	0	0	0	Bit A4				
0x0A	0	1	0					
0x0B	0	0	0	Bit A5				
0x0C	0	1	0					
0x0D	0	0	0	Bit A6				
0x0E	0	1	0					
0x0F	0	0	0	Bit A7				
0x10	0	1	0					
0x11	0	0	0	Bit D0 (LSB)				
0x12	0	1	0					
0x13	0	0	1	Bit D1				
0x14	0	1	1					
0x15	0	0	1	Bit D2				
0x16	0	1	1					
0x17	0	0	0	Bit D3				
0x18	0	1	0					
0x19	0	0	0	Bit D4				
0x1A	0	1	0					
0x1B	0	0	1	Bit D5				
0x1C	0	1	1					
0x1D	0	0	1	Bit D6				
0x1E	0	1	1					
0x1F	0	0	0	Bit D7				
0x20	0	1	0					
0x21	1	0	X	End of Write Cycle				
0x22	1	X	X					

SOFTWARE CONFIGURATION

Quick Start (Software—ChipView)

- Perform steps in the Quick Start (Hardware Configuration).
- Load ChipView software.
- Select COM port.
- Select Register View.
- From the Programs menu, launch the host application named ChipView.exe. If the default installation options were used, click the Start button on the Windows toolbar and select Programs -> ChipView -> ChipView.
- Load the DS26303DK.def file.
- Make sure that all the register settings are correct for the proper function desired for the DS26303DK.
- Refer to the DS26303 data sheet for all questions pertaining to device functionality.

MEMORY MAP

The on-board microcontroller is configured to start the user address space at 0x81000000. All offsets given below are relative to the beginning of the user address space.

Table 6. DS26303DK Relative Address Map

REF DES	DEVICE	OFFSET
U5	General-Purpose FPGA Tx/Rx Clock, Data Switch/Mux	0x0000
U4	DS2174 BERT	0x1000
U6	DS26303 8-Port T1/E1/J1 LIU	0x2000

All device registers can be easily modified using the ChipView.exe host-based user-interface software.

Table 7. General-Purpose FPGA Memory Map

OFFSET	REGISTER NAME	TYPE	DESCRIPTION
0x00	BRDID	Read-Only	Board ID
0x02	DSIDH	Read-Only	Dallas Extended ID Upper Nibble
0x03	DSIDM	Read-Only	Dallas Extended ID Middle Nibble
0x04	DSIDL	Read-Only	Dallas Extended ID Lower Nibble
0x05	BRDREV	Read-Only	Board Rev
0x06	ASMREV	Read-Only	Assembly Rev
0x07	FPGAREV	Read-Only	FPGA Firmware Rev
0x08	CTRL1	Control	Control Register 1
0x0A	ABSP	Control	Address Bank Select Pointer
0x0B	BTCLK	Control	BERT TCLK Input
0x0C	BRCLK	Control	BERT RCLK Input
0x0D	BRDAT	Control	BERT RDAT Input
0x10	TCLK	Control	Indirect Register for TCLK Source Control
0x11	TPOS	Control	Indirect Register for TPOS Source Control
0x12	TNEG	Control	Indirect Register for TPOS Source Control

ID REGISTERS

BID: BOARD ID (Offset = 0X0000)

BID is read-only with a value of 0xD.

XBIDH: HIGH NIBBLE EXTENDED BOARD ID (Offset = 0X0002)

XBIDH is read-only with a value of 0x0.

XBIDM: MIDDLE NIBBLE EXTENDED BOARD ID (Offset = 0X0003)

XBIDM is read-only with a value of 0x1.

XBIDL: LOW NIBBLE EXTENDED BOARD ID (Offset = 0X0004)

XBIDL is read-only with a value of 0x6.

BREV: BOARD FAB REVISION (Offset = 0X0005)

BREV is read-only and displays the current fab revision.

AREV: BOARD ASSEMBLY REVISION (Offset = 0X0006)

AREV is read-only and displays the current assembly revision.

PREV: FPGA REVISION (Offset = 0X0007)

PREV is read-only and displays the current PLD firmware revision.

CONTROL REGISTERS

Register Name: **CTRL_1**
Register Description: **DS26303DK FPGA CONTROL REGISTER 1**
Register Offset: **0x08**

Bit #	7	6	5	4	3	2	1	0
Name	INT303	ENRLOS1	CLKE	SPI_SWAP	SPI	OE	MCLK1	MCLK0

Bit 7: INT303. This bit indicates the status of the INT303 line.

If INT303 = LOW, there is no hardware interrupt on the DS26303.
If INT303 = HIGH, there is a hardware interrupt on the DS26303.

Bit 6: ENRLOS1. This bit enables the RLOS1 LED. This should not be enabled when driving TECLK from the DS26303.

If ENRLOS1 = LOW, the RLOS1 LED is not enabled.
If ENRLOS1 = HIGH, the RLOS1 LED is enabled and lights when RLOS1 is high.

Bit 5: CLKE. This bit sets the CLKE pin on the DS26303. This is only active when SPI (Bit 0) is HIGH. If SPI (Bit 0) is low, CLKE is always low.

If CLKE = LOW, SDO is clocked out on the rising edge of SCLK.
If CLKE = HIGH, SDO is clocked out on the falling edge of SCLK.

Bit 4: SPI_SWAP. This bit sets the BSWP/A5 pin on the DS26303. This is only active when SPI (Bit 0) is HIGH.

If SPI_SWAP = LOW, the SPI bus is LSB first.
If SPI_SWAP = HIGH, the SPI bus is MSB first.

Bit 3: SPI. This bit sets up the FPGA to use serial mode. This bit also changes the mode pin on the DS26303.

If SPI = LOW, the parallel bus is used for all read/write access. This also sets the MODE pin on the DS26303 to logic 1.
If SPI = HIGH, the SPI bus is used for all read/write access. This also sets the MODE pin on the DS26303 to logic 0.

Bit 2: OE. This bit controls the OE pin to the DS26303.

Bits 1 and 0: MCLK1 and MCLK0. These bits control the MCLK pin to the DS26303.

MCLK1	MCLK0	DESCRIPTION OF MCLK
0	0	MCLK = high-impedance mode
0	1	MCLK = on-board T1 oscillator
1	0	MCLK = on-board E1 oscillator
1	1	MCLK = user clock input

Register Name: **ABSP**
Register Description: **ADDRESS BANK SWAP POINTER**
Register Offset: **0x0A**

Bit #	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

Bits 7 to 0: D7 to D0. These bits control the address bank for address 0x10 (TCLK N), 0x11 (TPOS), and 0x12 (TNEG).

ABSP	DESCRIPTION
0x00	Bank Address Value for Port 1
0x01	Bank Address Value for Port 2
0x02	Bank Address Value for Port 3
0x03	Bank Address Value for Port 4
0x04	Bank Address Value for Port 5
0x05	Bank Address Value for Port 6
0x06	Bank Address Value for Port 7
0x07	Bank Address Value for Port 8

Register Name: **BTCLK**
Register Description: **BERT TCLK SOURCE**
Register Offset: **0x0B**

Bit #	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

Bits 7 to 0: D7 to D0. These bits control the source of the TCLK for the BERT.

BTCLK	DESCRIPTION
0x00	RCLK Port 1
0x01	RCLK Port 2
0x02	RCLK Port 3
0x03	RCLK Port 4
0x04	RCLK Port 5
0x05	RCLK Port 6
0x06	RCLK Port 7
0x07	RCLK Port 8
0x08	HI-Z
0x09	HI-Z
0x0A	HI-Z
0x0B	HI-Z
0x0C	HI-Z
0x0D	HI-Z
0x0E	HI-Z
0x0F	HI-Z
0x10	1.544MHz On-board oscillator
0x11	2.048MHz On-board oscillator
0x12	User clock
0x13	CLKA DS26303
0x14	TECLK DS26303
0x15	TCLKBERT OUT
0x16–0xFF	HI-Z

Register Name: **BRCLK**
Register Description: **BERT RCLK SOURCE**
Register Offset: **0x0C**

Bit #	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

Bits 7 to 0: D7 to D0. These bits control the source of the RCLK for the BERT.

BTCLK	DESCRIPTION
0x00	RCLK Port 1
0x01	RCLK Port 2
0x02	RCLK Port 3
0x03	RCLK Port 4
0x04	RCLK Port 5
0x05	RCLK Port 6
0x06	RCLK Port 7
0x07	RCLK Port 8
0x08	HI-Z
0x09	HI-Z
0x0A	HI-Z
0x0B	HI-Z
0x0C	HI-Z
0x0D	HI-Z
0x0E	HI-Z
0x0F	HI-Z
0x10	1.544MHz On-board oscillator
0x11	2.048MHz On-board oscillator
0x12	User clock
0x13	CLKA DS26303
0x14	TECLK DS26303
0x15	TCLKBERT OUT
0x16–0xFF	HI-Z

Register Name: **BRDAT**
Register Description: **BERT RDAT SOURCE**
Register Offset: **0x0D**

Bit #	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

Bits 7 to 0: D7 to D0. These bits control the source of the RDAT for the BERT. Note that the DS26303 must be in single-rail mode for BERT to function properly.

BRDAT	DESCRIPTION
0x00	RPOS Port 1
0x01	RPOS Port 2
0x02	RPOS Port 3
0x03	RPOS Port 4
0x04	RPOS Port 5
0x05	RPOS Port 6
0x06	RPOS Port 7
0x07	RPOS Port 8
0x08	HI-Z
0x09	HI-Z
0x0A	HI-Z
0x0B	HI-Z
0x0C	HI-Z
0x0D	HI-Z
0x0E	HI-Z
0x0F	HI-Z
0x10	1.544MHz On-board oscillator
0x11	2.048MHz On-board oscillator
0x12	User clock
0x13	CLKA DS26303
0x14	TECLK DS26303
0x15	TCLKBERT OUT
0x16–0xFF	HI-Z

Register Name: **TCLK**
Register Description: **PORT TCLK SOURCE**
Register Offset: **0x10**

Bit #	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

Note: *This is an indirect register that is related to ABSP (0x0A). See register description.*

Bits 7 to 0: D7 to D0. These bits control the source of the port TCLK for the DS26303.

TCLK	DESCRIPTION
0x00	RCLK Port 1
0x01	RCLK Port 2
0x02	RCLK Port 3
0x03	RCLK Port 4
0x04	RCLK Port 5
0x05	RCLK Port 6
0x06	RCLK Port 7
0x07	RCLK Port 8
0x08	HI-Z
0x09	HI-Z
0x0A	HI-Z
0x0B	HI-Z
0x0C	HI-Z
0x0D	HI-Z
0x0E	HI-Z
0x0F	HI-Z
0x10	1.544MHz On-board oscillator
0x11	2.048MHz On-board oscillator
0x12	User clock
0x13	CLKA DS26303
0x14	TECLK DS26303
0x15	TCLKBERT OUT
0x16–0xFF	HI-Z

Register Name: **TPOS**
Register Description: **PORT TPOS SOURCE**
Register Offset: **0x11**

Bit #	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

Note: *This is an indirect register that is related to ABSP (0x0A). See register description.*

Bits 7 to 0: D7 to D0. These bits control the source of the port TPOS for the DS26303.

TPOS	DESCRIPTION
0x00	RPOS Port 1
0x01	RPOS Port 2
0x02	RPOS Port 3
0x03	RPOS Port 4
0x04	RPOS Port 5
0x05	RPOS Port 6
0x06	RPOS Port 7
0x07	RPOS Port 8
0x08	HI-Z
0x09	HI-Z
0x0A	HI-Z
0x0B	HI-Z
0x0C	HI-Z
0x0D	HI-Z
0x0E	HI-Z
0x0F	HI-Z
0x10	1.544MHz On-board oscillator
0x11	2.048MHz On-board oscillator
0x12	User clock
0x13	CLKA DS26303
0x14	TECLK DS26303
0x15	TDATBERT OUT
0x16–0xFF	HI-Z

Register Name: **TNEG**
Register Description: **PORT TNEG SOURCE**
Register Offset: **0x12**

Bit #	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

Note: *This is an indirect register that is related to ABSP (0x0A). See register description.*

Bits 7 to 0: D7 to D0. These bits control the source of the port TNEG for the DS26303.

TNEG	DESCRIPTION
0x00	RNEG Port 1
0x01	RNEG Port 2
0x02	RNEG Port 3
0x03	RNEG Port 4
0x04	RNEG Port 5
0x05	RNEG Port 6
0x06	RNEG Port 7
0x07	RNEG Port 8
0x08	HI-Z
0x09	HI-Z
0x0A	HI-Z
0x0B	HI-Z
0x0C	HI-Z
0x0D	HI-Z
0x0E	HI-Z
0x0F	HI-Z
0x10	1.544MHz On-board oscillator
0x11	2.048MHz On-board oscillator
0x12	User clock
0x13	CLKA DS26303
0x14	TECLK DS26303
0x15	Drive Logic “0”
0x16–0xFF	HI-Z

DS26303 INFORMATION

For more information about the DS26303, refer to the DS26303 data sheet available on our website at www.maxim-ic.com/DS26303.

DS26303DK INFORMATION

For more information about the DS26303DK including software downloads, go to www.maxim-ic.com/DS26303DK.

TECHNICAL SUPPORT

For additional technical support, e-mail your questions to telecom.support@dalsemi.com.

SCHEMATICS

The DS26303DK schematics are featured in the following 22 pages.

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DS26303 DESIGN KIT
SCHEMATIC
DALLAS SEMICONDUCTOR / MAXIM

AUGUST 2005

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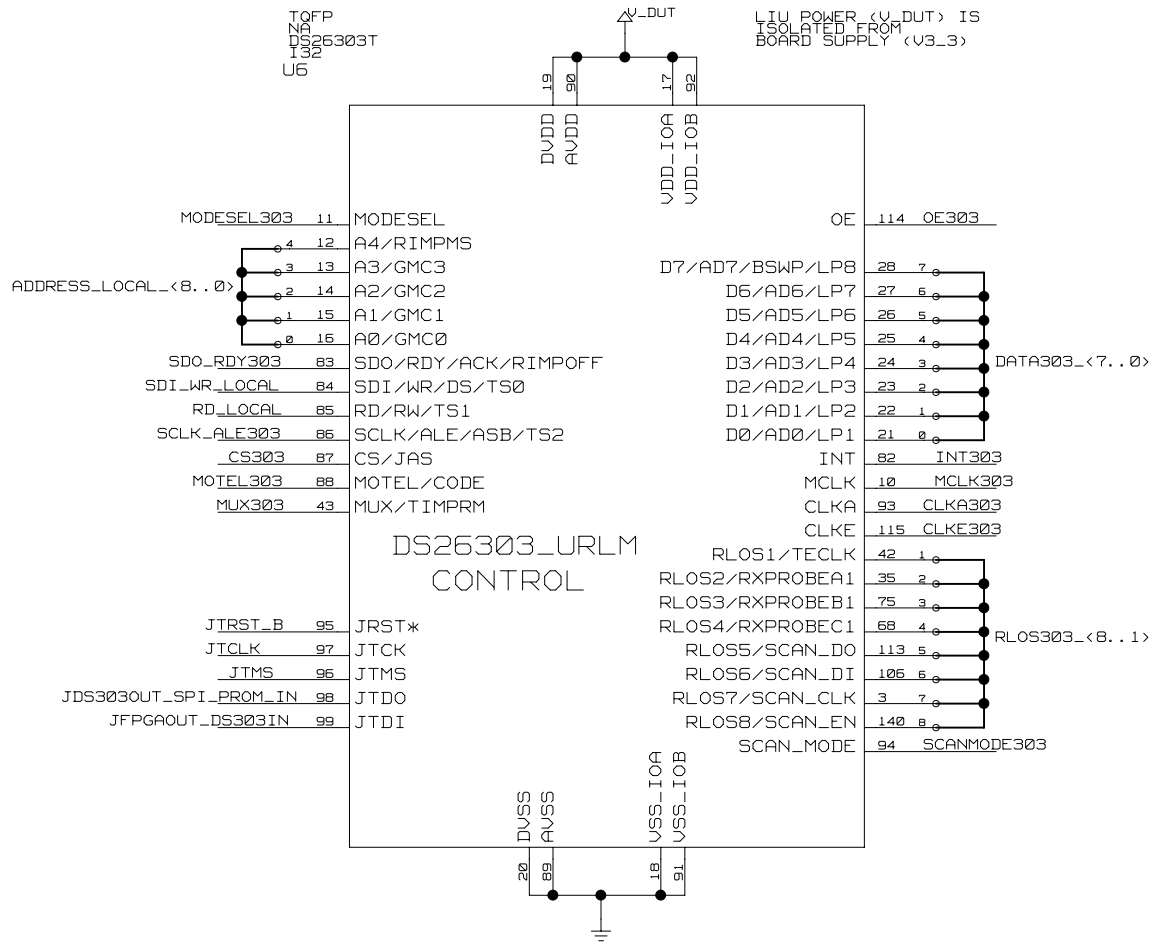

TITLE: DS26303 CONTROL BLOCK	DATE:
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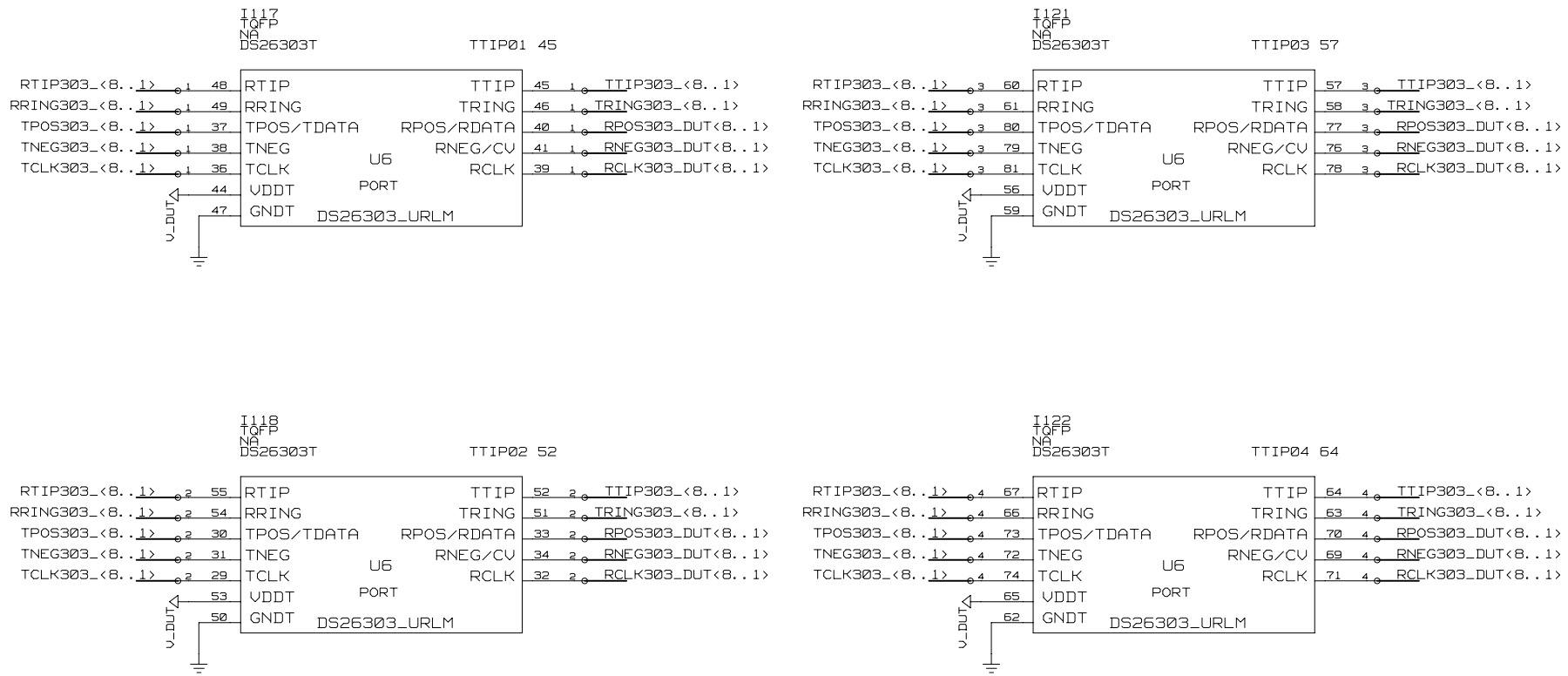

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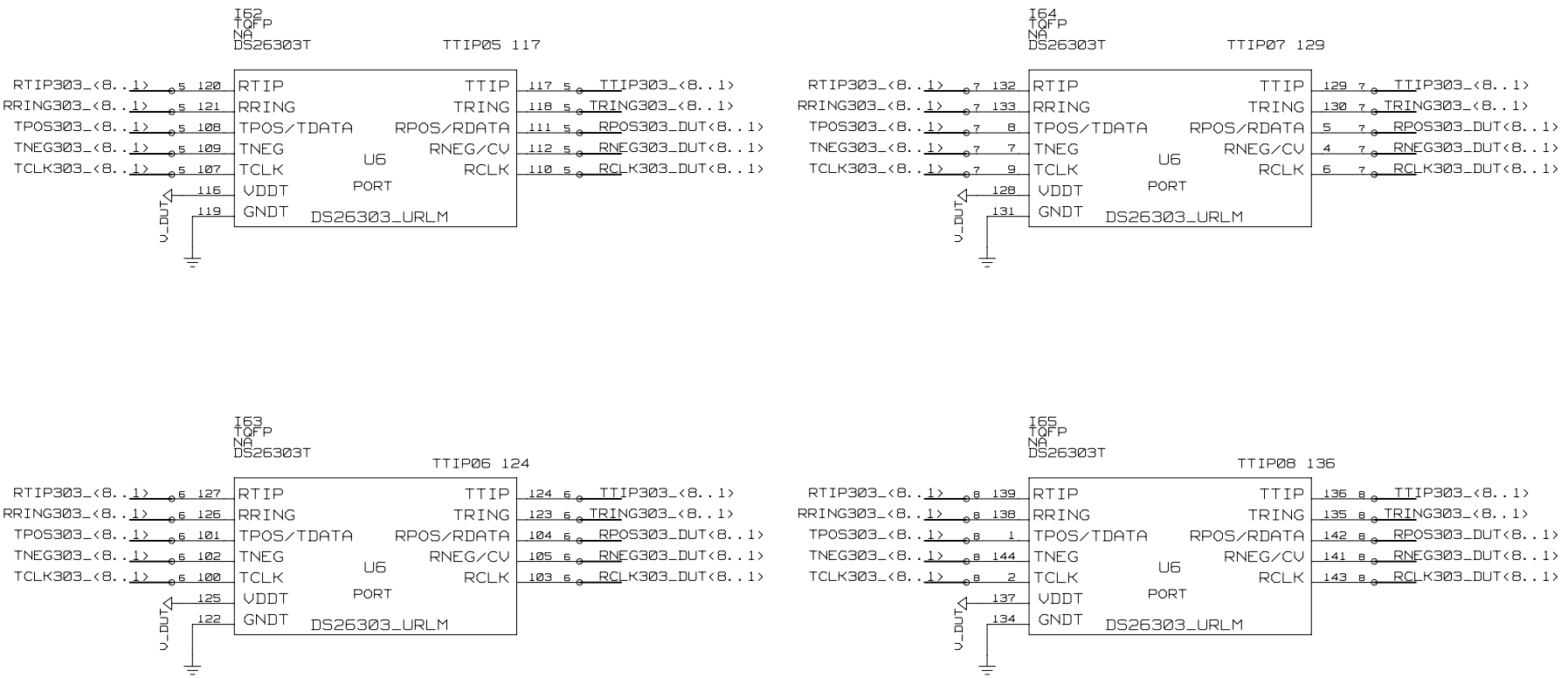

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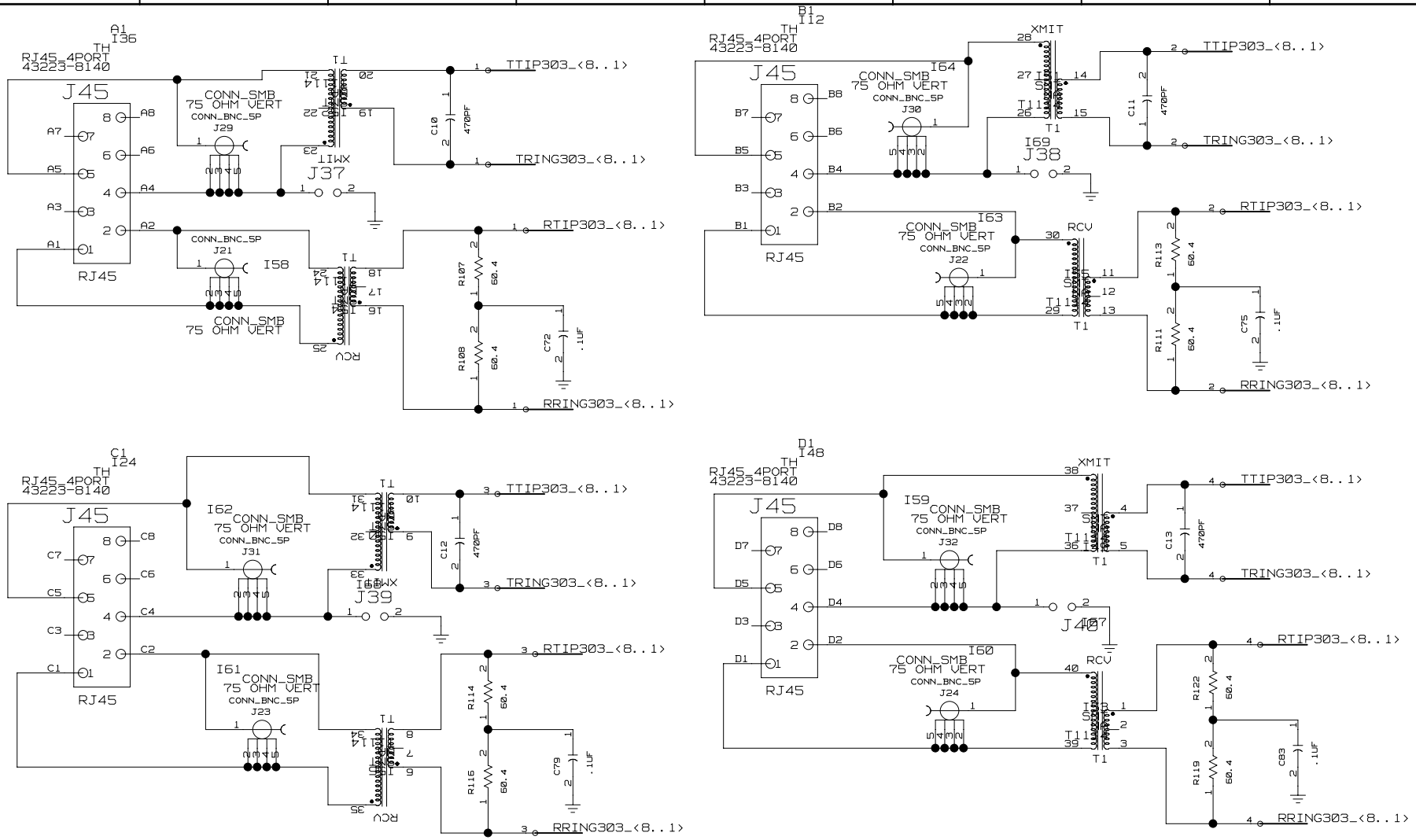
A1
I36
TH
RJ45_4PORT
43223-8140
J45
RJ45
CONN_SMB
75 OHM VERT
CONN_BNC_5P
J29
J21
I58
J37
XMIT
RCV
T1
C10
470PF
R107
R108
60.4
C72
.1UF
TTIP303_<8..1>
TRING303_<8..1>
RTIP303_<8..1>
RRING303_<8..1>
B1
I12
I64
I63
J30
J22
J38
I69
C11
R113
R111
C75
C1
I24
I62
I61
J31
J23
J39
I65
R114
R116
C79
C12
D1
I48
I59
I60
J32
J24
J40
I67
R122
R119
C83
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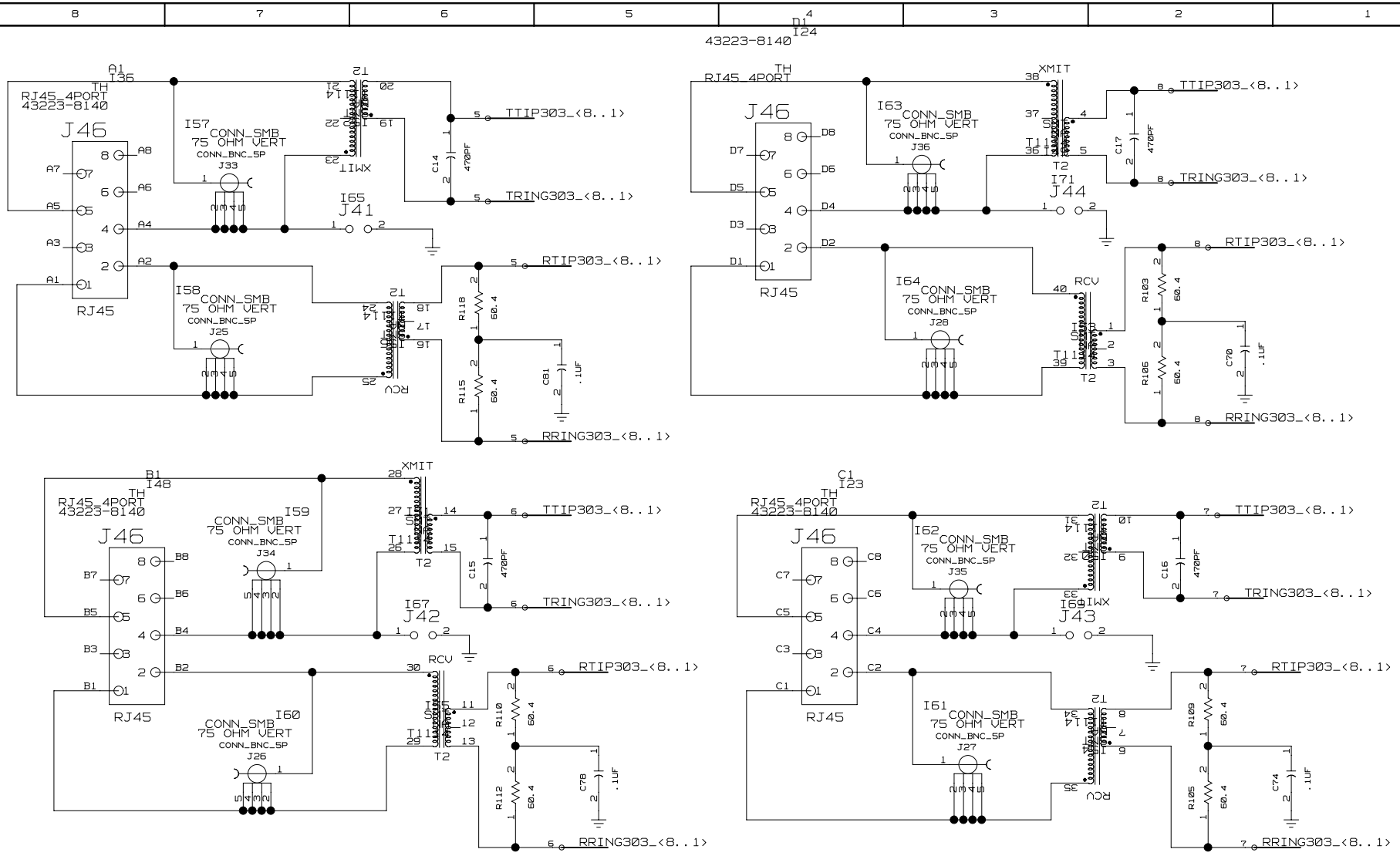
D1
I24
43223-8140
A1
I36
TH
RJ45_4PORT
43223-8140
J46
RJ45
I57
CONN_SMB
75 OHM VERT
CONN_BNC_5P
J33
I65
J41
I58
J25
T2
XMIT
RCV
C14
470PF
R118
R115
60.4
CB1
.1UF
TTIP303_<8..1>
TRING303_<8..1>
RTIP303_<8..1>
RRING303_<8..1>
I63
J36
I64
J28
I71
J44
R103
R105
C17
C70
B1
I48
I59
J34
I67
J42
I60
J26
C15
R110
R112
C78
C1
I23
I62
J35
I69
J43
I61
J27
C16
R109
R105
C74
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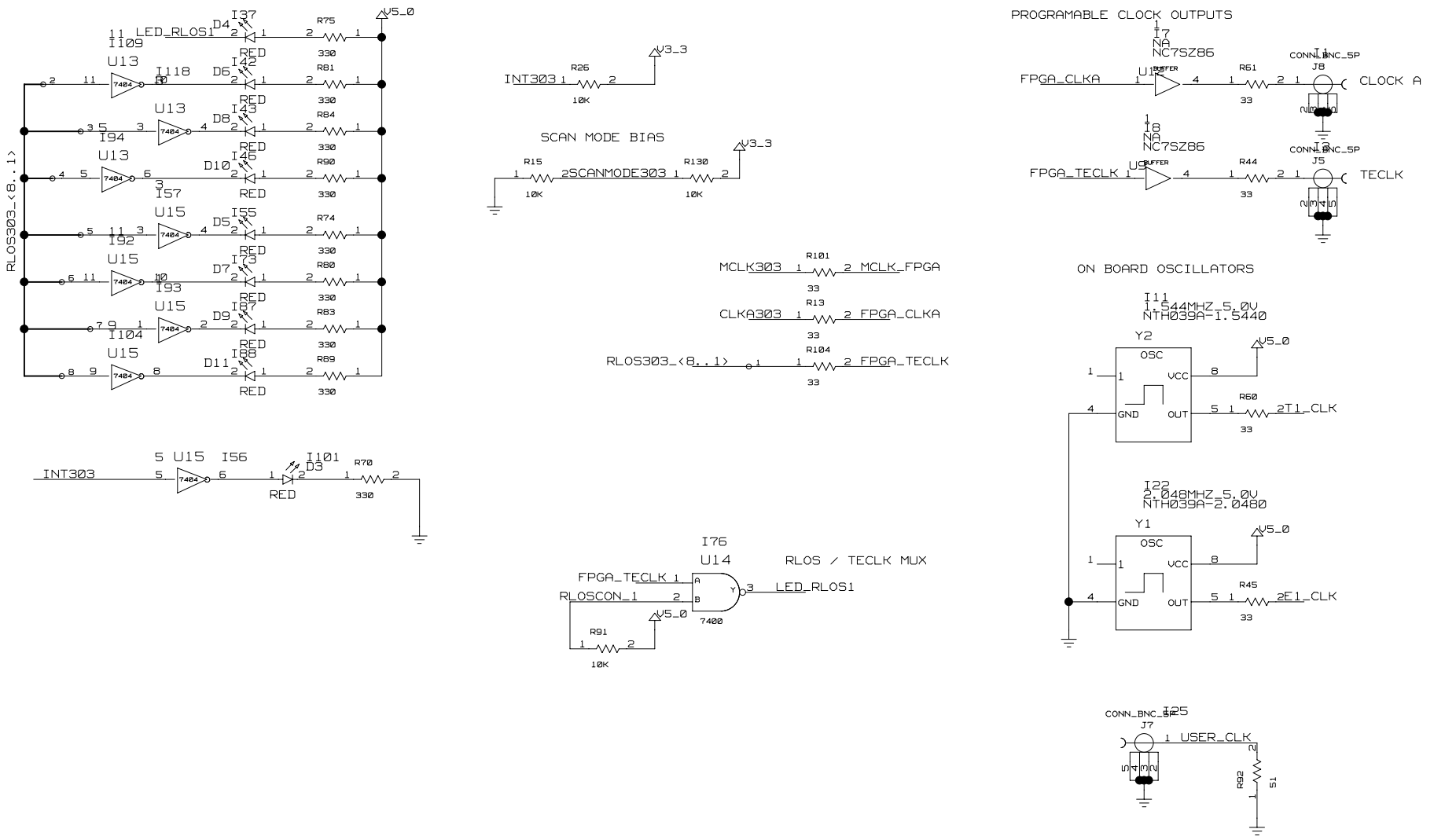

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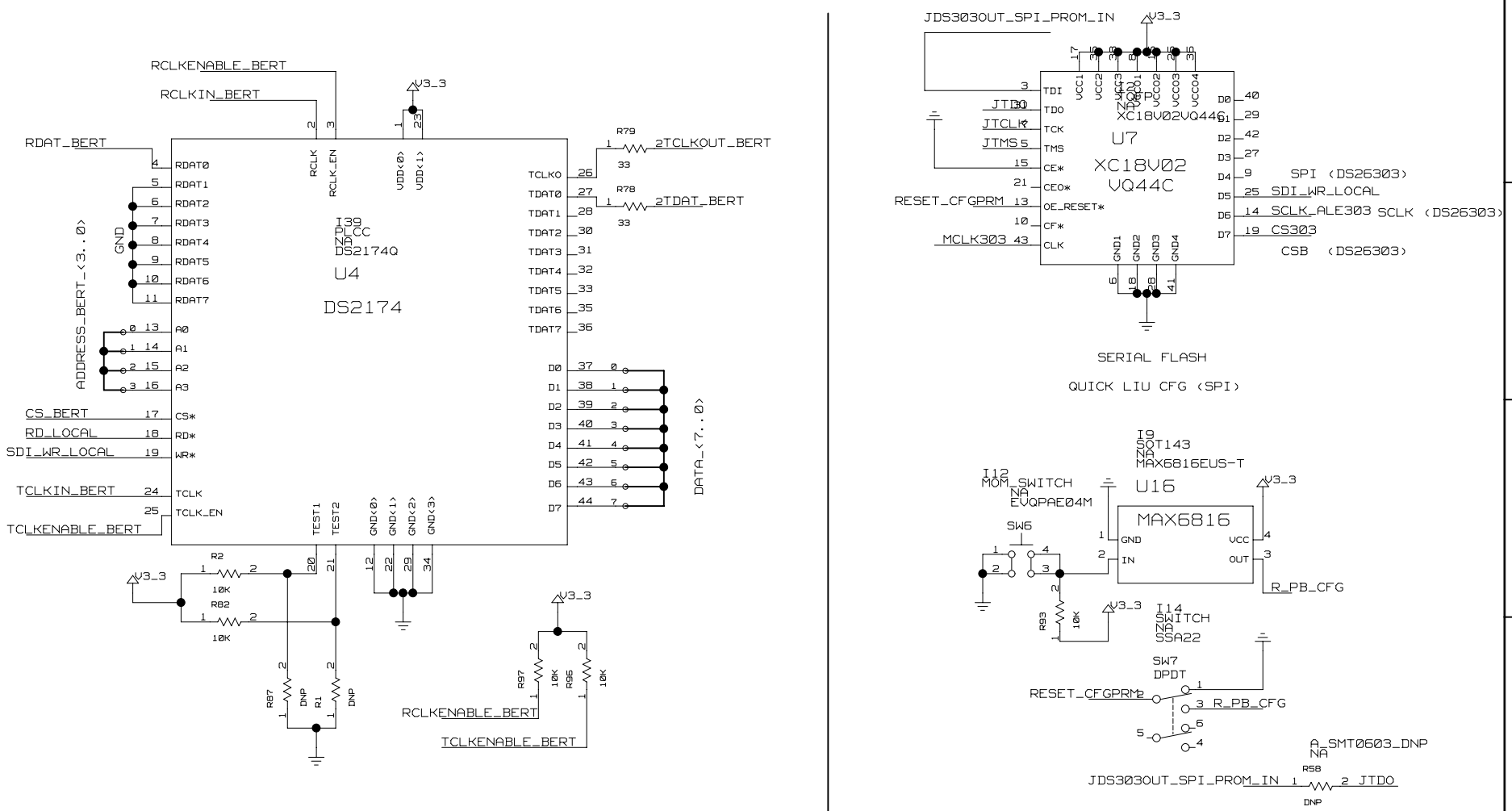

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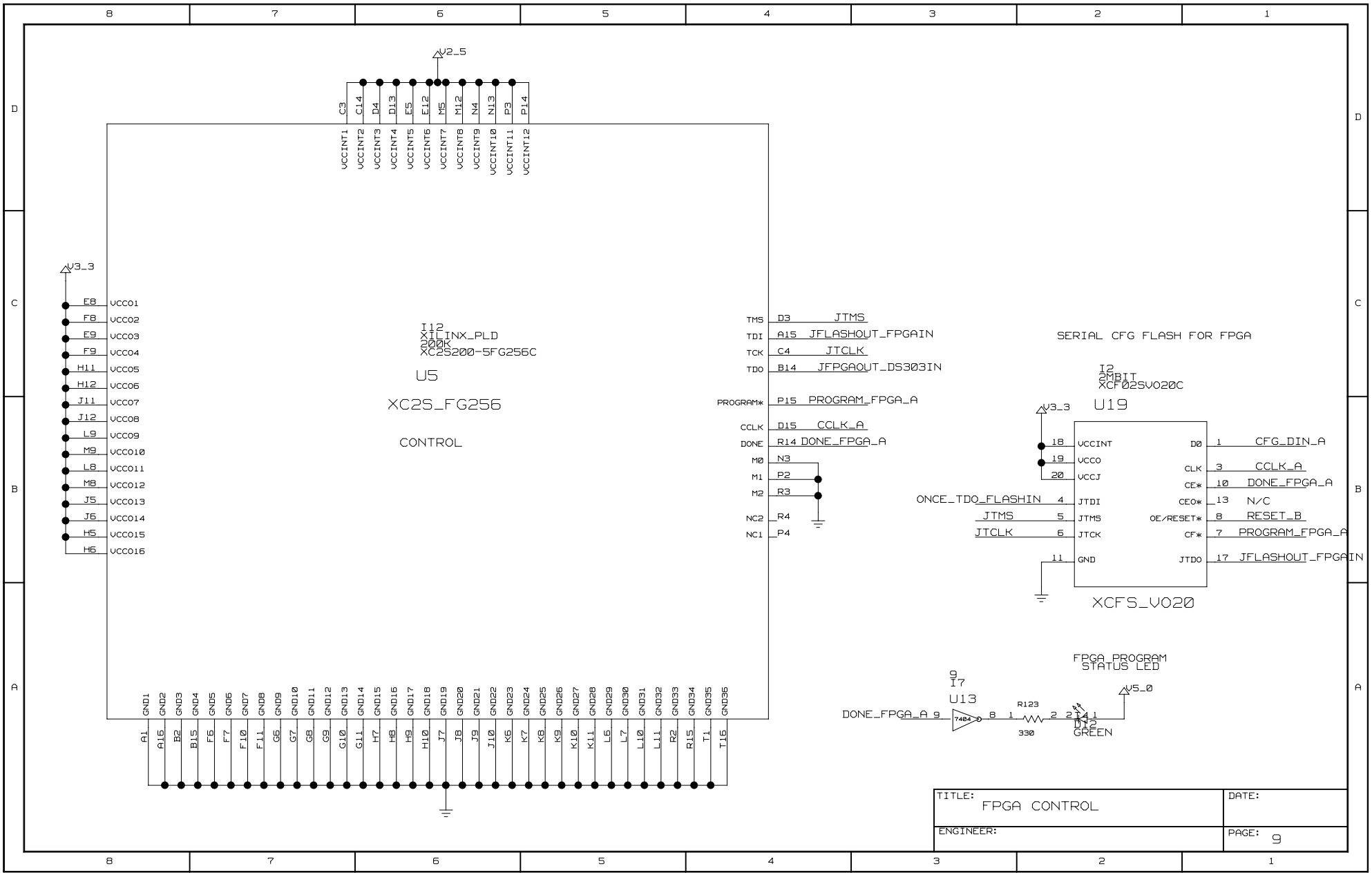
V2_5
C3
C14
D4
D13
E5
E12
M5
M12
N4
N13
P3
P14
VCCINT1
VCCINT2
VCCINT3
VCCINT4
VCCINT5
VCCINT6
VCCINT7
VCCINT8
VCCINT9
VCCINT10
VCCINT11
VCCINT12
V3_3
E8 VCCO1
F8 VCCO2
E9 VCCO3
F9 VCCO4
H11 VCCO5
H12 VCCO6
J11 VCCO7
J12 VCCO8
L9 VCCO9
M9 VCCO10
L8 VCCO11
M8 VCCO12
J5 VCCO13
J6 VCCO14
H5 VCCO15
H6 VCCO16
I12
XILINX_PLD
200K
XC2S200-5FG256C
U5
XC2S_FG256
CONTROL
TMS D3 JTMS
TDI A15 JFLASHOUT_FPGAIN
TCK C4 JTCLK
TDO B14 JFPGAOUT_DS303IN
PROGRAM* P15 PROGRAM_FPGA_A
CCLK D15 CCLK_A
DONE R14 DONE_FPGA_A
M0 N3
M1 P2
M2 R3
NC2 R4
NC1 P4
GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8 GND9 GND10 GND11 GND12 GND13 GND14 GND15 GND16 GND17 GND18 GND19 GND20 GND21 GND22 GND23 GND24 GND25 GND26 GND27 GND28 GND29 GND30 GND31 GND32 GND33 GND34 GND35 GND36
A1 A16 B2 B15 F6 F7 F10 F11 G6 G7 G8 G9 G10 G11 H7 H8 H9 H10 J7 J8 J9 J10 K6 K7 K8 K9 K10 K11 L6 L7 L10 L11 R2 R15 T1 T16
SERIAL CFG FLASH FOR FPGA
I2
2MBIT
XCF02SV020C
U19
V3_3
18 VCCINT
19 VCCO
20 VCCJ
ONCE_TDO_FLASHIN 4 JTDI
JTMS 5 JTMS
JTCLK 6 JTCK
11 GND
D0 1 CFG_DIN_A
CLK 3 CCLK_A
CE* 10 DONE_FPGA_A
CEO* 13 N/C
OE/RESET* 8 RESET_B
CF* 7 PROGRAM_FPGA_A
JTDO 17 JFLASHOUT_FPGAIN
XCFS_V020
FPGA_PROGRAM
STATUS LED
9
I7
U13
DONE_FPGA_A 9
7404
8 1
R123
330
2 2
D12
GREEN
V5_0
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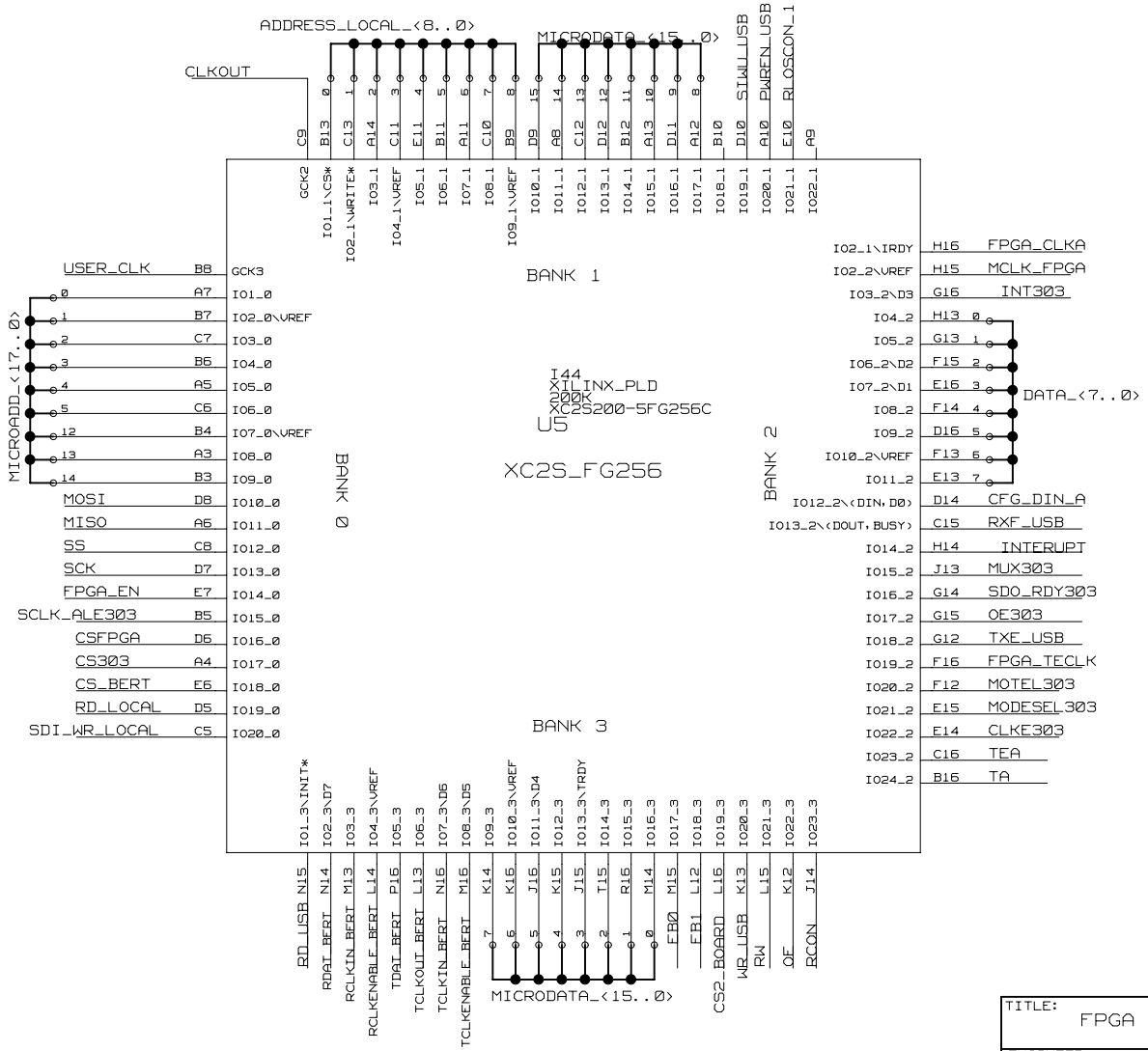

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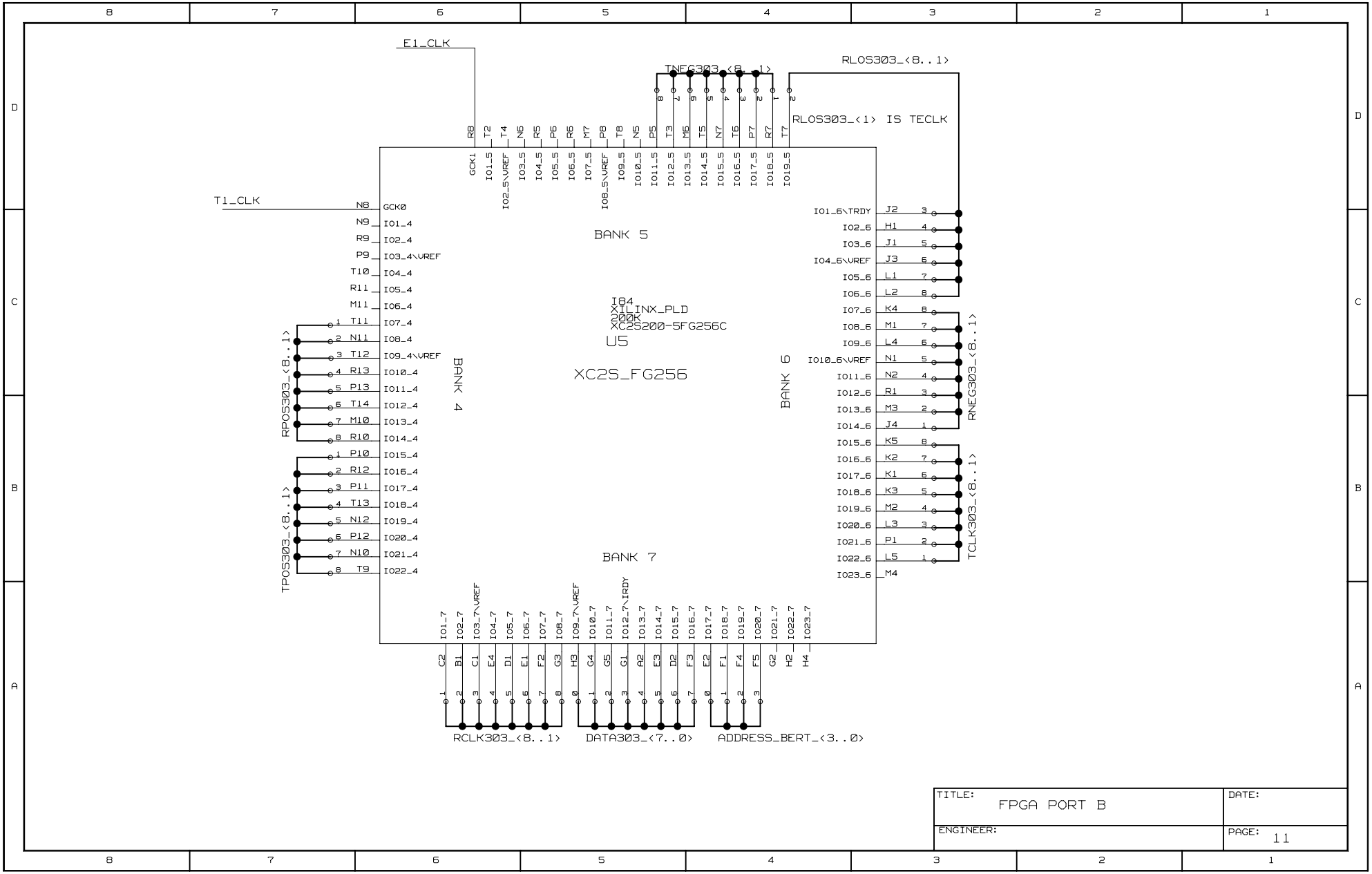

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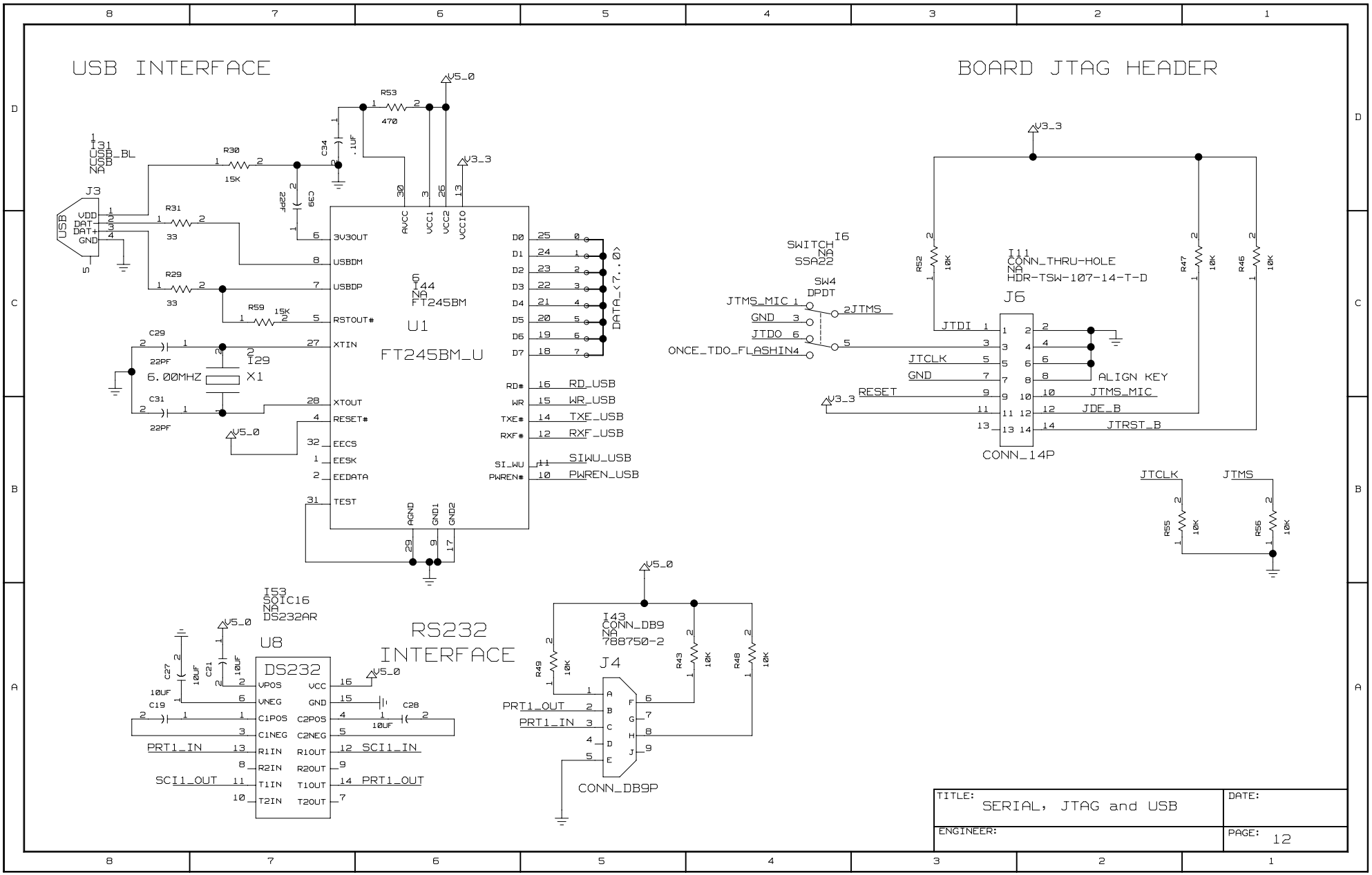
USB INTERFACE
BOARD JTAG HEADER
RS232 INTERFACE
V5_0
V3_3
R53
470
C34
.1UF
R30
15K
C39
22PF
J3
USB
VDD
DAT-
DAT+
GND
R31
33
R29
33
R59
15K
C29
22PF
C31
22PF
I29
6.00MHZ
X1
U1
FT245BM_U
3V3OUT
USBDM
USBDP
RSTOUT#
XTIN
XTOUT
RESET#
EECS
EESK
EEDATA
TEST
AVCC
VCC1
VCC2
VCC10
AGND
GND1
GND2
D0
D1
D2
D3
D4
D5
D6
D7
DATA<7..0>
RD#
WR
TXE#
RXF#
SI_WU
PWREN#
RD_USB
WR_USB
TXE_USB
RXF_USB
SIWU_USB
PWREN_USB
SWITCH
SSA2ND
I6
SW4
DPDT
JTMS_MIC
GND
JTDO
ONCE_TDO_FLASHIN4
2JTMS
R52
10K
R47
10K
R45
10K
I11
CONN_THRU-HOLE
HDR-TSW-107-14-T-D
J6
JTDI
JTCLK
GND
RESET
ALIGN KEY
JTMS_MIC
JDE_B
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CONN_14P
JTCLK
JTMS
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10K
R56
10K
I53
SOIC16
DS232AR
U8
DS232
VPOS
VNEG
C1POS
C1NEG
C2POS
C2NEG
R1IN
R2IN
T1IN
T2IN
R1OUT
R2OUT
T1OUT
T2OUT
VCC
GND
C27
C21
C19
C28
10UF
PRT1_IN
SCI1_OUT
SCI1_IN
PRT1_OUT
I43
CONN_DB9
788750-2
J4
R49
10K
R43
10K
R48
10K
CONN_DB9P
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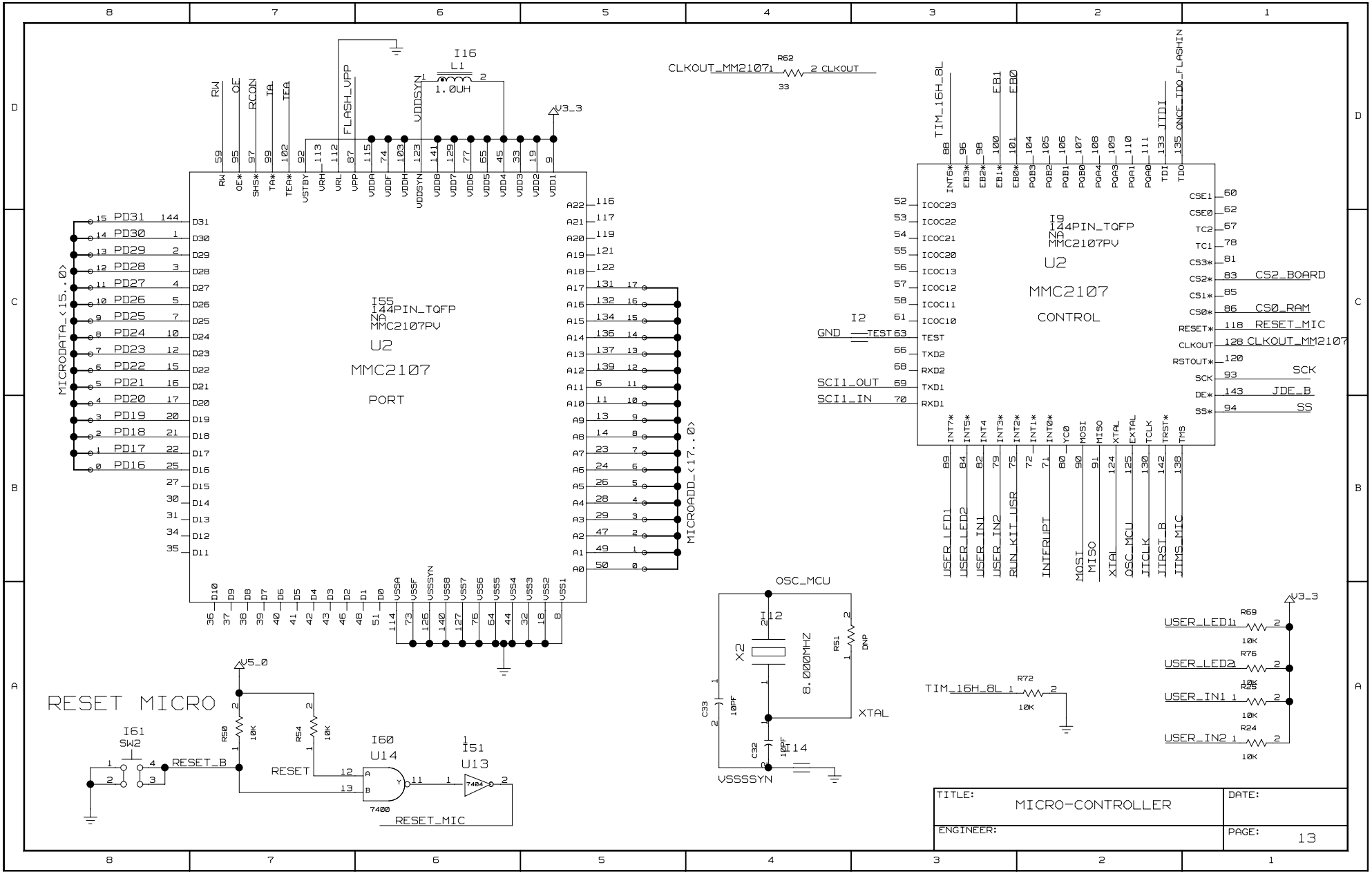
I16
L1
1.0UH
I55
144PIN_TQFP
MMC2107PV
U2
MMC2107
PORT
I9
144PIN_TQFP
MMC2107PV
U2
MMC2107
CONTROL
I2
CLKOUT_MM2107
R62
33
2 CLKOUT
MICRODATA_<15..0>
MICROADD_<17..0>
V3_3
V5_0
FLASH_VPP
VDDSYN
RW
OE
RCON
TA
TEA
RESET MICRO
I61
SW2
RESET_B
R50
10K
R54
10K
I60
U14
7400
I51
U13
7404
RESET
RESET_MIC
OSC_MCU
I12
X2
8.000MHZ
R51
DNP
XTAL
C33
10PF
C32
10PF
I14
VSSSSYN
TIM_16H_8L
R72
10K
USER_LED1
USER_LED2
USER_IN1
USER_IN2
R69
R76
R25
R24
10K
CS2_BOARD
CS0_RAM
RESET_MIC
CLKOUT_MM2107
SCK
JDE_B
SS
SCI1_OUT
SCI1_IN
GND
TEST
RUN_KIT_USR
INTERRUPT
MOSI
MISO
XTAL
OSC_MCU
IICLK
IIRST_B
IIMS_MIC
QNCE_TDO_FLASHIN
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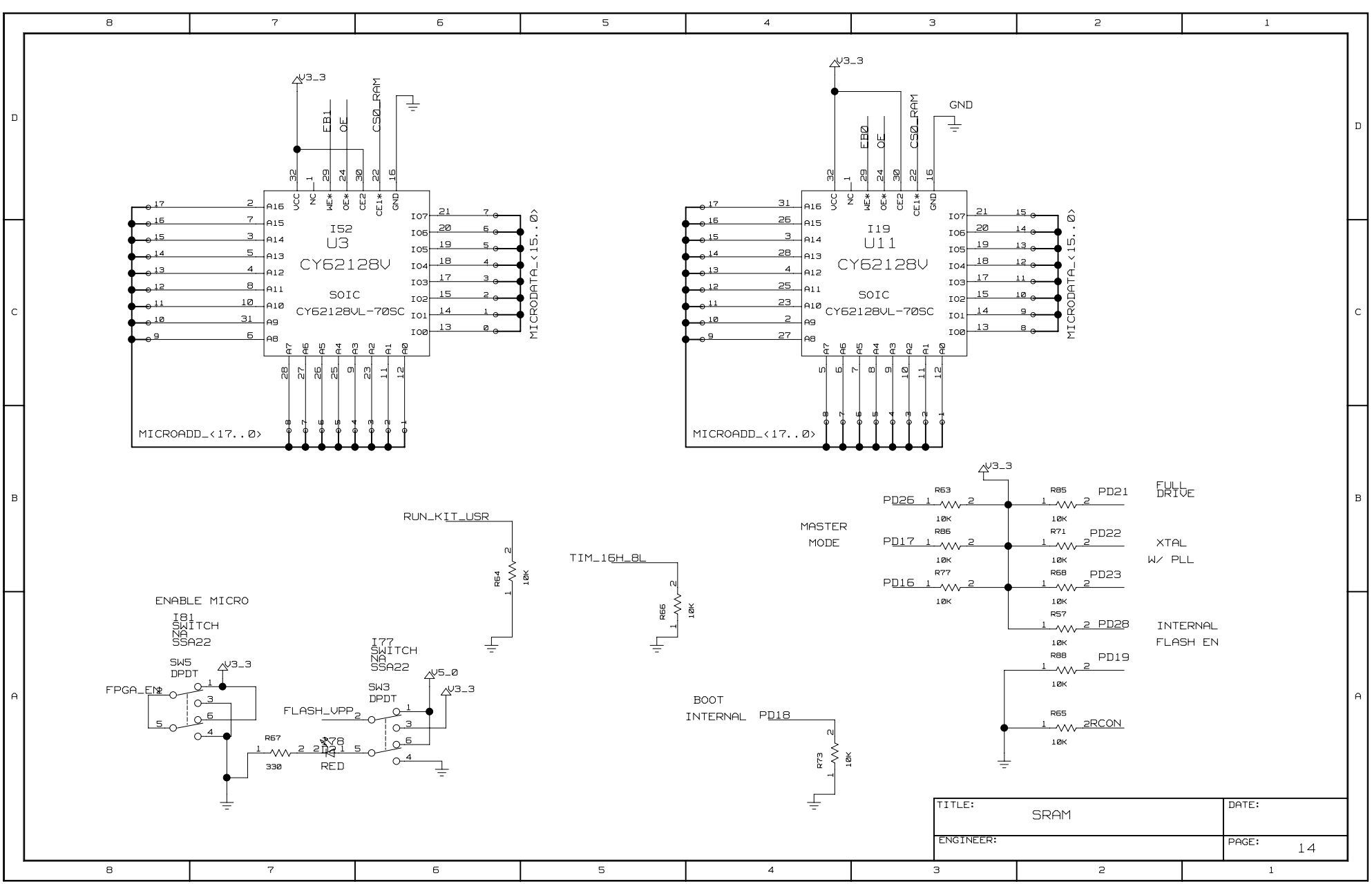
V3_3
FB1
OE
CS0_RAM
I52
U3
CY62128V
SOIC
CY62128VL-70SC
MICRODATA_<15..0>
MICROADD_<17..0>
V3_3
FB0
OE
CS0_RAM
GND
I19
U11
CY62128V
SOIC
CY62128VL-70SC
MICRODATA_<15..0>
MICROADD_<17..0>
RUN_KIT_USR
R64
10K
TIM_16H_8L
R66
10K
ENABLE MICRO
I81
SWITCH
SSA22
SW5
DPDT
V3_3
FPGA_EN
I77
SWITCH
SSA22
SW3
DPDT
V5_0
V3_3
FLASH_VPP
R67
330
D78
RED
BOOT
INTERNAL
PD18
R73
10K
MASTER
MODE
V3_3
PD26
R63
10K
R85
PD21
FULL
DRIVE
PD17
R86
10K
R71
PD22
XTAL
W/ PLL
PD16
R77
10K
R68
PD23
R57
PD28
INTERNAL
FLASH EN
R88
PD19
R65
2RCON
TITLE:
SRAM
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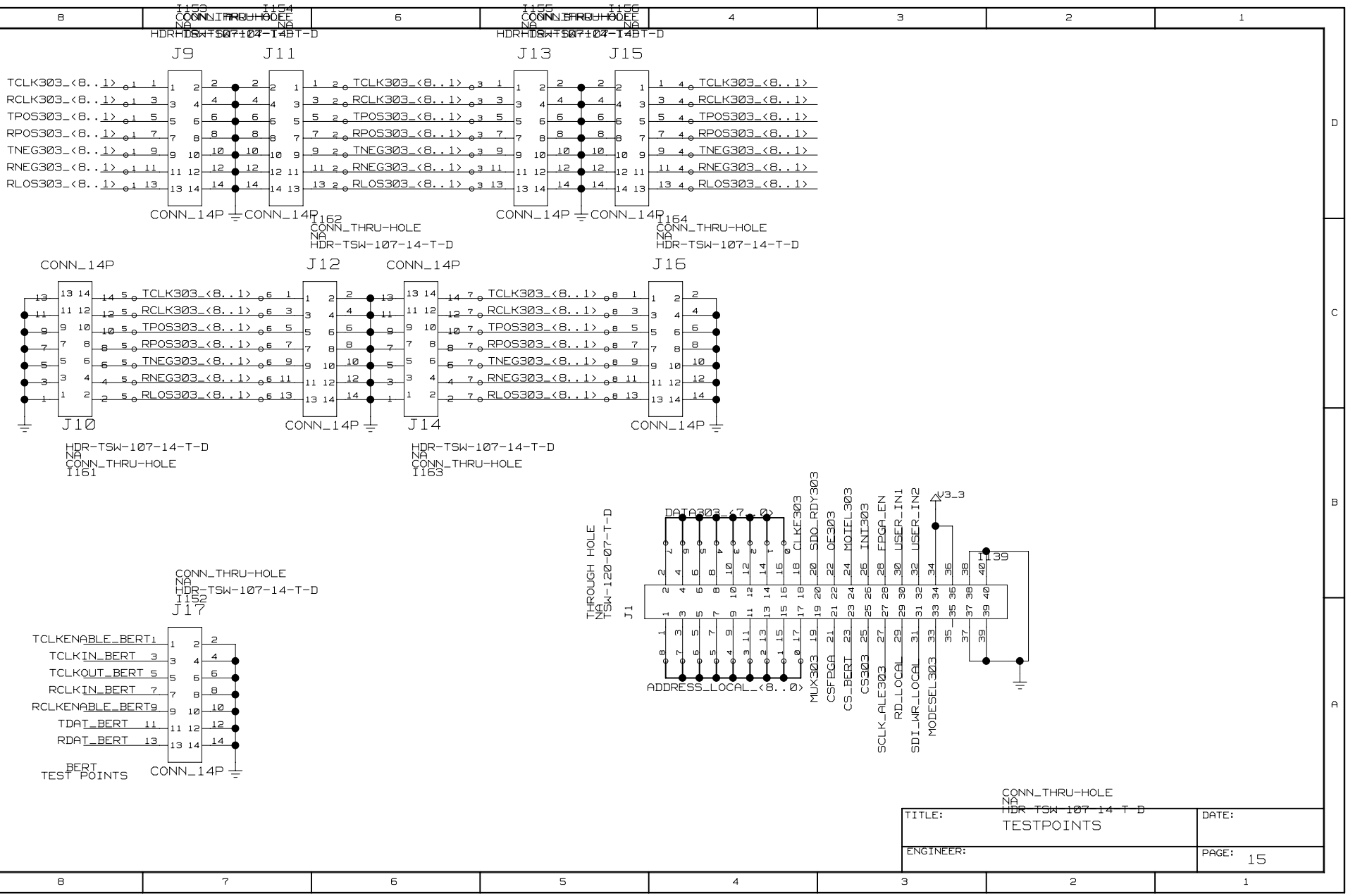
J9
J11
J13
J15
J12
J16
J10
J14
J17
J1
CONN_14P
HDR-TSW-107-14-T-D
CONN_THRU-HOLE
TCLK303_<8..1>
RCLK303_<8..1>
TPOS303_<8..1>
RPOS303_<8..1>
TNEG303_<8..1>
RNEG303_<8..1>
RLOS303_<8..1>
DATA303_<7..0>
ADDRESS_LOCAL_<8..0>
MUX303
CSFPGA
CS_BERT
CS303
SCLK_ALE303
RD_LOCAL
SDI_WR_LOCAL
MODESEL303
CLKE303
SDO_RDY303
OE303
MOIEL303
INT303
FPGA_EN
USER_IN1
USER_IN2
V3_3
THROUGH HOLE
TSW-120-07-T-D
TCLKENABLE_BERT
TCLKIN_BERT
TCLKOUT_BERT
RCLKIN_BERT
RCLKENABLE_BERT
TDAT_BERT
RDAT_BERT
BERT
TEST POINTS
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TESTPOINTS
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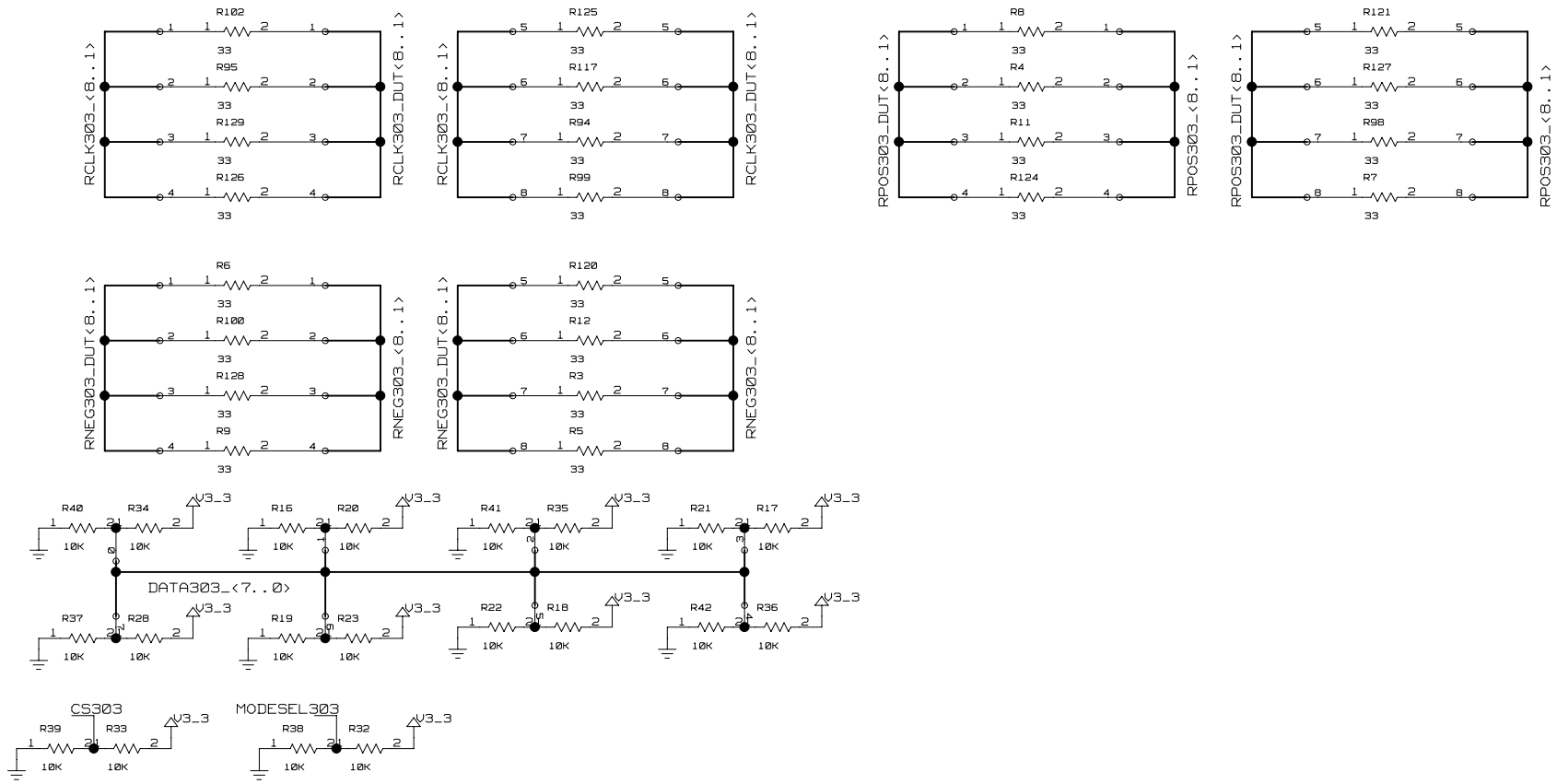
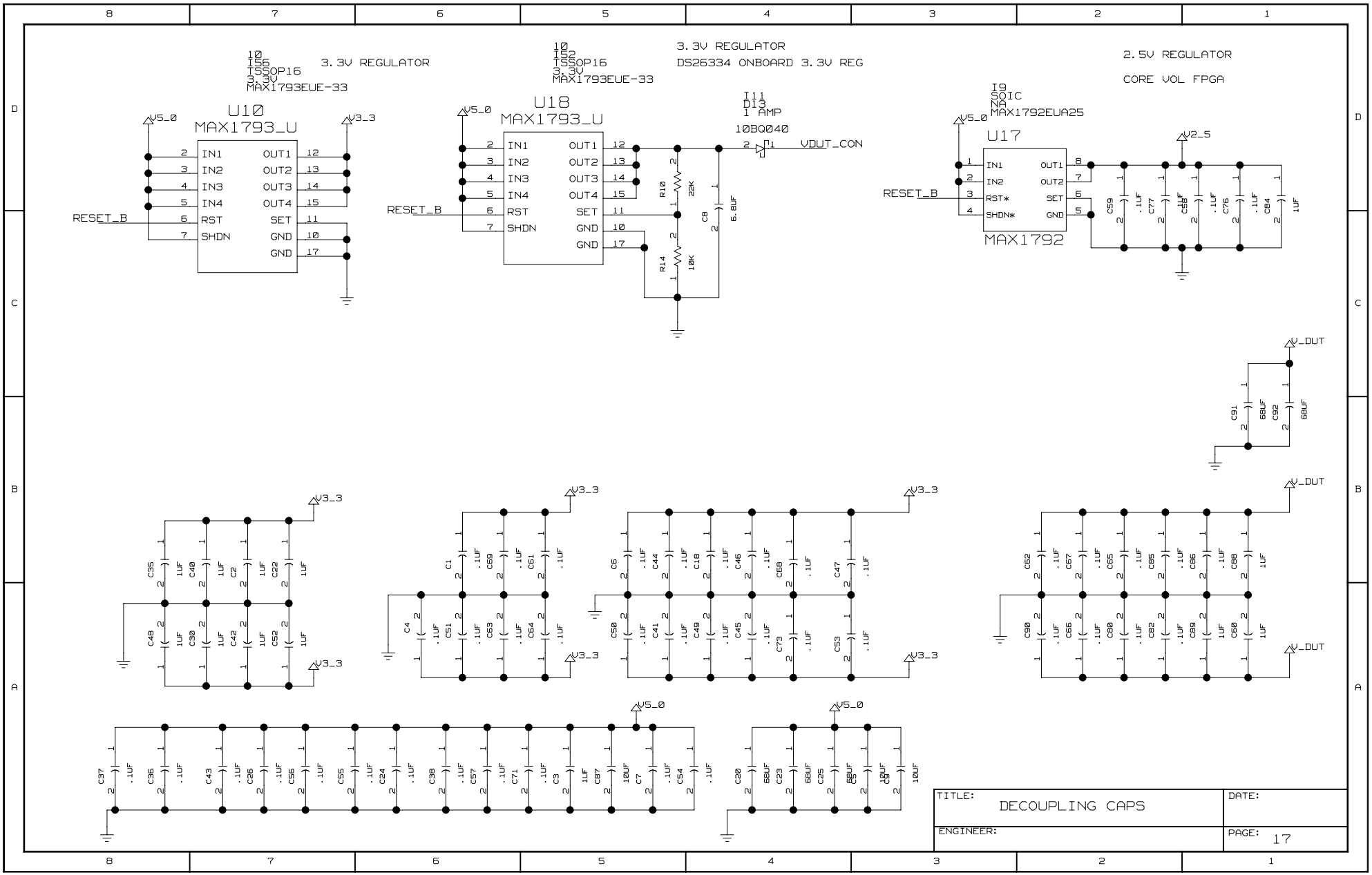


TITLE: SERIAL TERMINATION	DATE:
ENGINEER:	PAGE: 16


3.3V REGULATOR
U10
MAX1793_U
V5_0
V3_3
RESET_B
IN1
IN2
IN3
IN4
RST
SHDN
OUT1
OUT2
OUT3
OUT4
SET
GND
3.3V REGULATOR
DS26334 ONBOARD 3.3V REG
U18
MAX1793_U
I11
D10
1 AMP
10BQ040
VDUT_CON
R10
22K
R14
10K
C8
6.8UF
2.5V REGULATOR
CORE VOL FPGA
U17
MAX1792
V2_5
C59
C77
C58
C76
C84
1UF
.1UF
V_DUT
C91
C92
68UF
C35
C40
C2
C22
C48
C30
C42
C52
C1
C69
C61
C4
C51
C63
C64
C6
C44
C18
C45
C68
C47
C50
C41
C49
C73
C53
C62
C67
C65
C85
C86
C88
C90
C66
C80
C82
C89
C60
C37
C36
C43
C26
C56
C55
C24
C38
C57
C71
C3
C87
10UF
C7
C54
C20
C23
C25
C27
C19
TITLE:
DECOUPLING CAPS
DATE:
ENGINEER:
PAGE:
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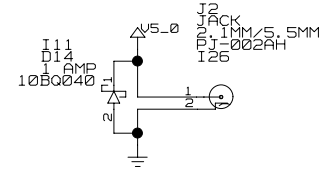
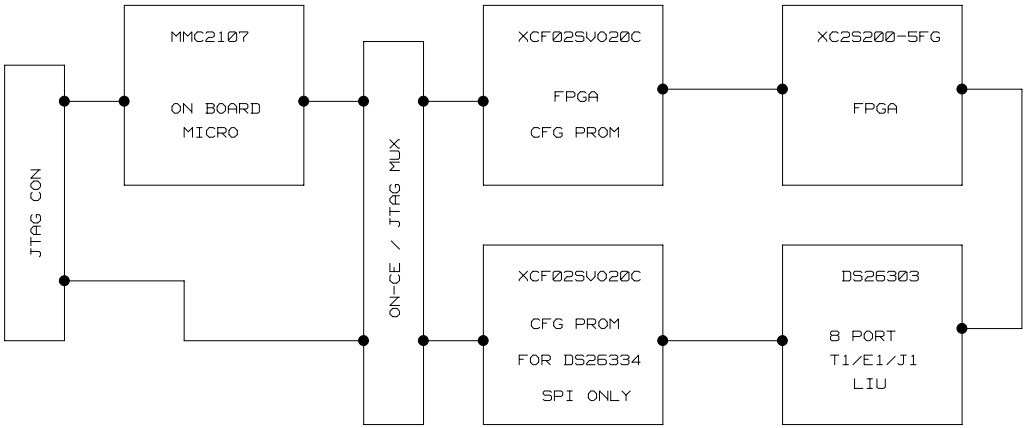
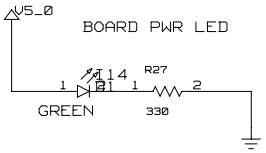
5V DC POWER SUPPLY
REVERSE BIAS PROTECTION

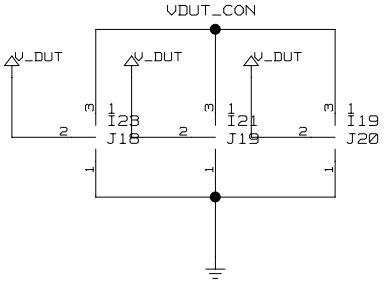




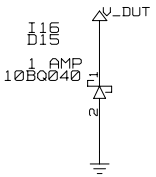


JTAG NOTES

SPLIT BOARD POWER SUPPLY
AND DUT POWER SUPPLY (V_DUT)



REVERSE BIAS PROTECTION

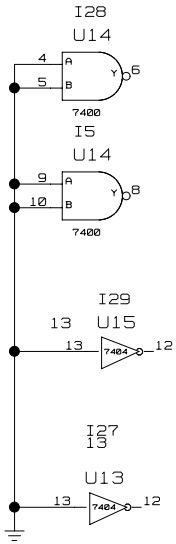


I1
0L_HARDWARE
.75STANDOFF_.25SCR
4-40KIT2
H1

I2
0L_HARDWARE
.75STANDOFF_.25SCR
4-40KIT2
H2

I3
0L_HARDWARE
.75STANDOFF_.25SCR
4-40KIT2
H3

I4
0L_HARDWARE
.75STANDOFF_.25SCR
4-40KIT2
H4



TITLE: POWER CON	DATE:
ENGINEER:	PAGE: 18

NOTES:

TITLE: NOTES	DATE:
ENGINEER:	PAGE:

*** Signal Cross-Reference for the entire design ***

```
ADDRESS_BERT_<3..0>  8C8 11A4
ADDRESS_LOCAL_<8..0>  2C7 10D6 15A5
CCLK_A               9B1< 9B3<>
CFG_DIN_A            9B1> 10B3<>
CLKA303              2B3<> 7C4<
CLKE303              2B3< 10A3<> 15B4<>
CLKOUT               10D7< 13D3<
CLKOUT_MM2107        13C1<> 13D4<
CS0_RAM              13C1<> 14D3< 14D6<
CS2_BOARD            10A4<> 13C1<>
CS303                2B7< 8C1> 10B7<> 15A3<> 16A8<
CSFPGA               10B7<> 15A3<>
CS_BERT              8B8< 10B7<> 15A3<>
DATA303_<7..0>       2C3 11A5 15B4 16B8
DATA_<7..0>          8B5 10C3 12C5
DONE_FPGA_A          9A3< 9B1< 9B3<>
E1_CLK               7B1< 11D6<
EB0                  10A4<> 13D3<> 14D3<
EB1                  10A4<> 13D3<> 14D7<
FLASH_VPP            13D7< 14A7<>
FPGA_CLKA            7C3< 7D3<> 10C3<>
FPGA_EN              10B7<> 14A8<> 15B3<>
FPGA_TECLK           7B5< 7C3< 7D3<> 10B3<>
INT303               2B3> 7B8< 7D5< 10C3<> 15B3<>
INTERUPT             10B3<> 13B2<>
JDE_B                12B2<> 13B1<>
JDS303OUT_SPI_PROM_IN  2A7> 8A2< 8D3<
JFLASHOUT_FPGAIN  9B1> 9C3<
JFPGAOUT_DS303IN  2A7< 9C3>
JTCLK                2B7< 8D3> 9B3< 9C3< 12B2< 12C3<>
                   13B2<>
JTDI                 12C3<> 13D2<>
JTDO                 8A1< 8D3> 12C4<>
JTMS                 2A7< 8D3< 9B3< 9C3< 12B1< 12C3<>
JTMS_MIC             12B2<> 12C4<> 13B2<>
JTRST_B              2B7< 12B2<> 13B2<>
LED_RLOS1            7B4> 7D7<>
MCLK303              2B3< 7C4< 8C3<
MCLK_FPGA            7C3< 10C3<>
MICROADD_<17..0>  10B7 13B4 14B4 14B8
MICRODATA_<15..0>  10A5 10D5 13B8 14C2 14C5
MISO                 10B7<> 13A2<>
MODESEL303           2C7< 10B3<> 15A3<> 16A7<
MOSI                 10B7<> 13A2<>
MOTEL303             2B7< 10B3<> 15B3<>
MUX303               2B7< 10B3<> 15A4<>
OE                   10A4<> 13D7<> 14D3< 14D7<
OE303                2C3< 10B3<> 15B3<>
ONCE_TDO_FLASHIN  9B3< 12C4<> 13D2<>
OSC_MCU              13B2<> 13B4<>
PD16                 13B8<> 14B3<
PD17                 13B8<> 14B3<
PD18                 13B8<> 14A4<
PD19                 13B8<> 14A2<
PD20                 13B8<>
PD21                 13C8<> 14B2<
PD22                 13C8<> 14B2<
PD23                 13C8<> 14B2<
PD24                 13C8<>
PD25                 13C8<>
PD26                 13C8<> 14B3<
PD27                 13C8<>
PD28                 13C8<> 14A2<
PD29                 13C8<>
PD30                 13C8<>
PD31                 13C8<>
PROGRAM_FPGA_A   9B1> 9B3<
PRT1_IN              12A6<> 12A8<
PRT1_OUT             12A6<> 12A6>
PWREN_USB            10D4<> 12B5>
RCLK303_<8..1>    11A6 15C5 15C8 15D3> 15D6 15D8<
                  16C6 16C8
RCLK303_DUT<8..1>  3B1> 3B4> 3C1> 3C4> 4A1> 4A5>
                  4C1> 4C5> 16C5 16C7
RCLKENABLE_BERT  8A6< 8D7< 10A6<> 15A8<>
RCLKIN_BERT      8D7< 10A6<> 15A8<>
RCON             10A4<> 13D7<> 14A2<
RDAT_BERT        8D8< 10A6<> 15A8<>
RD_LOCAL         2B7< 8B8< 10B7<> 15A3<>
RD_USB           10A6<> 12C5>
RESET            12B3<> 13A7<
RESET_B          9B1<> 13A8<> 17C6> 17C8> 17D3>
RESET_CFGPRM     8A3<> 8C3<>
RESET_MIC        13A6> 13C1<>
RLOS303_<8..1>   2B3 7C5< 7C8 11D4 15C5 15C8 15D3>
                 15D6 15D8<
RLOSCON_1          7B5< 10D4<>
RNEG303_<8..1>   11B3 15C5 15C8 15D3> 15D6 15D8<
                 16B5 16B7
RNEG303_DUT<8..1>  3B1> 3B4> 3C1> 3C4> 4B1> 4B5>
                 4C1> 4C5> 16B6 16B8
RPOS303_<8..1>   11B7 15C5 15C8 15D3> 15D6 15D8<
                 16C1 16C3
RPOS303_DUT<8..1>  3B1> 3B4> 3C1> 3C4> 4B1> 4B5>
                 4C1> 4C5> 16C3 16C4
RRING303_<8..1>  3B4< 3B8< 3C4< 3C8< 4B4< 4B8< 4C4<
                 4C8< 5A1> 5A5> 5C1> 5C5> 6A1> 6A5>
                 6B5> 6C1>
RTIP303_<8..1>   3B4< 3B8< 3D4< 3D8< 4B4< 4B8< 4C4<
                 4C8< 5A5> 5B1> 5C1> 5C5> 6A1> 6A5>
                 6C1> 6C5>
RUN_KIT_USR      13B3<> 14B6<
RW               10A4<> 13D7<>
RXF_USB          10B3<> 12B5>
R_PB_CFG         8A2<> 8B2>
SCANMODE303      2A3< 7D5<
SCI1_IN          12A6> 13B4<>
SCI1_OUT         12A8< 13C4<>
SCK              10B7<> 13C1<>
SCLK_ALE303      2B7< 8C1> 10B7<> 15A3<>
SDI_WR_LOCAL     2B7< 8B8< 8C1> 10A7<> 15A3<>
SDO_RDY303       2C7> 10B3<> 15B4<>
SIWU_USB         10D4<> 12B5>
SS               10B7<> 13B1<>
T1_CLK           7B1< 11C7<
TA               10A3<> 13D7<>
TCLK303_<8..1>   3B4< 3B8< 3C4< 3C8< 4A4< 4A8< 4C4<
                 4C8< 11B3 15C5 15C8 15D3> 15D6 15D8<

TCLKENABLE_BERT  8A6< 8B8< 10A5<> 15A8<>
TCLKIN_BERT      8B8< 10A5<> 15A8<>
TCLKOUT_BERT     8D5< 10A6<> 15A8<>
TDAT_BERT        8C5< 10A6<> 15A8<>
TEA              10A3<> 13D7<>
TEST             13C3<>
TIM_16H_8L       13A3< 13D3<> 14B5<
TNEG303_<8..1>   3B4< 3B8< 3C4< 3C8< 4B4< 4B8< 4C4<
                 4C8< 11D5 15C5 15C8 15D3> 15D6 15D8<

TPOS303_<8..1>   3B4< 3B8< 3C4< 3C8< 4B4< 4B8< 4C4<
                 4C8< 11A7 15C5 15C8 15D3> 15D6 15D8<

TRING303_<8..1>  3B1> 3B5> 3C1> 3C5> 4B1> 4B5> 4C1>
                 4C5> 5B1> 5B5> 5D1> 5D5> 6B1> 6B5>
                 6D1> 6D5>
TTIP303_<8..1>   3B1> 3B5> 3D1> 3D5> 4B1> 4B5> 4C1>
                 4C5> 5B1> 5B5> 5D1> 5D5> 6B1> 6B5>
                 6D1> 6D5>
TXE_USB            10B3<> 12B5<
USER_CLK         7A2<> 10C7<
USER_IN1         13A2< 13B3<> 15B3<>
USER_IN2         13A2< 13B3<> 15B3<>
USER_LED1        13A2< 13B3<>
USER_LED2        13A2< 13B3<>
VDDSYN           13D6<>
VDUT_CON         17D4<> 18A7<>
VSSSSYN          13A4<
WR_USB           10A4<> 12B5>
XTAL             13A3<> 13B2<>
```

TITLE:	DATE:
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*** Part Cross-Reference for the entire design ***

C1	CAP1	17B6
C2	CAP1	17B7
C3	CAP1	17A5
C4	CAP1	17A6
C5	CAP1	17A3
C6	CAP1	17B5
C7	CAP1	17A5
C8	CAP1	17C4
C9	CAP1	17A3
C10	CAP1	5D6
C11	CAP1	5D2
C12	CAP1	5B6
C13	CAP1	5B2
C14	CAP1	6D6
C15	CAP1	6B6
C16	CAP1	6B2
C17	CAP1	6D2
C18	CAP1	17B4
C19	CAP1	12A8
C20	CAP1	17A4
C21	CAP1	12A7
C22	CAP1	17B7
C23	CAP1	17A4
C24	CAP1	17A6
C25	CAP1	17A4
C26	CAP1	17A7
C27	CAP1	12A8
C28	CAP1	12A6
C29	CAP1	12C8
C30	CAP1	17A7
C31	CAP1	12B8
C32	CAP1	13A4
C33	CAP1	13A4
C34	CAP1	12D7
C35	CAP1	17B8
C36	CAP1	17A8
C37	CAP1	17A8
C38	CAP1	17A6
C39	CAP1	12D7
C40	CAP1	17B7
C41	CAP1	17A5
C42	CAP1	17A7
C43	CAP1	17A7
C44	CAP1	17B5
C45	CAP1	17A4
C46	CAP1	17B4
C47	CAP1	17B4
C48	CAP1	17A8
C49	CAP1	17A4
C50	CAP1	17A5
C51	CAP1	17A6
C52	CAP1	17A7
C53	CAP1	17A4
C54	CAP1	17A5
C55	CAP1	17A7
C56	CAP1	17A7
C57	CAP1	17A6
C58	CAP1	17C1
C59	CAP1	17C2
C60	CAP1	17A1
C61	CAP1	17B5
C62	CAP1	17B2
C63	CAP1	17A6
C64	CAP1	17A5
C65	CAP1	17B2
C66	CAP1	17A2
C67	CAP1	17B2
C68	CAP1	17B4
C69	CAP1	17B6
C70	CAP1	6C2
C71	CAP1	17A6
C72	CAP1	5C5
C73	CAP1	17A4
C74	CAP1	6A1
C75	CAP1	5C2
C76	CAP1	17C1
C77	CAP1	17C2
C78	CAP1	6A5
C79	CAP1	5A5
C80	CAP1	17A2
C81	CAP1	6C5
C82	CAP1	17A2
C83	CAP1	5A1
C84	CAP1	17C1
C85	CAP1	17B2
C86	CAP1	17B1
C87	CAP1	17A5
C88	CAP1	17B1
C89	CAP1	17A1
C90	CAP1	17A2
C91	CAP1	17B1
C92	CAP1	17B1
D1	LED	18B7
D2	LED	14A7
D3	LED	7B7
D4	LED	7D7
D5	LED	7C7
D6	LED	7D7
D7	LED	7C7
D8	LED	7D7
D9	LED	7C7
D10	LED	7D7
D11	LED	7C7
D12	LED	9A2
D13	SCHOTTKYDIODE1	17D4
D14	SCHOTTKYDIODE1	18D8
D15	SCHOTTKYDIODE1	18A6
H1	4_40_HDWR	18B1
H2	4_40_HDWR	18B1
H3	4_40_HDWR	18A1
H4	4_40_HDWR	18A1
J1	CONN_40P	15A5
J2	POWER_JACK	18D8
J3	USB_BCON_U	12D8
J4	CONN_DB9P	12A5
J5	CONN_BNC_5P	7D1
J6	CONN_14P	12C3
J7	CONN_BNC_5P	7A2
J8	CONN_BNC_5P	7D1
J9	CONN_14P	15D7
J10	CONN_14P	15B8
J11	CONN_14P	15D7
J12	CONN_14P	15C7
J13	CONN_14P	15D5
J14	CONN_14P	15B6
J15	CONN_14P	15D5
J16	CONN_14P	15C4
J17	CONN_14P	15A7
J18	JMP3	18A8
J19	JMP3	18A7
J20	JMP3	18A7
J21	CONN_BNC_5P	5C7
J22	CONN_BNC_5P	5C3
J23	CONN_BNC_5P	5A7
J24	CONN_BNC_5P	5A3
J25	CONN_BNC_5P	6C7
J26	CONN_BNC_5P	6A7
J27	CONN_BNC_5P	6A3
J28	CONN_BNC_5P	6C3
J29	CONN_BNC_5P	5D7
J30	CONN_BNC_5P	5D3
J31	CONN_BNC_5P	5B7
J32	CONN_BNC_5P	5B3
J33	CONN_BNC_5P	6D7
J34	CONN_BNC_5P	6B7
J35	CONN_BNC_5P	6B3
J36	CONN_BNC_5P	6D3
J37	JMP_OPEN_2P	5D7
J38	JMP_OPEN_2P	5D3
J39	JMP_OPEN_2P	5B6
J40	JMP_OPEN_2P	5B3
J41	JMP_OPEN_2P	6D7
J42	JMP_OPEN_2P	6B6
J43	JMP_OPEN_2P	6B3
J44	JMP_OPEN_2P	6D3
J45	RJ45_8	5B4 5B8 5D4 5D8
J46	RJ45_8	6B4 6B8 6D4 6D8
L1	COIL_2P	13D6
R1	RES1	8A7
R2	RES1	8B7
R3	RES1	16C6
R4	RES1	16D4
R5	RES1	16C6
R6	RES1	16C7
R7	RES1	16D2
R8	RES1	16D4
R9	RES1	16C7
R10	RES1	17D5
R11	RES1	16D4
R12	RES1	16C6
R13	RES1	7C4
R14	RES1	17C5
R15	RES1	7D5
R16	RES1	16B7
R17	RES1	16B5
R18	RES1	16B6
R19	RES1	16B7
R20	RES1	16B7
R21	RES1	16B5
R22	RES1	16B6
R23	RES1	16B7
R24	RES1	13A1
R25	RES1	13A1
R26	RES1	7D5
R27	RES1	18B7
R28	RES1	16B8
R29	RES1	12C8
R30	RES1	12D7
R31	RES1	12C8
R32	RES1	16A7
R33	RES1	16A8
R34	RES1	16B8
R35	RES1	16B6
R36	RES1	16B5
R37	RES1	16B8
R38	RES1	16A7
R39	RES1	16A8
R40	RES1	16B8
R41	RES1	16B6
R42	RES1	16B5
R43	RES1	12A5
R44	RES1	7D2
R45	RES1	7B2
R46	RES1	12C1
R47	RES1	12C1
R48	RES1	12A4
R49	RES1	12A5
R50	RES1	13A7
R51	RES1	13A4
R52	RES1	12C3
R53	RES1	12D6
R54	RES1	13A7
R55	RES1	12B2
R56	RES1	12B1
R57	RES1	14A2
R58	RES1	8A2
R59	RES1	12C7
R60	RES1	7C2
R61	RES1	7D2
R62	RES1	13D4
R63	RES1	14B3
R64	RES1	14B6
R65	RES1	14A2
R66	RES1	14A5
R67	RES1	14A7
R68	RES1	14B2
R69	RES1	13A1
R70	RES1	7B6
R71	RES1	14B2
R72	RES1	13A2
R73	RES1	14A4
R74	RES1	7C6
R75	RES1	7D6
R76	RES1	13A1
R77	RES1	14B3
R78	RES1	8C5
R79	RES1	8D5
R80	RES1	7C6
R81	RES1	7D6
R82	RES1	8B7
R83	RES1	7C6
R84	RES1	7D6
R85	RES1	14B2
R86	RES1	14B3
R87	RES1	8A7
R88	RES1	14A2
R89	RES1	7C6
R90	RES1	7D6
R91	RES1	7A5
R92	RES1	7A2
R93	RES1	8A3
R94	RES1	16D6
R95	RES1	16D7
R96	RES1	8A5
R97	RES1	8A6
R98	RES1	16D2
R99	RES1	16D6
R100	RES1	16C7
R101	RES1	7C4
R102	RES1	16D7
R103	RES1	6C2
R104	RES1	7C4
R105	RES1	6A2
R106	RES1	6C2
R107	RES1	5C6
R108	RES1	5C6
R109	RES1	6A2
R110	RES1	6A6
R111	RES1	5C2
R112	RES1	6A6
R113	RES1	5C2
R114	RES1	5A6
R115	RES1	6C6
R116	RES1	5A6
R117	RES1	16D6
R118	RES1	6C6
R119	RES1	5A2
R120	RES1	16C6
R121	RES1	16D2
R122	RES1	5A2
R123	RES1	9A2
R124	RES1	16D4
R125	RES1	16D6
R126	RES1	16D7
R127	RES1	16D2
R128	RES1	16C7
R129	RES1	16D7
R130	RES1	7D4
SW2	PUSHBUTTON	13A8
SW3	SWITCH_DPDT_SLIDE_6P	14A6
SW4	SWITCH_DPDT_SLIDE_6P	12C4
SW5	SWITCH_DPDT_SLIDE_6P	14A8
SW6	PUSHBUTTON	8B3
SW7	SWITCH_DPDT_SLIDE_6P	8A2
T1	XFMR_QUADPORT_T1_U	5A2 5A6 5B2 5B6 5C2 5C6 5D3 5D6
T2	XFMR_QUADPORT_T1_U	6A2 6A6 6B2 6B6 6C2 6C6 6D3 6D6
U1	FT245BM_U	12C6
U2	MMC2107_1	13C2 13C6
U3	CY62128V_2	14C7
U4	DS2174	8C7
U5	XC2S_FG256	9C6 10C5 11C5
U6	DS26303_DALM	2D6 3B3 3B6 3C3 3C6 4B3 4B6 4C3 4C6
U7	XC18V02VQ44C	8D3

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U8	DS232 12A7
U9	NC7SZ86_U 7D2
U10	MAX1793_U 17D7
U11	CY62128V_2 14C3
U12	NC7SZ86_U 7D2
U13	74_04_U 7D7 7D8 9A3 13A6 18A2
U14	74_00 7B4 13A6 18B2
U15	74_04_U 7B7 7C7 7C7 7C8 7C8 18A2
U16	MAX6816_2 8B2
U17	MAX1792_1 17D3
U18	MAX1793_U 17D5
U19	XCFS_V020 9B2
X1	XTAL_U 12C7
X2	XTAL 13A4
Y1	OSC2 7B2
Y2	OSC2 7C2

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