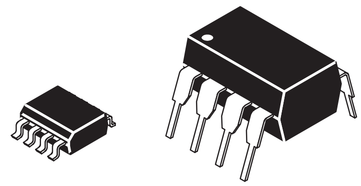


DIFFERENTIAL BUS TRANSCEIVER

FEATURES

- **One-Fourth Unit Load Allows up to 128 Devices on a Bus**
- **ESD Protection for Bus Terminals:**
  - **±15-kV Human Body Model**
  - **±8-kV IEC61000-4-2, Contact Discharge**
  - **±15-kV IEC61000-4-2, Air-Gap Discharge**
- **Meets or Exceeds the Requirements of ANSI Standard TIA/EIA-485-A and ISO 8482: 1987(E)**
- **Controlled Driver Output-Voltage Slew Rates Allow Longer Cable Stub Lengths**
- **Designed for Signaling Rates† Up to 250-kbps**
- **Low Disabled Supply Current . . . 250 μA Max**
- **Thermal Shutdown Protection**
- **Open-Circuit Fail-Safe Receiver Design**
- **Receiver Input Hysteresis . . . 70 mV Typ**
- **Glitch-Free Power-Up and Power-Down Protection**

APPLICATIONS

- **Utility Meters**
- **Industrial Process Control**
- **Building Automation**

DESCRIPTION

The SN65LBC182 and SN75LBC182 are differential data line transceivers with a high level of ESD protection in the trade-standard footprint of the SN75176. They are designed for balanced transmission lines and meet ANSI standard TIA/EIA-485-A and ISO 8482. The SN65LBC182 and SN75LBC182 combine a 3-state, differential line driver and differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected together to function as a direction control.

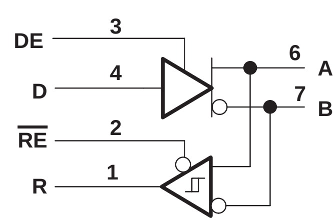
The driver outputs and the receiver inputs connect internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus. This port operates over a wide range of common-mode voltage, making the device suitable for party-line applications. The device also includes additional features for party-line data buses in electrically noisy environment applications such as industrial process control or power inverters.

The SN75LBC182 and SN65LBC182 bus pins also exhibit a high input resistance equivalent to one-fourth unit load allowing connection of up to 128 similar devices on the bus. The high ESD tolerance protects the device for cabled connections. (For an even higher level of protection, see the SN65/75LBC184, literature number SLLS236.)

The differential driver design incorporates slew-rate-controlled outputs sufficient to transmit data up to 250 kbps. Slew-rate control allows longer unterminated cable runs and longer stub lengths from the main backbone than possible with uncontrolled voltage transitions. The receiver design provides a fail-safe output of a high level when the inputs are left floating (open circuit). Very low device supply current can be achieved by disabling the driver and the receiver.

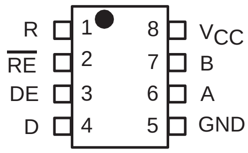
The SN65LBC182 is characterized for operation from −40°C to 85°C, and the SN75LBC182 is characterized for operation from 0°C to 70°C.

functional block diagram

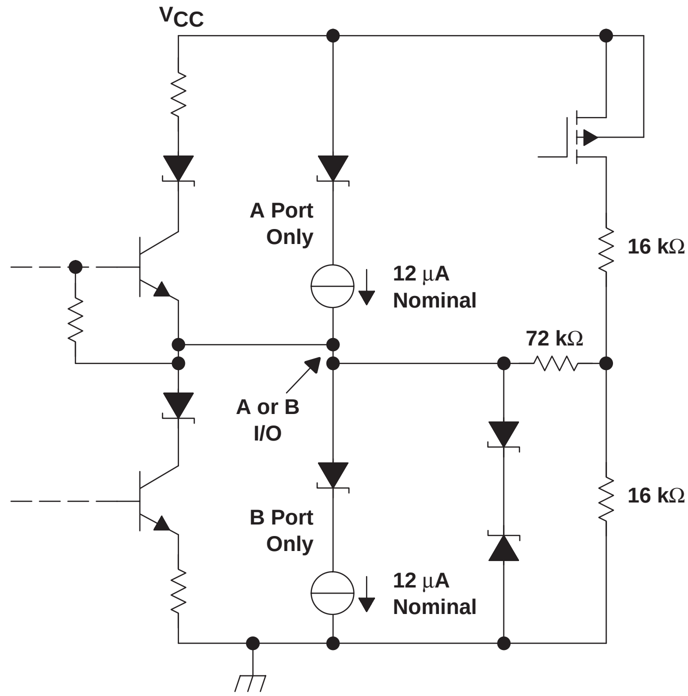


† The signaling rate of a line, is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

SN65LBC182D (Marked as 6LB182)
SN75LBC182D (Marked as 7LB182)
SN65LBC182P (Marked as 65LBC182)
SN75LBC182P (Marked as 75LBC182)
(TOP VIEW)



schematic of inputs and outputs



Function Tables

DRIVER

INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z
Open	H	H	L

RECEIVER

DIFFERENTIAL INPUTS	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
$-0.2V < V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	H

AVAILABLE OPTIONS

T_A	PACKAGE	
	PLASTIC SMALL-OUTLINE† (JEDEC MS-012)	PLASTIC DUAL-IN-LINE PACKAGE (JEDEC MS-001)
0°C to 70°C	SN75LBC182D	SN75LBC182P
−40°C to 85°C	SN65LBC182D	SN65LBC182P

† Add R suffix for taped and reel.
† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

absolute maximum ratings† over operating free−air temperature range unless otherwise noted

Supply voltage range, (see Note 1) V_{CC} . . . . −0.5 V to 7 V
Voltage range at any bus terminal (A or B) . . . . −15 V to 15 V
Input voltage, V_I (D, DE, R or $\overline{RE}$) . . . . −0.3 V to 7 V
Receiver output current, I_O . . . . ±20 mA
Electrostatic discharge: Human body model (see Note 2) A, B, GND . . . . 15 kV
All pins . . . . 3 kV
Contact discharge (IEC61000-4-2) A, B, GND . . . . 8 kV
Air discharge (IEC61000-4-2) A, B, GND . . . . 15 kV
Continuous total power dissipation . . . . See Dissipation Rating Table

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
2. Tested in accordance with JEDEC Standard 22, Test Method A114-A.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1150 mW	9.2 mW/°C	736 mW	598 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

NOTE: The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus I/O terminal (separately or common mode) V_I or V_{IC}		−7		12	V
High-level input voltage, V_{IH}	D, DE, $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, DE, $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 3)		−12		12	V
Output current, I_O	Driver	−60		60	mA
	Receiver	−8		4	mA
Operating free-air temperature, T_A	SN65LBC182	−40		85	°C
	SN75LBC182	0		70	°C

NOTE 3: Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

driver electrical characteristics over recommended operating conditions

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −18 mA		−1.5			V
V_O	Output voltage		I_O = 0		0		V_{CC}	V
$\|V_{OD}\|$	Differential output voltage		R_L = 54 Ω,	See Figure 1	1.5	2.2	V_{CC}	V
			V_{test} = −7 V to 12 V,	See Figure 2	1.5	2.2	V_{CC}	V
ΔV_{OD}	Change in magnitude of differential output voltage		See Figure 1		−0.2		0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage				1		3	
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage		See Figures 1 and 4		−0.2		0.2	
$V_{OC(PP)}$	Peak-to-peak change in common-mode output voltage during state transitions					0.8		V
I_{OZ}	High-impedance output current		See receiver input currents					
I_{IH}	High-level input current (D, DE)		V_I = 2.4 V				50	μA
I_{IL}	Low-level input current (D, DE)		V_I = 0.4 V		−50			μA
I_{OS}	Short-circuit output current		V_O = −7 V to 12 V		−250		250	mA
I_{CC}	Supply current	SN75LBC182	No load, DE at V_{CC},	$\overline{RE}$ at V_{CC}		12	25	mA
		SN65LBC182				12	30	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

driver switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_r	Differential output signal rise time	R_L = 54 Ω, See Figure 3	C_L = 50 pF,	0.25	0.72	1.2	μs
t_f	Differential output signal fall time			0.25	0.73	1.2	
t_{PLH}	Propagation delay time, low-to-high-level output					1.3	
t_{PHL}	Propagation delay time, high-to-low-level output					1.3	
$t_{sk(p)}$	Pulse skew (t_{PHL} − t_{PLH})				0.075	0.15	
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 5			3.5	μs
t_{PHZ}	Output disable time from high level					3.5	
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 6			3.5	μs
t_{PLZ}	Output disable time from low level					3.5	

receiver electrical characteristics over recommended operating conditions (unless otherwise noted)

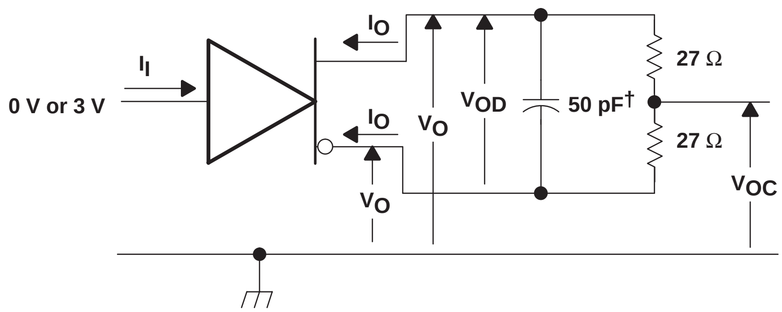
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage					0.2	V
V_{IT-}	Negative-going input threshold voltage			−0.2			V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)				70		mV
V_{IK}	Enable-input clamp voltage	$I_I = -18$ mA		−1.5			V
V_{OH}	High-level output voltage	$V_{ID} = 200$ mV, $I_O = -8$ mA,	See Figure 7	2.8			V
V_{OL}	Low-level output voltage	$V_{ID} = 200$ mV, $I_O = 4$ mA,	See Figure 7			0.4	V
I_{OZ}	High-impedance-state output current	$V_O = 0.4$ to 2.4 V				±1	µA
I_I	Bus input current	$V_{IH} = 12$ V, $V_{CC} = 5$ V	Other input at 0 V			250	µA
		$V_{IH} = 12$ V, $V_{CC} = 0$ V				250	
		$V_{IH} = -7$ V, $V_{CC} = 5$ V		−200			
		$V_{IH} = -7$ V, $V_{CC} = 0$ V		−200			
I_{IH}	High-level input current ($\overline{RE}$)	$V_{IH} = 2$ V				50	µA
I_{IL}	Low-level input current ($\overline{RE}$)	$V_{IL} = 0.8$ V		−50			µA
I_{CC}	Supply current	No load	DE at 0 V, $\overline{RE}$ at 0 V			3.5	mA
			DE at 0 V, $\overline{RE}$ at V_{CC}		175	250	µA

† All typical values are at $V_{CC} = 5$ V and $T_A = 25°C$.

receiver switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_r	Differential output signal rise time	$C_L = 50$ pF,	See Figure 7		20		ns
t_f	Differential output signal fall time				20		
t_{PLH}	Propagation delay time, low-to-high-level output					150	
t_{PHL}	Propagation delay time, high-to-low-level output					150	
t_{PZH}	Output enable time to high level	See Figure 8				100	ns
t_{PZL}	Output enable time to low level					100	
t_{PHZ}	Output disable time from high level					100	ns
t_{PLZ}	Output disable time from low level					100	
$t_{sk(p)}$	Pulse skew $\|t_{PHL} - t_{PLH}\|$					50	ns

PARAMETER MEASUREMENT INFORMATION



†Includes probe and jig capacitance

Figure 1. Driver Test Circuit, V_{OD} and V_{OC} Without Common-Mode Loading

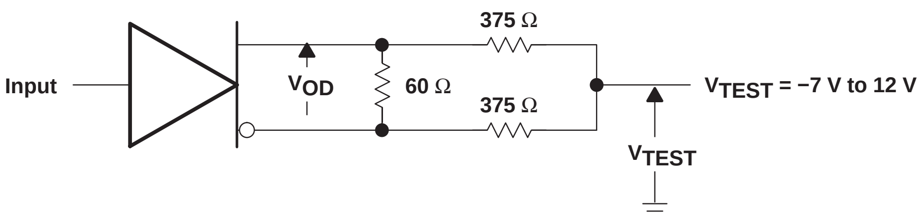
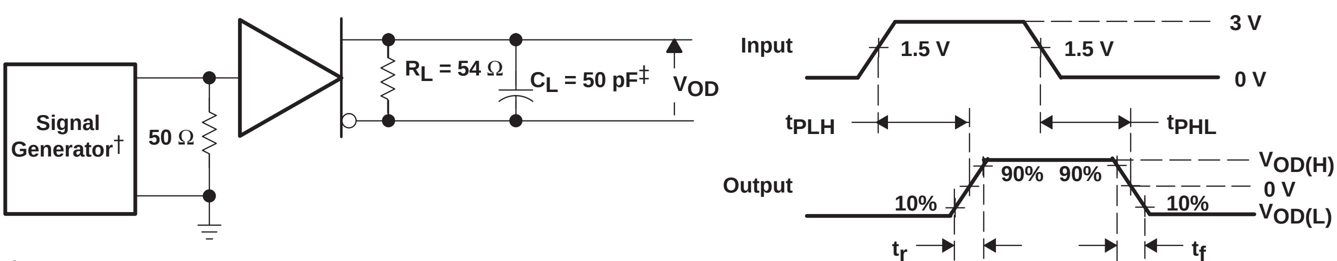


Figure 2. Driver Test Circuit, V_{OD} With Common-Mode Loading



†PRR = 1 MHz, 50% duty cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω
‡Includes probe and jig capacitance

Figure 3. Driver Switching Test Circuit and Waveforms

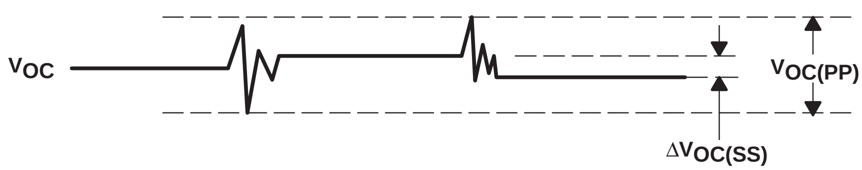
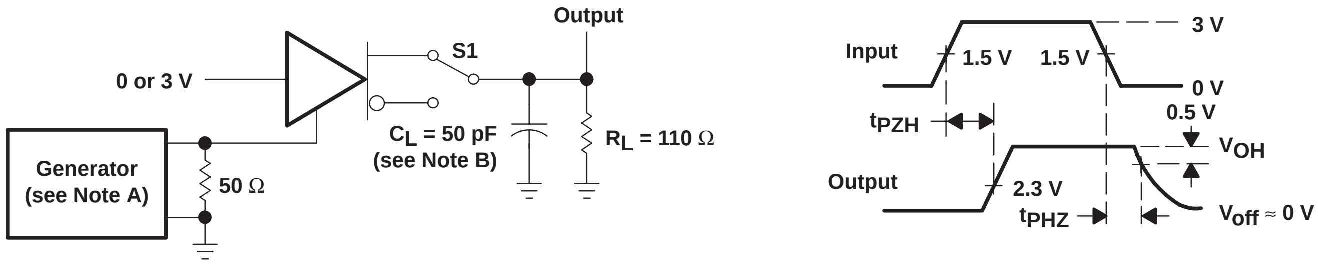


Figure 4. V_{OC} Definitions

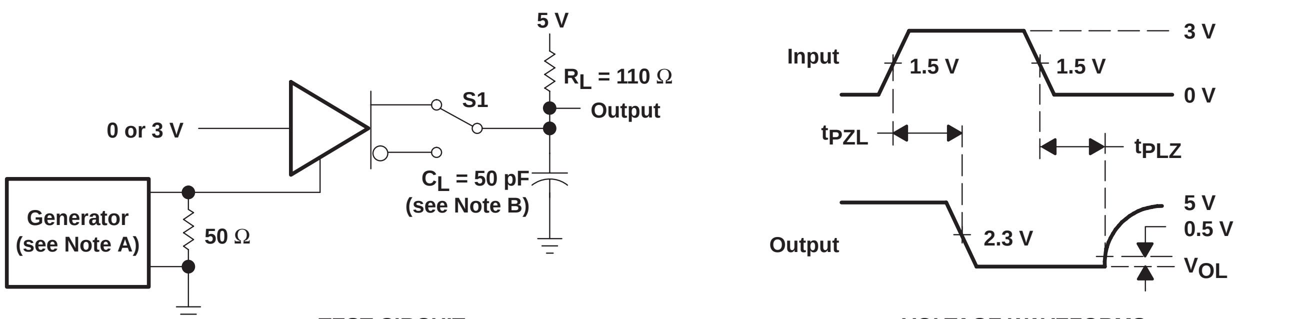
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1.25 kHz, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

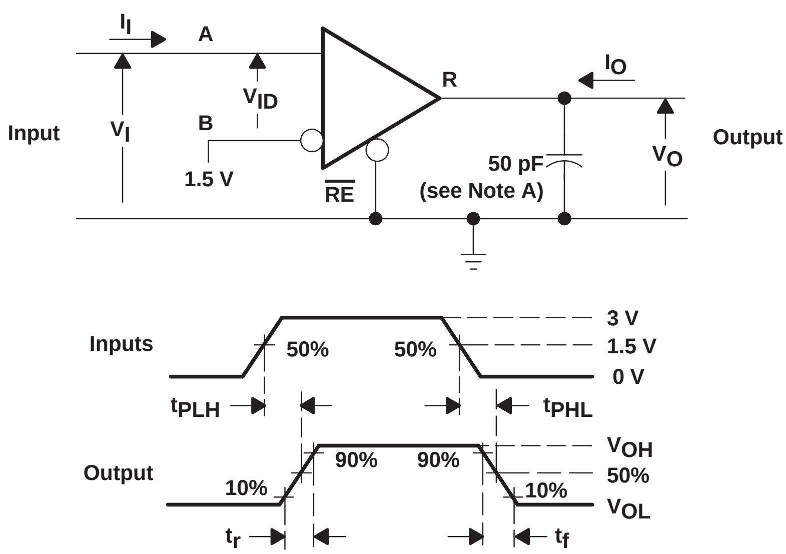
Figure 5. Driver t_{PZH} and t_{PHZ} Test Circuit and Voltage Waveforms



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1.25 kHz, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

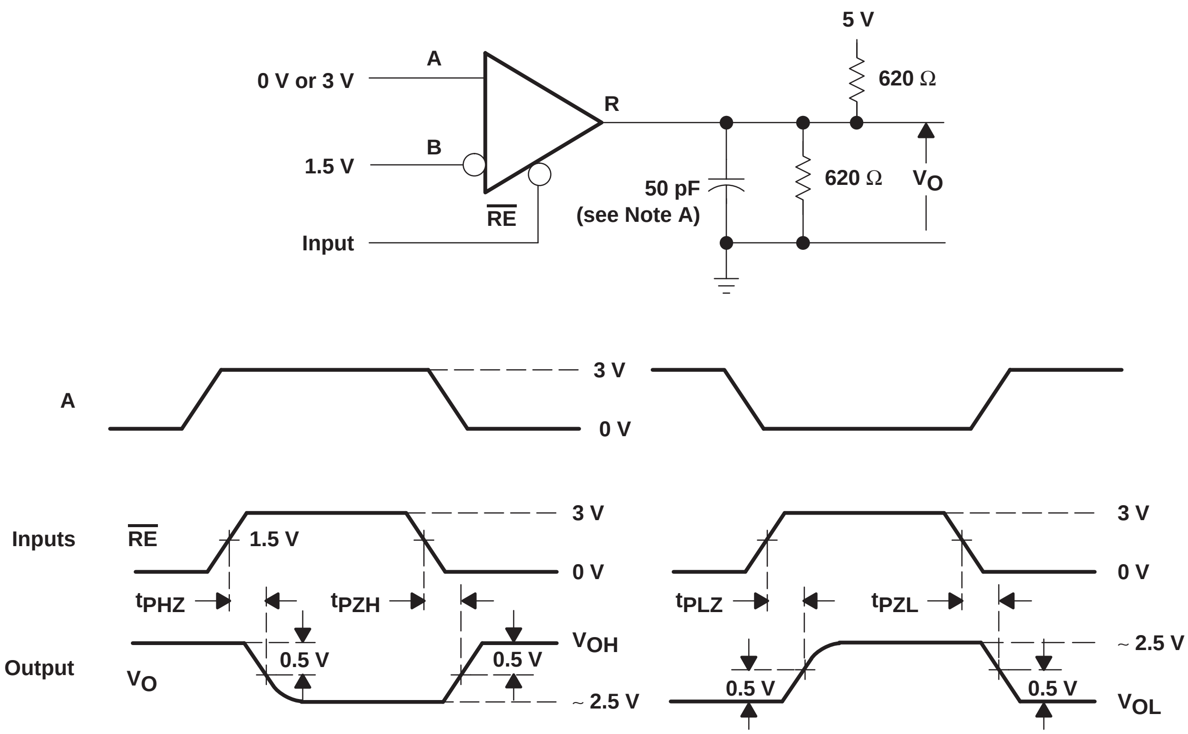
Figure 6. Driver t_{PZL} and t_{PLZ} Test Circuit and Voltage Waveforms



NOTE A: This value includes probe and jig capacitance (± 10%).

Figure 7. Receiver t_{PLH} and t_{PHL} Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: This value includes probe and jig capacitance (± 10%).

Figure 8. Receiver t_{PZL}, t_{PLZ}, t_{PZH}, and t_{PHZ} Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs TEMPERATURE

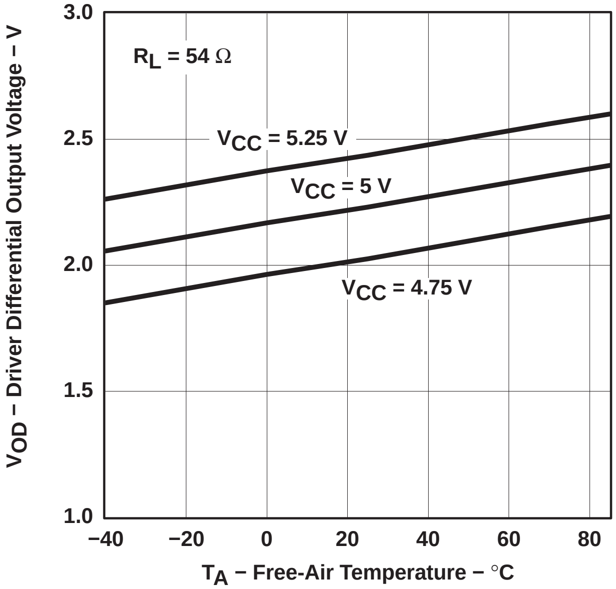


Figure 9

DRIVER PROPAGATION DELAY TIME vs TEMPERATURE

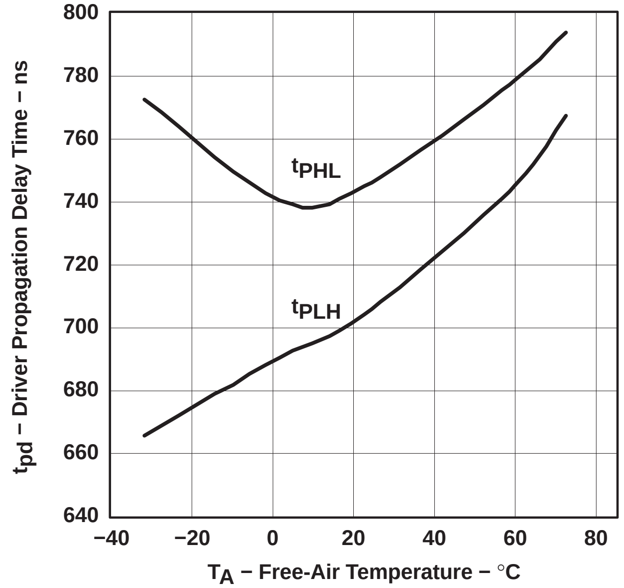


Figure 10

DRIVER TRANSITION TIME vs TEMPERATURE

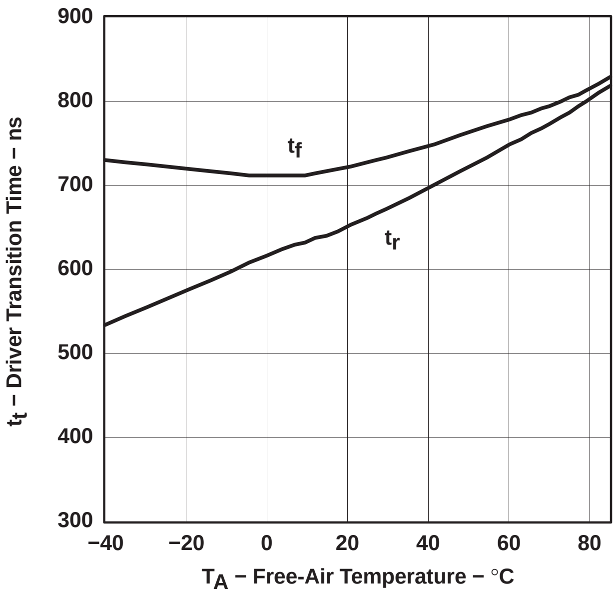


Figure 11

DIFFERENTIAL OUTPUT VOLTAGE vs OUTPUT CURRENT

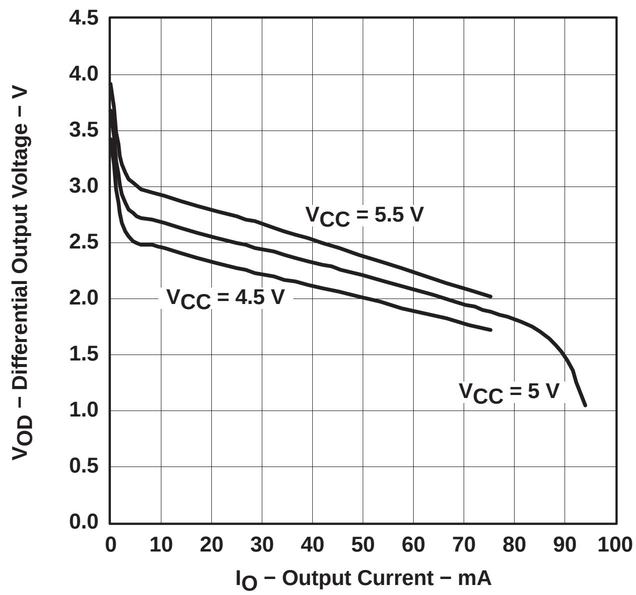


Figure 12

TYPICAL CHARACTERISTICS

RECEIVER INPUT CURRENT
vs
INPUT VOLTAGE

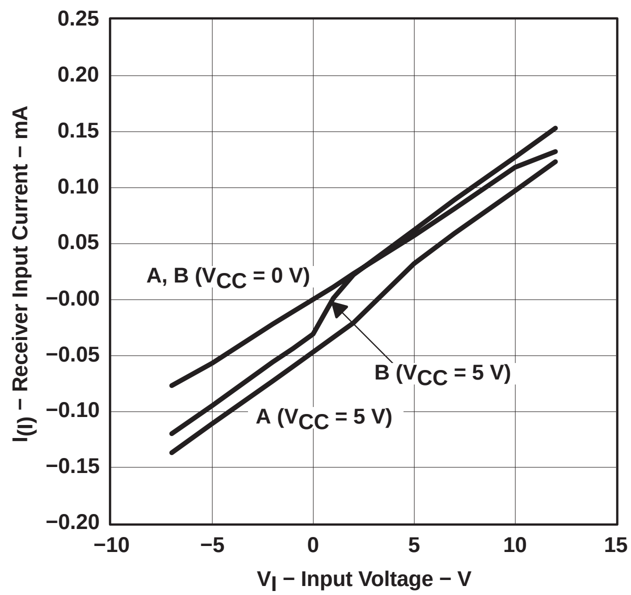
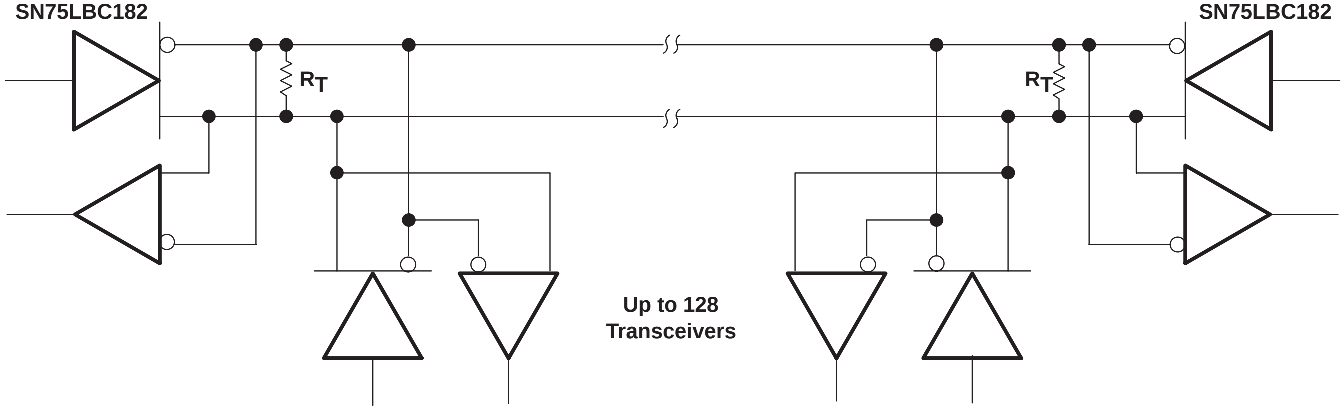


Figure 13

APPLICATION INFORMATION



NOTE A: The line should be terminated at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

Figure 14. Typical Application Circuit

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN65LBC182D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB182	Samples
SN65LBC182DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB182	Samples
SN65LBC182DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB182	Samples
SN65LBC182DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB182	Samples
SN65LBC182P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	65LBC182	Samples
SN65LBC182PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	65LBC182	Samples
SN75LBC182D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7LB182	Samples
SN75LBC182DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7LB182	Samples
SN75LBC182DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7LB182	Samples
SN75LBC182DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7LB182	Samples
SN75LBC182P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	75LBC182	Samples
SN75LBC182PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	75LBC182	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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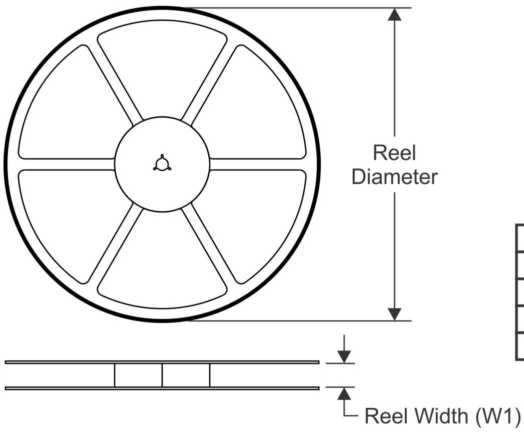
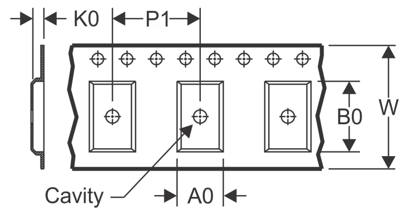
TAPE AND REEL INFORMATION

REEL DIMENSIONS

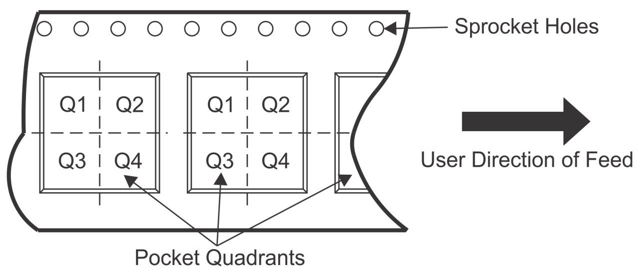


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

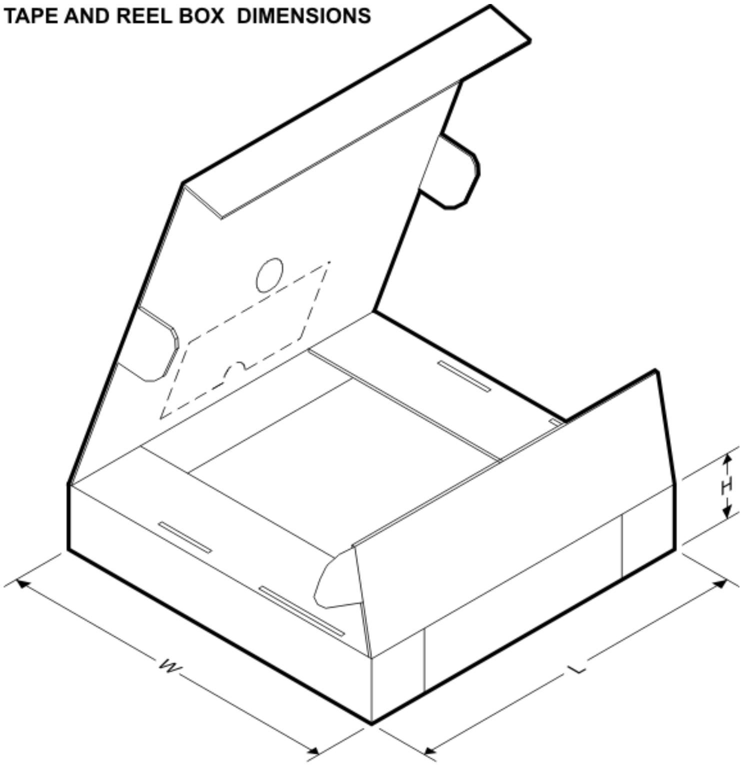
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC182DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65LBC182DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75LBC182DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

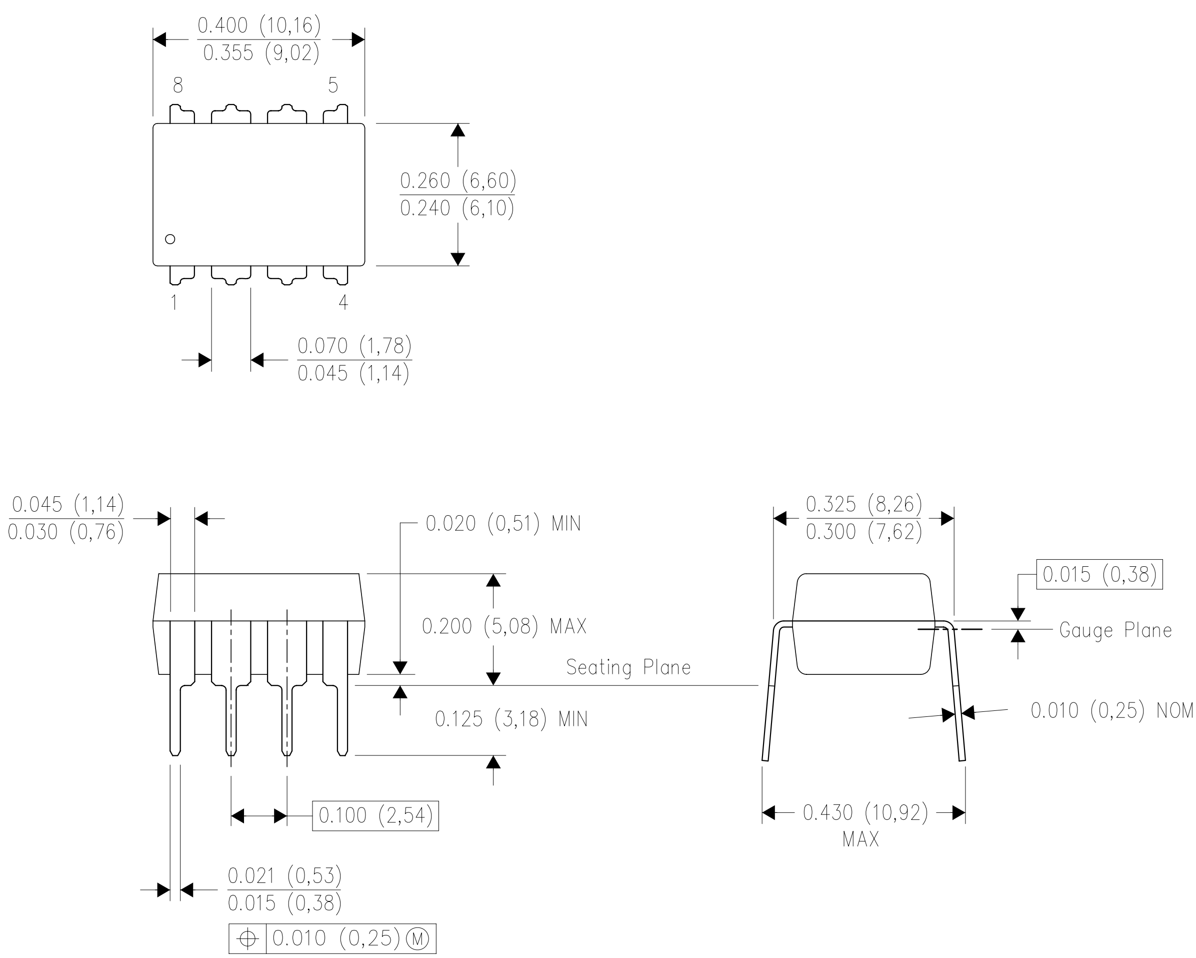
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC182DR	SOIC	D	8	2500	340.5	338.1	20.6
SN65LBC182DR	SOIC	D	8	2500	367.0	367.0	35.0
SN75LBC182DR	SOIC	D	8	2500	340.5	338.1	20.6

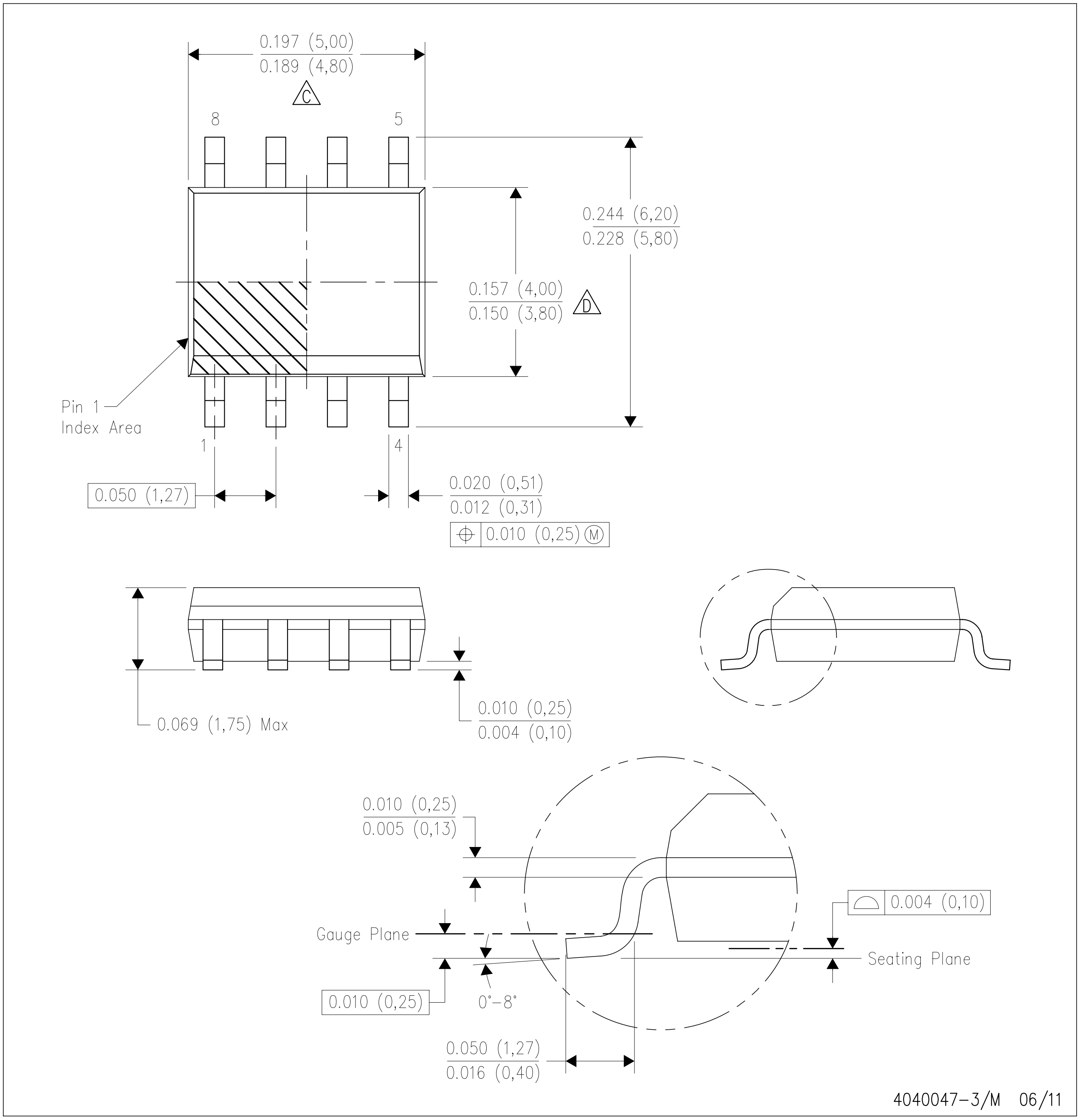
P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



4040082/E 04/2010

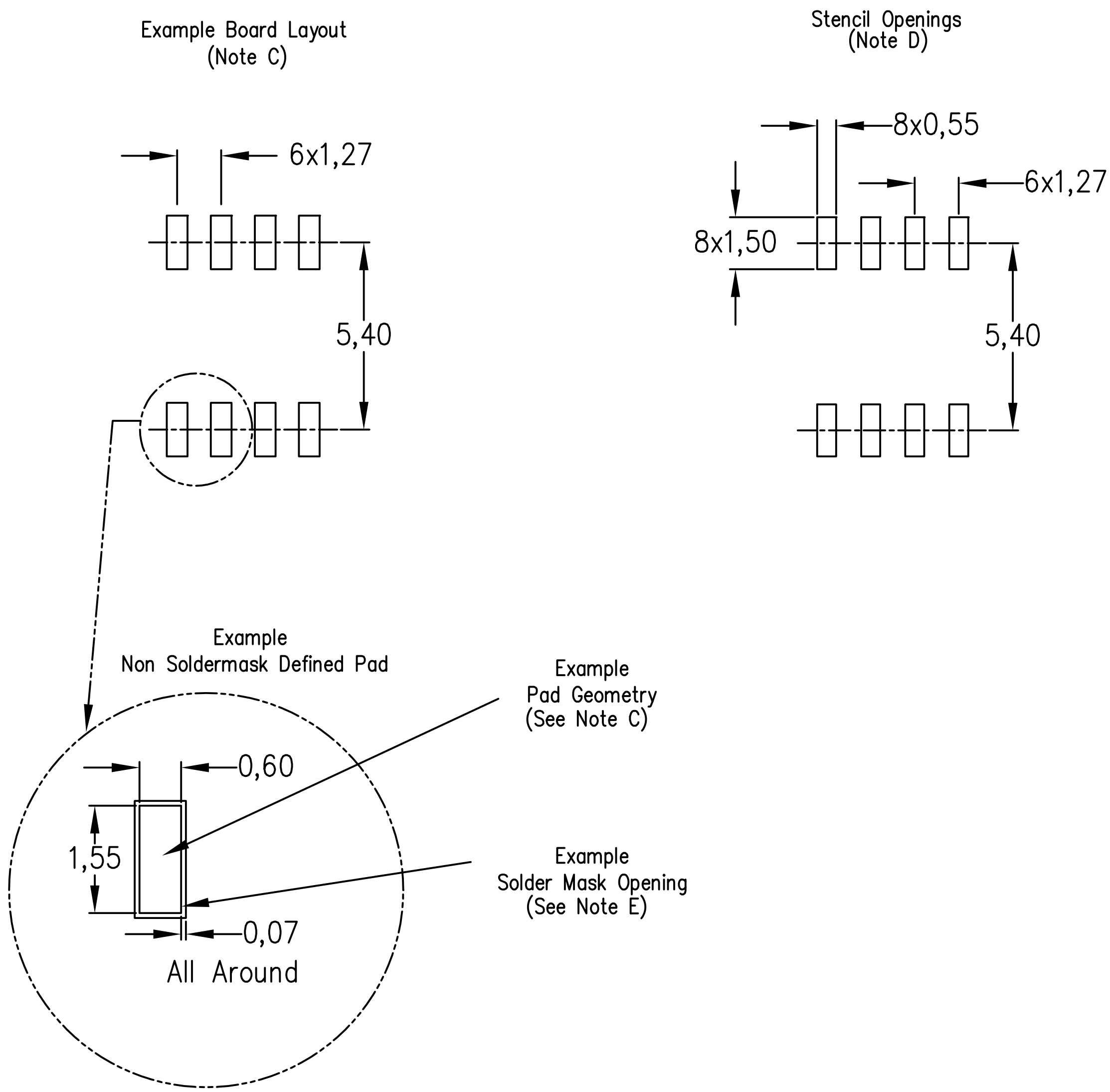
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



4211283-2/E 08/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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