

Am25LS2519

Quad Register with Two Independently Controlled Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- Two sets of fully buffered three-state outputs
- Four D-type flip-flops
- Polarity control on W outputs
- Buffered common clock enable
- Buffered common asynchronous clear
- Separate buffered common output enable for each set of outputs

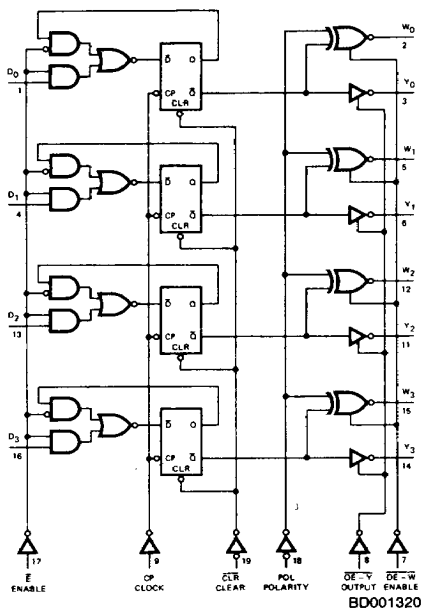
GENERAL DESCRIPTION

The Am25LS2519 consists of four D-type flip-flops with a buffered common clock enable. Information meeting the set-up and hold time requirements on the D inputs is transferred to the flip-flop outputs on the LOW-to-HIGH transition of the clock. Data on the Q outputs of the flip-flops is enabled at the three-state outputs when the output control ($\overline{OE}$) input is LOW. When the appropriate $\overline{OE}$ input is HIGH, the outputs are in the high impedance state. Two independent sets of outputs – W and Y – are provided such

that the register can simultaneously and independently drive two buses. One set of outputs contains a polarity control such that the outputs can either be inverting or non-inverting.

The device also features an active LOW asynchronous clear. When the clear input is LOW, the Q output of the internal flip-flops are forced LOW independent of the other inputs. The Am25LS2519 is packaged in a space saving (0.3-inch row spacing) 20-pin package.

BLOCK DIAGRAM

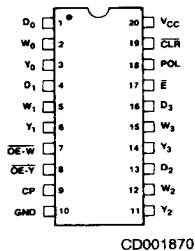


RELATED PRODUCTS

Part No.	Description
Am25S18, Am2918	Quad D Register
Am25LS2518	Quad D Register

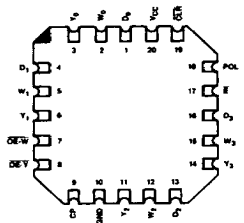
CONNECTION DIAGRAM Top View

D-20-1



CD001870

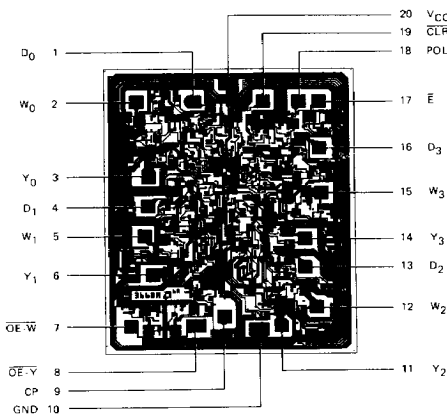
L-20-1



CD001880

Note: Pin 1 is marked for orientation

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.083" x 0.099"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25LS2519

D

C

B

Screening Option

Blank - Standard processing

B - Burn-in

Temperature (See Operating Range)

C - Commercial (0°C to +70°C)

M - Military (-55°C to +125°C)

Package

D - 20-pin Cerdip

F - 20-pin flatpak

L - 20-pin leadless chip carrier

P - 20-pin plastic DIP

X - Dice

Device type

Quad D Register

Valid Combinations

Am25LS2519

PC
DC, DM
FM
LC, LM
XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	D _i	I	Any of the four D flip-flop data lines.
17	E	I	Clock Enable. When LOW, the data is entered into the register on the next clock LOW-to-HIGH transition. When HIGH, the data in the register remains unchanged, regardless of the data in.
9	CP	I	Clock Pulse. Data is entered into the register on the LOW-to-HIGH transition.
7, 8	OE-W, OE-Y	O	Output Enable. When OE is LOW, the register is enable to the output. When HIGH, the output is in the high-impedance state. The OE-W controls the W set of outputs, and OE-Y controls the Y set.
	Y _i	O	Any of the four non-inverting three-state output lines.
	W _i	O	Any of the four three-state outputs with polarity control.
18	POL	O	Polarity Control. The W _i outputs will be non-inverting when POL is LOW, and when it is HIGH, the outputs are inverting.
19	CLR	I	Asynchronous Clear. When CLR is LOW, the internal Q flip-flops are reset to LOW.

FUNCTION TABLE

FUNCTION	INPUTS								INTERNAL	OUTPUTS	
	CP	D _i	E	CLR	POL	OE-W	OE-Y	Q		W _i	Y _i
Output Three-State Control	X	X	X	X	X	H	L	NC		Z	Enabled
	X	X	X	X	X	L	H	NC		Enabled	Z
	X	X	X	X	X	H	H	NC		Z	Enabled
	X	X	X	X	X	L	L	NC		Enabled	Z
W _i Polarity	X	X	X	X	L	L	L	NC		Non-Inverting	Non-Inverting
	X	X	X	X	H	L	L	NC		Inverting	Non-Inverting
Asynchronous Clear	X	X	X	L	L	L	L	L		L	L
	X	X	X	L	H	L	L	L		H	L
Clock Enabled	↑	X	H	H	X	X	X	NC		NC	NC
	↑	L	L	H	L	L	L	L		L	L
	↑	L	L	H	H	L	L	L		H	L
	↑	H	L	H	L	L	L	H		H	H
	↑	H	L	H	H	L	L	H		L	H

L = LOW

H = HIGH

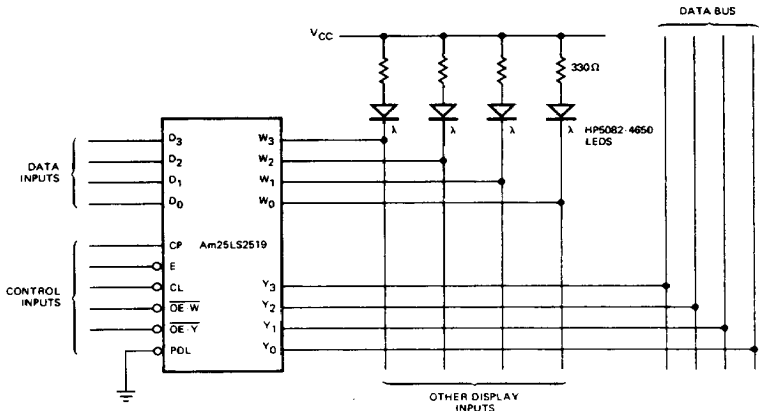
Z = High-Impedance

X = Don't Care

NC = No Change

↑ = LOW to HIGH Transition

APPLICATION



Convenient Register Content Monitor or Test Point

ABSOLUTE MAXIMUM RATINGS

Storage Temperature -65°C to +150°C
 Ambient Temperature Under Bias -55°C to +125°C
 Supply Voltage to Ground Potential
 Continuous -0.5V to +7.0V
 DC Voltage Applied to Outputs For
 High Output State -0.5V to +V_{CC} max
 DC Input Voltage -0.5V to +7.0V
 DC Output Current, Into Outputs 30mA
 DC Input Current -30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Temperature 0°C to +70°C
 Supply Voltage +4.75V to +5.25V

Military (M) Devices

Temperature -55°C to +125°C
 Supply Voltage +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
V _{OH}	Output HIGH Voltage	V _{CC} = MIN V _{IN} = V _{IH} or V _{IL}	MIL, I _{OH} = -1.0mA COM'L, I _{OH} = -2.6mA	2.4 2.4	3.4 3.4		Volts
V _{OL}	Output LOW Voltage	V _{CC} = MIN V _{IN} = V _{IH} or V _{IL}	I _{OL} = 4.0 mA I _{OL} = 8.0mA I _{OL} = 12mA			0.4 0.45 0.5	Volts
V _{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V _{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs.				0.7 0.8	Volts
V _I	Input Clamp Voltage	V _{CC} = MIN, I _{IN} = -18mA				-1.5	Volts
I _{IL}	Input LOW Current	V _{CC} = MAX, V _{IN} = 0.4V				-0.36	mA
I _{IH}	Input HIGH Current	V _{CC} = MAX, V _{IN} = 2.7V				20	μA
I _I	Input HIGH Current	V _{CC} = MAX, V _{IN} = 7.0V				0.1	mA
I _{oz}	Off-State (High-Impedance) Output Current	V _{CC} = MAX	V _O = 0.4V V _O = 2.4V			-20 20	μA
I _{SC}	Output Short Circuit Current (Note 3)	V _{CC} = MAX		-15		-85	mA
I _{CC}	Power Supply Current (Note 4)	V _{CC} = MAX	MIL COM'L		24 24	36 39	mA

- Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
 2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
 3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
 4. Inputs grounded; outputs open.

SWITCHING CHARACTERISTICS ($T_A = +25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$)

Parameters	Description		Test Conditions	Min	Typ	Max	Units
t _{PHL}	Clock to Y _i		C _L = 15pF R _L = 2.0kΩ		22	33	ns
t _{PHL}					20	30	
t _{PLH}	Clock to W _i (Either Polarity)				24	36	ns
t _{PHL}					24	36	
t _{PHL}	Clear to Y _i				29	43	ns
t _{PLH}	Clear to W _i				25	37	ns
t _{PHL}					30	45	
t _{PLH}	Polarity to W _i				23	34	ns
t _{PHL}					25	37	
t _{pw}	Clear			18			ns
t _{pw}	Clock Pulse Width	LOW		15			ns
		HIGH		18			
t _s	Data			15			ns
t _h	Data			5			ns
t _s	Data Enable			20			ns
t _h	Data Enable			0			ns
t _s	Set-up Time, Clear Recovery (Inactive) to clock			20	15		ns
t _{ZH}	Output Enable to W or Y				11	17	ns
t _{ZL}					13	20	
t _{HZ}	Output Enable to W or Y		C _L = 5.0pF R _L = 2.0kΩ	13	20	ns	
t _{LZ}				11	17		
f _{max}	Maximum Clock Frequency (Note 1)		C _L = 15pF R _L = 2.0kΩ	35	45	MHz	

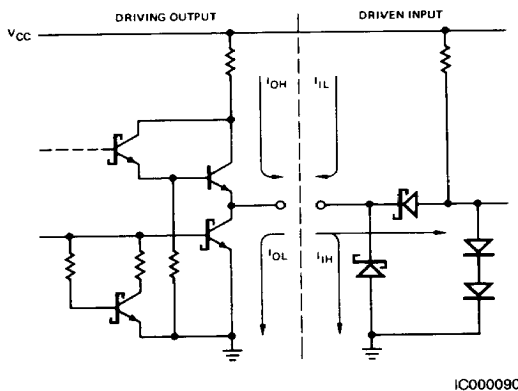
Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r , t_f , pulse width or duty cycle.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

Parameters	Description	Test Conditions	COMMERCIAL		MILITARY		Units	
			Am25LS2519		Am25LS2519			
			Min	Max	Min	Max		
tPLH	Clock to Yi	CL = 50pF RL = 2.0kΩ		39		42	ns	
tPHL				39		45		
tPLH	Clock to Wi (Either Polarity)			41		43	ns	
tPHL				44		48		
tPHL	Clear to Yi			52		58	ns	
tPLH	Clear to Wi			42		43	ns	
tPHL				51		53		
tPLH	Polarity to Wi			41		45	ns	
tPHL				42		44		
tpw	Clear			20		20	ns	
tpw	Clock		LOW		20		20	ns
			HIGH		20		20	
ts	Data			15		15	ns	
th	Data			10		10	ns	
ts	Data Enable			25		25	ns	
th	Data Enable			0		0	ns	
ts	Set-up Time, Clear Recovery (Inactive) to Clock			23		24	ns	
tZH	Output Enable to Wi or Yi				24		27	
tZL				29		35		
tHZ	Output Enable to Wi or Yi		33		45	ns		
tLZ			22		26			
fmax	Maximum Clock Frequency (Note 1)	CL = 5.0pF RL = 2.0kΩ	30		25	MHz		

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Am25LS2519
LOW-POWER SCHOTTKY INPUT/OUTPUT
CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.