

# SN54ALS74A, SN54AS74, SN74ALS74A, SN74AS74 DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

SDAS143A – D2661, APRIL 1982 – REVISED SEPTEMBER 1987

- Package Options Include Plastic Small Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY ( $C_L = 50$ pF)	TYPICAL POWER DISSIPATION PER FLIP-FLOP
'ALS74A	50 MHz	6 mW
'AS74	134 MHz	26 mW

## description

These devices contain two independent D-type positive-edge triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

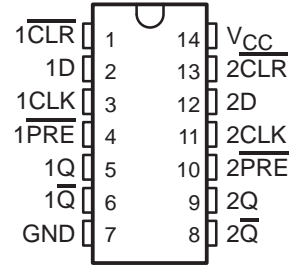
The SN54ALS74A and SN54AS74 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS74A and SN74AS74 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

FUNCTION TABLE

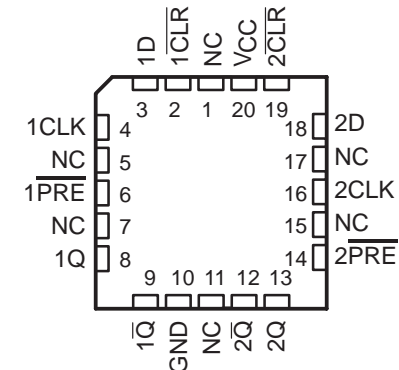
INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	$H^{\dagger}$	$H^{\dagger}$
H	H	$\uparrow$	H	H	L
H	H	$\uparrow$	L	L	H
H	H	L	X	$Q_O$	$\bar{Q}_O$

$\dagger$  The output levels in this configuration are not guaranteed to meet the minimum levels for  $V_{OH}$  if the lows at Preset and Clear are near  $V_{IL}$  maximum. Furthermore, this configuration is nonstable; that is, it will not persist when Preset or Clear; returns to their inactive (high) level.

SN54ALS74A, SN54AS74 ... J PACKAGE  
SN74ALS74A, SN74AS74 ... D OR N PACKAGE  
(TOP VIEW)

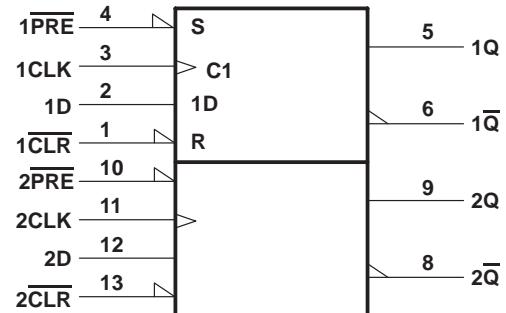


SN54ALS74A, SN54AS74 ... FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## logic symbol†



$\dagger$  This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

# SN54ALS74A, SN54AS74, SN74ALS74A, SN74AS74

## DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$	7 V
Input voltage	7 V
Operating free-air temperature range: SN54ALS74A, SN54ALS74	–55°C to 125°C
SN74ALS74A, SN74ALS74	0°C to 70°C
Storage temperature range	–65°C to 150°C

### recommended operating conditions

		SN54AS74			SN74AS74			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage						0.8	V
				0.8†				
				0.7‡				
$I_{OH}$	High-level output current			–0.4			–0.4	mA
$I_{OL}$	Low-level output current			4			8	mA
$f_{clock}$	Clock frequency	0		25	0		34	MHz
$t_w$	Pulse duration	PRE or CLR low		15	15			ns
		CLK high		16.5	14.5			
		CLK low		16.5	14.5			
$t_{su}$	Setup time before CLK↑	Data		15	15			ns
		PRE or CLR inactive		10	10			
$t_h$	Hold time, data after CLK↑	0			0			ns
$T_A$	Operating free-air temperature	–55		125	0		70	°C

† Tested at –55°C to 70°C.

‡ Tested at 70°C 125°C, per MIL-STD-883, method 5005, sub-group 1, 2, and 3. Static tests are performed at 25°C, 125°C, and –55°C.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54AS74			SN74AS74			UNIT
			MIN	TYP§	MAX	MIN	TYP§	MAX	
$V_{IK}$		$V_{CC} = 4.5$ V, $I_I = -18$ mA				–1.2		–1.5	V
$V_{OH}$		$V_{CC} = 4.5$ V to 5.5 V, $I_{OH} = -2$ mA	$V_{CC} - 2$			$V_{CC} - 2$			V
$V_{OL}$		$V_{CC} = 4.5$ V, $I_{OL} = 4$ mA		0.25	0.4		0.25	0.4	V
$V_{OL}$		$V_{CC} = 4.5$ V, $I_{OL} = 8$ mA					0.35	0.5	
$I_I$	CLK or D	$V_{CC} = 4.5$ V, $V_I = 7$ V			0.1			0.1	mA
	PRE or CLR				0.2			0.2	
$I_{IH}$	CLK or D	$V_{CC} = 4.5$ V, $V_I = 2.7$ V			20			20	µA
	PRE or CLR				40			40	
$I_{IL}$	CLK or D	$V_{CC} = 4.5$ V, $V_I = 0.4$ V			–0.2			–0.2	mA
	PRE or CLR				–0.4			–0.4	
$I_{O\uparrow}$		$V_{CC} = 5.5$ V, $V_O = 2.25$ V	–30		–112	–30		–112	mA
$I_{CC}$		$V_{CC} = 5.5$ V, See Note 1		2.4	4		2.4	4	mA

§ All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

¶ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

NOTE 1:  $I_{CC}$  is measured with D, CLK, and PRE grounded, then with D, CLK, and CLR grounded.

**SN54ALS74A, SN74ALS74A**  
**DUAL D-TYPE POSITIVE-EDGE-TRIGGERED**  
**FLIP-FLOPS WITH CLEAR AND PRESET**  
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**switching characteristics (see Note 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN TO MAX†				UNIT
			SN54ALS74A		SN74ALS74A		
			MIN	MAX	MIN	MAX	
f <sub>max</sub>			25		34		MHz
t <sub>PLH</sub>	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	3	13.5	3	13	ns
t <sub>PHL</sub>			5	17	5	15	
t <sub>PLH</sub>	CLK	Q or $\overline{\text{Q}}$	5	17	5	16	ns
t <sub>PHL</sub>			5	18	5	18	

<sup>†</sup> For conditions shown MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Load circuit and voltage waveforms are shown in Section 1 of the *ALS/AS Logic Data Book*, 1986.

# SN54AS74, SN74AS74

## DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

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### recommended operating conditions

			SN54AS74			SN74AS74			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage		2			2			V
V <sub>IL</sub>	Low-level input voltage				0.8			0.8	V
I <sub>OH</sub>	High-level output current				−2			−2	mA
I <sub>OL</sub>	Low-level output current				20			20	mA
f <sub>clock</sub>	Clock frequency		0		90	0		105	MHz
t <sub>w</sub>	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	4			4			ns
		CLK high	4			4			
		CLK low	5.5			5.5			
t <sub>su</sub>	Setup time before CLK↑	Data	4.5			4.5			ns
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	2			2			
t <sub>h</sub>	Hold time, data after CLK↑		0			0			ns
T <sub>A</sub>	Operating free-air temperature		−55		125	0		70	°C

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS74			SN74AS74			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = −18 mA				−1.2	−1.2	V	
V <sub>OH</sub>		V <sub>CC</sub> = 4.5 V to 5.5 V,	I <sub>OH</sub> = −2mA	V <sub>CC</sub> −2			V <sub>CC</sub> −2		V	
V <sub>OL</sub>		V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 20 mA	0.25		0.5	0.25		0.5	V
I <sub>I</sub>		V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 7 V	0.1			0.1		mA	
I <sub>IH</sub>	CLK or D	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V	20			20		μA	
	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$			40			40			
I <sub>IL</sub>	CLK or D	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.4 V	−0.5			−0.5		mA	
	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$			−1.8			−1.8			
I <sub>O</sub> ‡		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.25 V	−30	−112	−30	−112	mA		
I <sub>CC</sub>		V <sub>CC</sub> = 5.5 V,	See Note 1	10.5	16	10.5	16	mA		

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

NOTE 1:  $I_{CC}$  is measured with D, CLK, and  $\overline{PRE}$  grounded, then with D, CLK, and  $\overline{CLR}$  grounded.

### switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN TO MAX§				UNIT
			SN54AS74A		SN74AS74A		
			MIN	MAX	MIN	MAX	
f <sub>max</sub>			90		105		MHz
t <sub>PLH</sub>	PRE or CLR	Q or Q̄	3	8.5	3	7.5	ns
t <sub>PHL</sub>			3.5	11.5	3.5	10.5	
t <sub>PLH</sub>	CLK	Q or Q̄	3.5	9	3.5	8	ns
t <sub>PHL</sub>			4.5	10.5	4.5	9	

§ For conditions shown MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Load circuit and voltage waveforms are shown in Section 1 of the *ALS/AS Logic Data Book*, 1986.



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