



HIGH-PERFORMANCE CMOS BUFFER

IDT54/74FCT827A/B

FEATURES:

- Faster than AMD's Am29827 series
- Equivalent to AMD's Am29827 bipolar buffers in pinout/function, speed, and output drive over full temperature and voltage supply extremes
- IDT54/74FCT827A equivalent to FAST™ speed
- IDT54FCT827B 35% faster than FAST
- $I_{OL} = 48\text{mA}$ (commercial) and 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 series ($5\mu\text{A}$ max.)
- Military product compliant to MIL-STD-883, Class B
- Available in the following packages:
 - Commercial: SOIC
 - Military: CERDIP, LCC

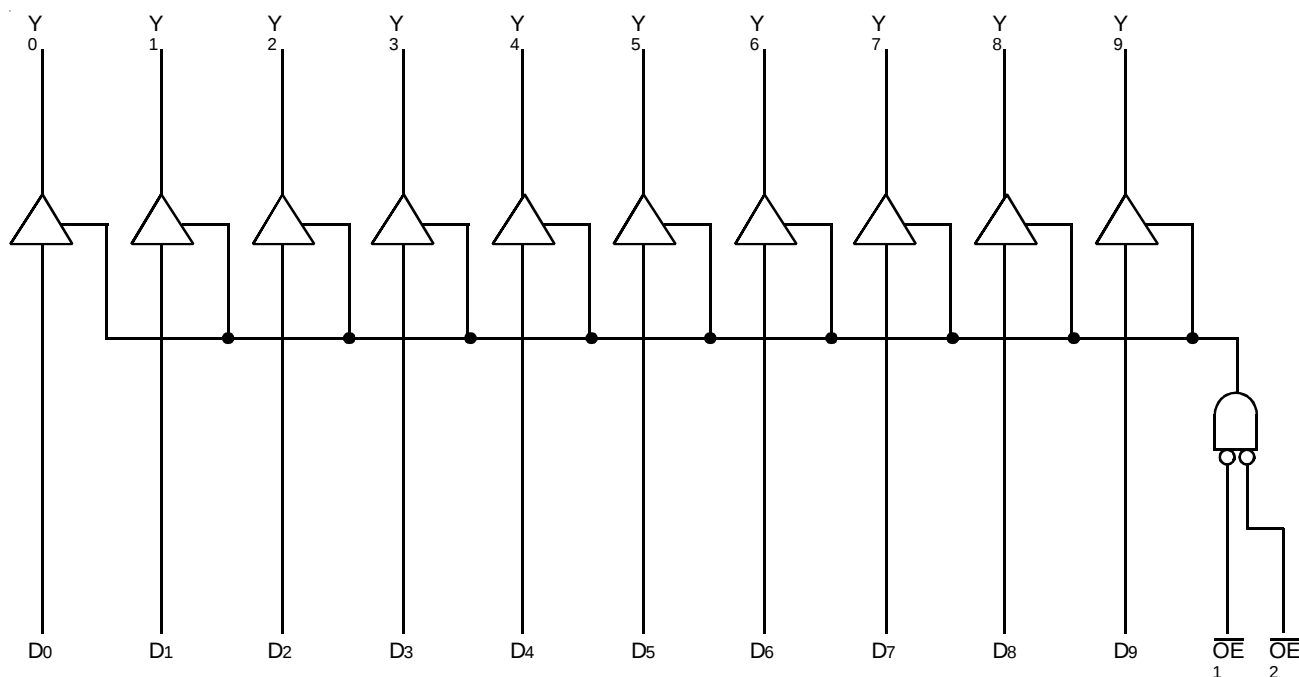
DESCRIPTION:

The IDT54/74FCT800 series is built using an advanced dual metal CMOS technology.

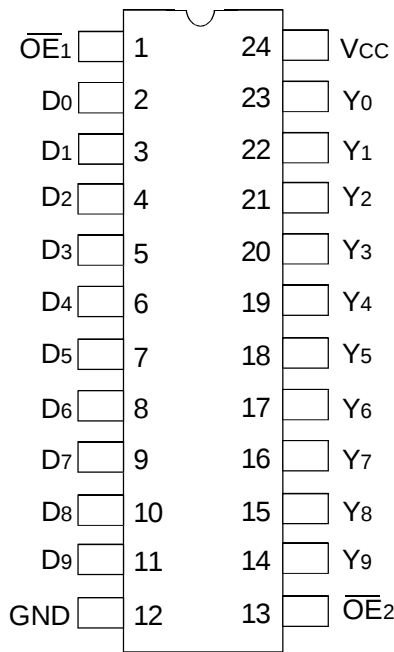
The IDT54/74FCT827 10-bit bus drivers provide high-performance bus interface buffering for wide data/address paths or buses carrying parity. The 10-bit buffers have NAND-ed output enables for maximum control flexibility.

All of the IDT54/74FCT800 high-performance interface family are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in high-impedance state.

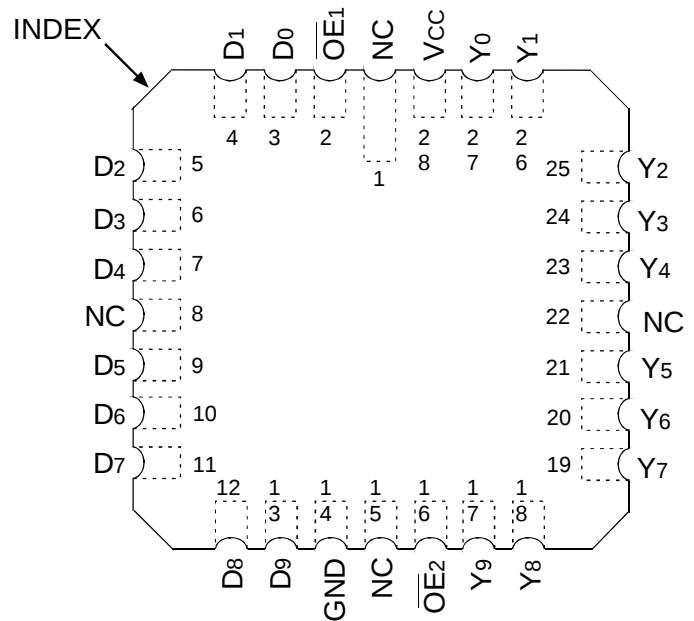
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



CERDIP/ SOIC
TOP VIEW



LCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7	-0.5 to +7	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to V _{CC}	-0.5 to V _{CC}	V
T _A	Operating Temperature	0 to +70	-55 to +125	°C
T _{BIAS}	Temperature under BIAS	-55 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P _T	Power Dissipation	0.5	0.5	W
I _{OUT}	DC Output Current	120	120	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.

2. Input and V_{CC} terminals only.

3. Output and I/O terminals only.

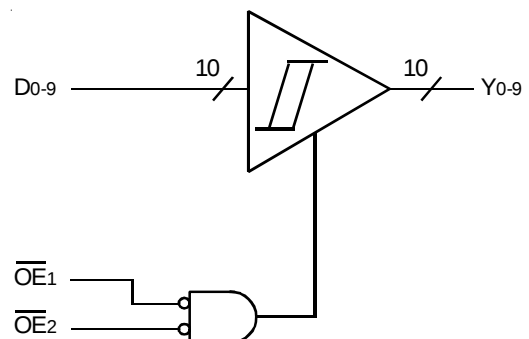
CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

LOGIC SYMBOL



PIN DESCRIPTION

Pin Name	I/O	Description
$\overline{OE}_x$	I	When both are LOW, the outputs are enabled. When either one or both are HIGH, the outputs are High Z.
Dx	I	10-bit data input
Yx	O	10-bit data output

FUNCTION TABLE⁽¹⁾

Inputs			Outputs	Function
$\overline{OE}_1$	$\overline{OE}_2$	Dx	Yx	
L	L	L	L	Transparent
L	L	H	H	
H	X	X	Z	3-State
X	H	X	Z	

NOTE:

1. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: $V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

Commercial: $T_A = 0^\circ C$ to $+70^\circ C$, $V_{CC} = 5.0V \pm 5\%$, Military: $T_A = -55^\circ C$ to $+125^\circ C$, $V_{CC} = 5.0V \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V _{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V _{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I _{IH}	Input HIGH Current	V _{CC} = Max.	V _I = V _{CC}	—	—	5	μA
I _{IL}	Input LOW Current		V _I = 2.7V	—	—	5 ⁽⁴⁾	
			V _I = 0.5V	—	—	−5 ⁽⁴⁾	
			V _I = GND	—	—	−5	
I _{OZH}	Off State (High Impedance) Output Current	V _{CC} = Max.	V _O = V _{CC}	—	—	10	μA
I _{OZL}			V _O = 2.7V	—	—	10 ⁽⁴⁾	
			V _O = 0.5V	—	—	−10 ⁽⁴⁾	
			V _O = GND	—	—	−10	
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = −18mA		—	−0.7	−1.2	V
I _{OS}	Short Circuit Current	V _{CC} = Max., V _O = GND ⁽³⁾		−75	−120	—	mA
V _{OH}	Output HIGH Voltage	V _{CC} = 3V, V _{IN} = V _{LC} or V _{HC} , I _{OH} = −32μA		V _{HC}	V _{CC}	—	V
		V _{CC} = Min V _{IN} = V _{IH} or V _{IL}	I _{OH} = −300μA	V _{HC}	V _{CC}	—	
			I _{OH} = −15mA MIL	2.4	4.3	—	
			I _{OH} = −24mA COM'L	2.4	4.3	—	
V _{OL}	Output LOW Voltage	V _{CC} = 3V, V _{IN} = V _{LC} or V _{HC} , I _{OL} = 300μA		—	GND	V _{LC}	V
		V _{CC} = Min V _{IN} = V _{IH} or V _{IL}	I _{OL} = 300μA	—	GND	V _{LC} ⁽⁴⁾	
			I _{OL} = 32mA MIL	—	0.3	0.5	
			I _{OL} = 48mA COM'L	—	0.3	0.5	

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 5.0V$, $+25^\circ C$ ambient and maximum loading.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max. V _{IN} ≥ V _{HC} ; V _{IN} ≤ V _{LC}		—	0.2	1.5	mA
ΔI _{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max. V _{IN} = 3.4V ⁽³⁾		—	0.5	2	mA
I _{CCD}	Dynamic Power Supply Current ⁽⁴⁾	V _{CC} = Max. Outputs Open $\overline{OE}_1 = \overline{OE}_2 = GND$ LE = V _{CC} One Input Toggling 50% Duty Cycle	V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC}	—	0.15	0.25	mA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max. Outputs Open f _i = 10MHz 50% Duty Cycle $\overline{OE}_1 = \overline{OE}_2 = GND$ LE = V _{CC} One Bit Toggling	V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC} (FCT)	—	1.7	4	mA
			V _{IN} = 3.4V V _{IN} = GND	—	2	5	
		V _{CC} = Max. Outputs Open f _i = 2.5MHz 50% Duty Cycle $\overline{OE}_1 = \overline{OE}_2 = GND$ LE = V _{CC} Eight Bits Toggling	V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC} (FCT)	—	3.2	6.5 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND	—	5.2	14.5 ⁽⁵⁾	

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical values are at V_{CC} = 5.0V, +25°C ambient.

3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.

4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.

5. Values for these conditions are examples of ΔI_{CC} formula. These limits are guaranteed but not tested.

6. I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

I_C = I_{CC} + ΔI_{CC} D_HN_T + I_{CCD} (f_{CP}/2 + f_iN_i)

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{CCD} = Dynamic Current caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for register devices (zero for non-register devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

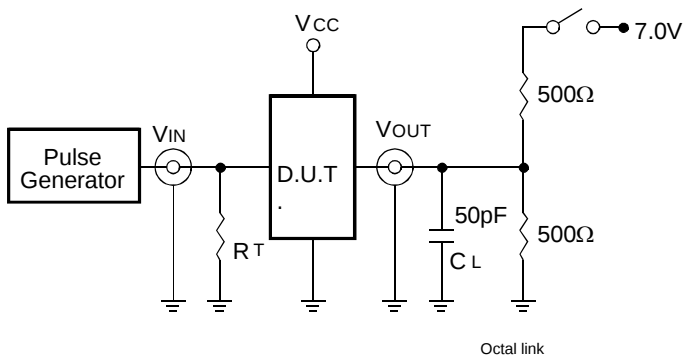
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	54/74FCT827A				54FCT827B		Unit
			Com'l.		Mil.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay Dx to Yx	CL = 50pF RL = 500Ω	1.5	8	1.5	9	1.5	6.5	ns
		CL = 300pF ⁽³⁾ RL = 500Ω	1.5	15	1.5	17	1.5	14	
t _{PZH} t _{PZL}	Output Enable Time, OE to Yx	CL = 50pF RL = 500Ω	1.5	12	1.5	13	1.5	9	ns
		CL = 300pF ⁽³⁾ RL = 500Ω	1.5	23	1.5	25	1.5	16	
t _{PHZ} t _{PLZ}	Output Disable Time, OE to Yx	CL = 5pF ⁽³⁾ RL = 500Ω	1.5	9	1.5	9	1.5	7	ns
		CL = 50pF RL = 500Ω	1.5	10	1.5	10	1.5	8	

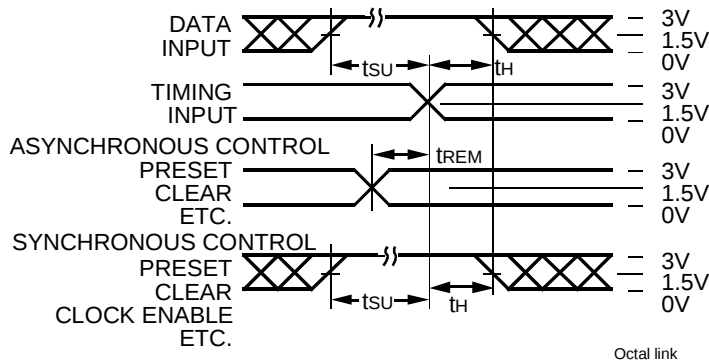
NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested.

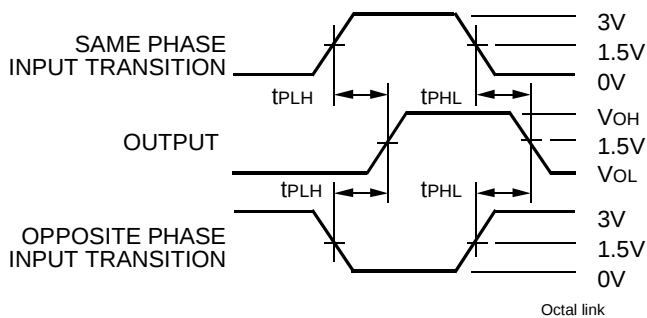
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-Up, Hold, and Release Times



Propagation Delay

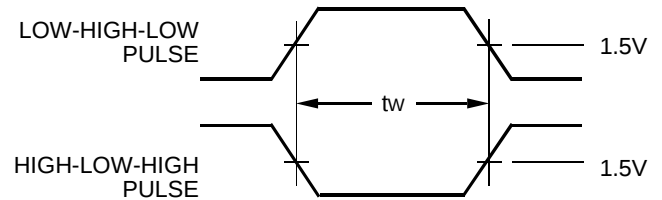
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

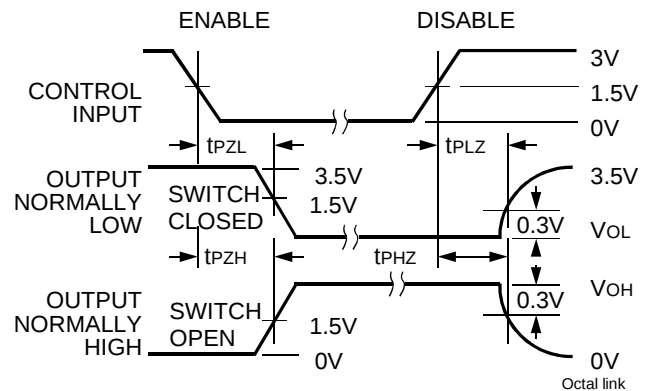
DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width



Enable and Disable Times

NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $Z_o \leq 50\Omega$; $t_r \leq 2.5\text{ns}$; $t_f \leq 2.5\text{ns}$.

ORDERING INFORMATION

IDT	XX	FCT	XXXX	XX	X		
Temp. Range	Device Type		Package	Process			
					Blank	Commercial	
					B	MIL-STD-883, Class B	
					SO	<u>Commercial Options</u> Small Outline IC	
					D L	<u>Military Options</u> CERDIP Leadless Chip Carrier	
					827A 827B	High Performance CMOS Buffer, 10-Bit	
					54 74	– 55°C to +125°C 0°C to +70°C	



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