



Synchronous Buck Converter Controller

FEATURES

- 6- to 16.5-V Input Range (Si9150CY)
- Voltage-Mode PWM Control
- Low-Current Standby Mode
- Enable Control
- Dual 100-mA Output Drivers
- 2% Band Gap Reference
- Multiple Converters Easily Synchronized
- Over-Current Protection

DESCRIPTION

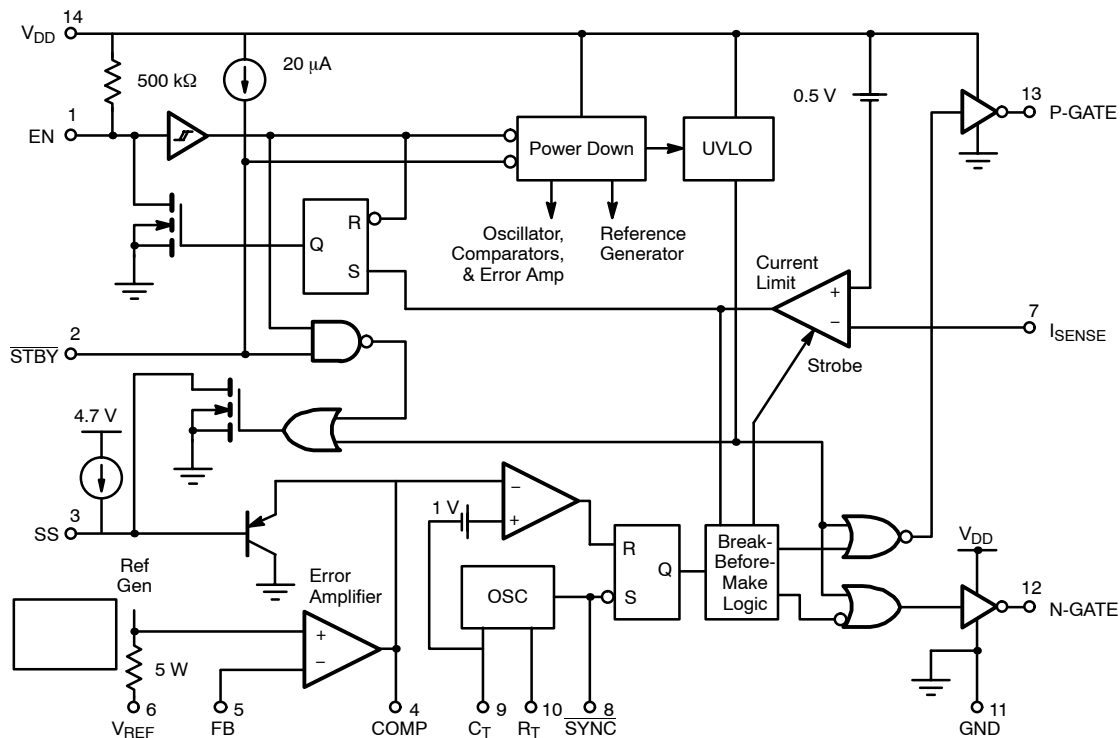
The Si9150 synchronous buck regulator controller is ideally suited for high-efficiency step down converters in battery-powered equipment. Combined with the Si9943DY MOSFET half-bridge, a 90% efficient, 7.5-W, 3.3-V or 5-V power supply can be implemented using standard surface-mount assembly techniques. The wide input range allows operation from NiCd or NiMH battery packs using six to ten cells.

Over-current protection is achieved by sensing the on-state voltage drop across the high side p-channel MOSFET, which eliminates the need for a current sense resistor.

Duty ratios of 0 to 100% and switching frequencies up to 300 kHz are possible. The IC can be disabled by pulling EN low ($I_{DD} = 100 \mu\text{A}$), or the 2.5-V reference can be maintained, with all other functions disabled, by pulling $\overline{\text{STBY}}$ low ($I_{DD} = 500 \mu\text{A}$).

The Si9150 is available in both standard and lead (Pb)-free 14-pin SOIC and rated for the commercial temperature range of 0 to 70°C (C suffix), and the industrial temperature range of -40 to +85°C (D suffix).

FUNCTIONAL BLOCK DIAGRAM



Synchronous Buck Regulator Controller

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to GND.

V_{DD}	18 V
ISENSE Input	-2 V to $V_{DD} + 2$ V
All Other Inputs	-0.3 to $V_{DD} + 0.3$ V
P-Gate, N-Gate Continuous Source/Sink Current	50 mA
Storage Temperature	-65 to 125°C
Operating Junction Temperature	150°C

Power Dissipation (Package)^a

14-Pin SOIC (Y Suffix)^b 900 mW

Thermal Impedance (θ_{JA})

14-Pin SOIC 140°C/W

Notes

a. Device mounted with all leads soldered or welded to PC board.

b. Derate 7.2 mW/°C.

SPECIFICATIONS^a

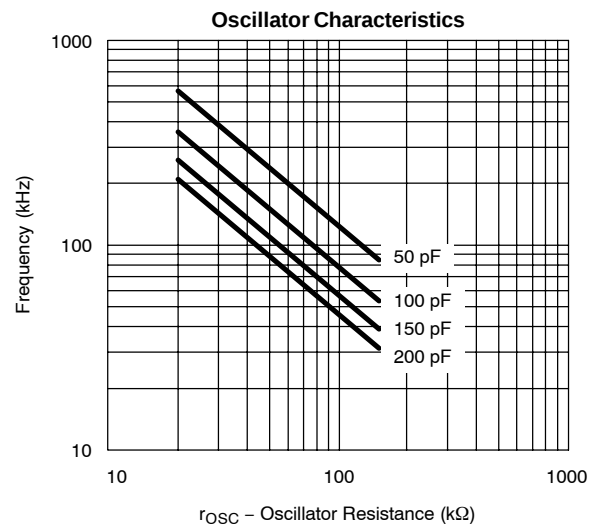
Parameter	Symbol	Test Conditions Unless Otherwise Specified 6.0 ≤ V _{DD} ≤ 16.5 V	Limits C Suffix 0 to 70°C			Limits D Suffix −40 to 85°C			Unit
			Min ^b	Typ ^c	Max ^b	Min ^b	Typ ^c	Max ^b	
Reference									
Output Voltage	V _{REF}	T _A = 25°C Measured at Feedback ^e Pin 5	2.45	2.50	2.55	2.45	2.50	2.55	V
		T _{MIN} to T _{MAX} ^d	2.425	2.500	2.575	2.40	2.500	2.60	
Oscillator									
Maximum Frequency	f _{MAX}	C _{OSC} =94.3 pF, R _{OSC} = 28.7 kΩ T _A = 25°C ^f	255	300	345	255	300	345	kHz
Initial Accuracy	f _{OSC}	C _{OSC} =212 pF, R _{OSC} = 41.2 kΩ T _A = 25°C ^f	85	100	115	85	100	115	
Oscillator Ramp Amplitude	V _{OSC}	T _A = 25°C, 100 kHz	2.05	2.65	2.85	2.05	2.65	2.85	V
Temperature Stability ^d	f _{TEMP}	V _{DD} = 10 V, T _{MIN} to T _{MAX}	−5	±3	+5	−6	± 4	+6	%
Error Amplifier									
Input BIAS Current	I _B	V _{FB} = V _{REF}		25	500		25	750	nA
Open Loop Voltage Gain ^d	A _{VOL}		60	72		58	72		dB
Offset Voltage	V _{OS}			10	25		10	30	mV
Unity Gain Bandwidth ^d	BW		1	1.5		1	1.5		MHz
Output Current	I _{OUT}	Source, V _{COMP} = 2.50 V		−0.30	−0.20		−0.30	−0.15	mA
		Sink, V _{COMP} = 1.0 V	1	2.5		0.9	2.5		
Power Supply Rejection	PSRR		50	70		48	70		dB
Protection									
Current Limit Threshold Voltage	V _{CL}	T _A = 25°C, V _{DD} = 10 V	0.43	0.49	0.55	0.43	0.49	0.55	V
Current Limit Delay to Output ^d	t _d	T _A = 25°C		500	1000		500	1000	ns
Undervoltage Lockout Voltage	V _{UVLO}	Upper Threshold	5.4	5.7	6.0	5.38	5.7	6.01	V
Undervoltage Hysteresis	V _{HYS}		0.10	0.17	0.25	0.10	0.17	0.26	
Softstart Pull-Up Current	I _{SS}			20			20		μA
Supply									
Supply Current (Enable Low)	I _{OFF}			60	100		60	100	μA
Supply Current (Enable High)	I _{CC}	C _L = 0 pF, f _{OSC} = 100 kHz V _{DD} = 10 V		2.2	3.0		2.2	3.0	mA
Supply Current (STBY Low)	I _{SB}			300	500		300	550	μA

**SPECIFICATIONS^a**

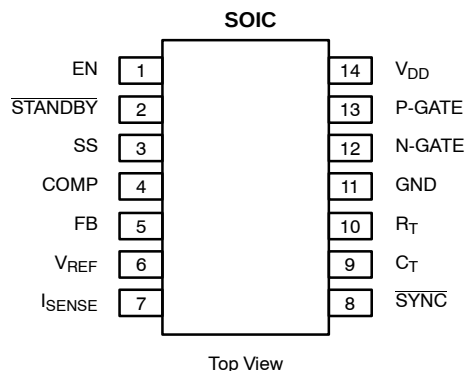
Parameter	Symbol	Test Conditions Unless Otherwise Specified 6.0 ≤ V _{DD} ≤ 16.5 V	Limits C Suffix 0 to 70°C			Limits D Suffix −40 to 85°C			Unit
			Min ^b	Typ ^c	Max ^b	Min ^b	Typ ^c	Max ^b	
Output									
Output High Voltage	V _{OH}	I _{OUT} = 10 mA, V _{DD} = 10 V	9.75			9.7			V
Output Low Voltage	V _{OL}	I _{OUT} = −10 mA, V _{DD} = 10 V			0.25			0.3	
Output Resistance	R _{OUT}	I _{OUT} = 100 mA, V _{DD} = 10 V		10	20		10	25	Ω
Rise Time ^d	t _r	C _L = 800 pF, V _{DD} = 10 V		30	60		30	70	ns
Fall Time ^d	t _f			30	60		30	70	
Logic									
Delay to Output	t _{d(EN)}	Transition High to Low		0.25	1		0.25	1	μs
Enable Pull-Up Resistance	R _{EN}			500			500		kΩ
STBY Pull-Up Current	I _{STBY}	T _A = 25°C, V _{STBY} = 0 V V _{DD} = 10 V	−25	−20	−15	−28	−20	−12	μA
Turn-On Threshold	V _{ENH}	V _{DD} = 10 V, Rising Input Voltage	6	6.8	8	6	6.8	8	V
Turn-Off Threshold	V _{ENL}	V _{DD} = 10 V, Falling Input Voltage	2	3.75	5	2	3.75	5	

Notes

- Refer to PROCESS OPTION FLOWCHART for additional information.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- Guaranteed by design, not subject to production test.
- The voltage reference is trimmed with the feedback (Pin 5) connected to compensation (Pin 4) so that the effect of the error amplifier's input offset voltage is eliminated.
- C_{OSC} includes the PC board's parasitic capacitance.

TYPICAL CHARACTERISTICS (25°C UNLESS OTHERWISE NOTED)

PIN CONFIGURATION AND ORDERING INFORMATION



ORDERING INFORMATION

ORDERING INFORMATION		
Part Number	Temperature Range	Package
Si9150CY	0 to 70°C	SOIC-14
Si9150CY-T1		
Si9150CY-T1—E3		
Si9150DY	–40 to 85°C	
Si9150DY-T1		
Si9150DY-T1—E3		

PIN DESCRIPTION

Pin 1: EN

When this pin is low, the IC is shut down. After a low signal is applied to EN, then COMP, REF, R_T , and C_T settle toward ground; N-GATE, $\overline{STBY}$ and Soft-Start are grounded; and P-GATE is pulled high. The current consumption is no more than 100 μ A in this state. This input's threshold has substantial hysteresis so that a capacitor to GND can be used to delay restart after the current limit is activated. After V_{ENH} is exceeded, one clock cycle elapses before N-GATE and P-GATE are enabled. EN is pulled up to V_{DD} through a 500-k resistor and is pulled down internally when the current limit is triggered.

Pin 2: $\overline{STBY}$

Has a function similar to EN. The differences are that the EN pin is unaffected, that the reference is still available, that bias currents are still present internally, and that this pin's pull up current is present. This pin should be used to disable an application if the reference voltage is still needed.

Pin 3: Soft-Start (SS)

This pin limits the maximum voltage that the error amplifier can output. A capacitor between this pin and ground will limit the rate at which the duty factor can increase during initial power up, during a restart when EN or $\overline{STBY}$ goes high, or after the current limit is triggered. A capacitor here can prevent an application from triggering the Si9150's current limit during startup. Soft-Start is pulled low if either EN or $\overline{STBY}$ is low.

Pin 4: Compensation (COMP)

This pin is tied directly to the output of the error amplifier. The feedback network which insures the stability of an application

uses this pin. COMP settles low when either EN or $\overline{STBY}$ is pulled low.

Pin 5: Feedback (FB)

This pin is attached directly to the inverting input of the error amplifier. This pin is used to regulate the power supply's output voltage.

Pin 6: Reference (V_{REF})

The internal 2.5-V reference generator is attached to this pin through a 5- Ω resistor. A 0.1- μ F bypass capacitor is needed to suppress noise. Also note that the generator has an open emitter; it will not pull down. The maximum current that the generator will source before it current limits is about 10 mA. Many parts of the IC use this voltage, so it is important not to overload the reference generator.

Pin 7: I_{SENSE}

This pin should be attached to the switched node (the drains of the application's p-channel and n-channel MOSFETs). If the voltage between V_{DD} and this pin is more than 0.46 V while the P-GATE is low, the current limit is activated. The current limit is relatively slow to prevent false triggering due to noise. Activating the current limit causes EN to be pulled to GND. I_{SENSE} may be operated from $V_{DD} + 2$ V to GND – 2 V. For operation above 13.5 V_{DD} a filter (1 k Ω , 33 pF) is needed between the MOSFET drains and the I_{SENSE} pin; refer to Figure 1.

Pin 8: $\overline{SYNC}$

This pin forces the clock to reset when low, and is also pulled low when the clock resets itself. Thus if several Si9150's have their sync pins shorted together, they will be synchronized; the shortest duration clock will control the other clocks.

Pin 9: C_T

A capacitor from this pin to ground is charged until it reaches 2.5 V, at which point the capacitor is rapidly discharged. The resulting sawtooth with about 1 V added is compared to the input voltage at COMP to determine whether P-GATE and N-GATE should be high or low. The maximum recommended value for C_{OSC} is 200 pF (See Typical Characteristics). The capacitor's charging current is controlled by Pin 10, R_T.

Pin 10: R_T

The IC applies 2.5 V to this pin, and the current is mirrored and applied to Pin 9 while charging the capacitor. The minimum recommended value of R_{OSC} is 20 k Ω (Figure 1).

Pin 11: GND

Since the Si9150 has a high-side current limit, it is important that V_{DD} track the voltage on the source of the p-channel power MOSFET. For noise immunity, it is best to separate the logic ground from the power ground. The logic ground should be decoupled to V_{DD} through at least a 1- μ F capacitor. The two grounds may be connected by a path that is long compared to

the the path from V_{DD} to the source of the application's p-channel MOSFET.

Pin 12: N-GATE

This pin is used to drive the application's n-channel MOSFET. When turning the n-channel MOSFET off, the p-channel MOSFET will not be turned on until N-GATE is within a few volts of ground. This pin is low while either EN or STBY is low.

Pin 13: P-GATE

This pin is used to drive the application's p-channel MOSFET. The break before make circuitry for the P-GATE is complimentary to that for the N-GATE. This pin is high while either EN or $\overline{\text{STBY}}$ is low.

Pin 14: V_{DD}

This pin powers the IC. The connection between this pin and the source of the p-channel FET should be as short as practical. Read Pin 11's description for bypassing suggestions.

APPLICATIONS

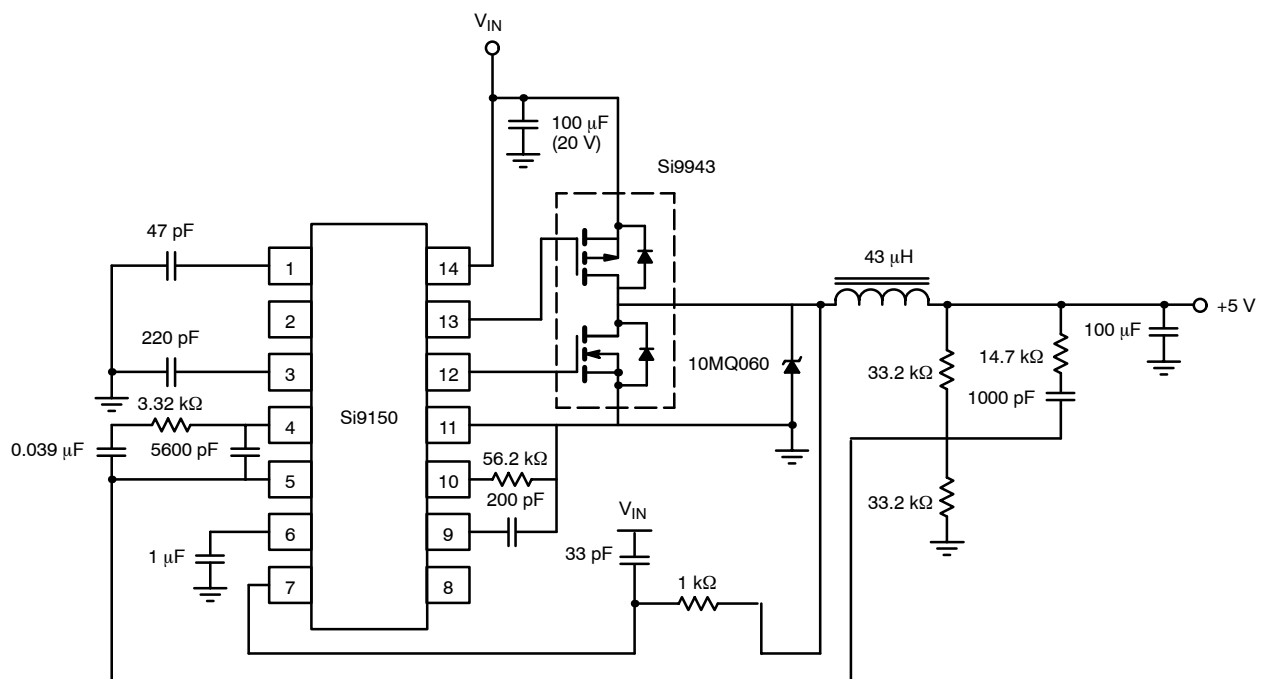


FIGURE 1. Typical Application Circuit



Notice

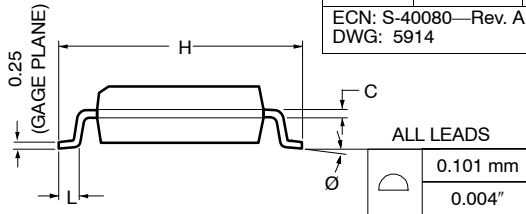
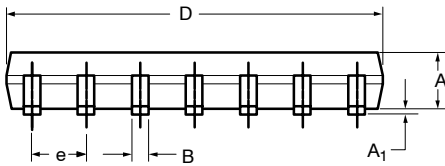
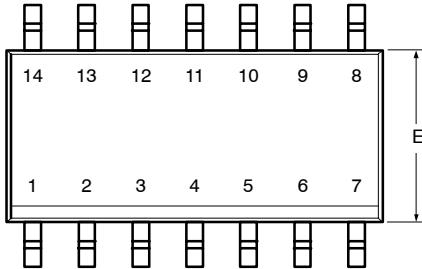
Specifications of the products displayed herein are subject to change without notice. Vishay Intertechnology, Inc., or anyone on its behalf, assumes no responsibility or liability for any errors or inaccuracies.

Information contained herein is intended to provide a product description only. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Vishay's terms and conditions of sale for such products, Vishay assumes no liability whatsoever, and disclaims any express or implied warranty, relating to sale and/or use of Vishay products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright, or other intellectual property right.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications. Customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Vishay for any damages resulting from such improper use or sale.



SOIC (NARROW): 14-LEAD (POWER IC ONLY)



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.38	0.51	0.015	0.020
C	0.18	0.23	0.007	0.009
D	8.55	8.75	0.336	0.344
E	3.8	4.00	0.149	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.50	0.93	0.020	0.037
Ø	0°	8°	0°	8°

ECN: S-40080—Rev. A, 02-Feb-04
DWG: 5914



Disclaimer

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay's knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer's responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and/or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer's technical experts. Product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein.

Except as expressly indicated in writing, Vishay products are not designed for use in medical, life-saving, or life-sustaining applications or for any other application in which the failure of the Vishay product could result in personal injury or death. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.

Material Category Policy

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as RoHS-Compliant fulfill the definitions and restrictions defined under Directive 2011/65/EU of The European Parliament and of the Council of June 8, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (EEE) - recast, unless otherwise specified as non-compliant.

Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.