FEATURES

- Four (4) Completely Independent T1 or E1 Transceivers In One Small 27mm x 27mm Package
- Each Transceiver Contains a Short & Long Haul Line Interface Plus a Full Featured Framer with Alarm Detection/Generation, Elastic Stores, Hardware Based Signaling Support, Per DS0 Channel Control and HDLC Controller
- Each Multi-Chip Module (MCM) Contains Four Die of:
  - DS21352 (DS21Q352)
  - DS21552 (DS21Q552)
  - DS21354 (DS21Q354)
  - DS21554 (DS21Q554)
- Selection Guide:

	Supply	Device
T1	3.3V	DS21Q352
T1	5V	DS21Q552
E1	3.3V	DS21Q354
E1	5V	DS21Q554

- See the Specific DS21352/DS21552 and DS21354/DS21554 Data Sheets for Details on their Feature Set and Operation
- All Four T1 or E1 Transceivers Can be Concatenated into a Single 8.192MHz Backplane Data Stream
- IEEE 1149.1 JTAG-Boundary Scan Architecture
- DS21Q352/DS21Q552 and DS21Q354/DS21Q554 are Pin Compatible to Allow the Same Footprint to Support T1 and E1 Applications
- 256–lead MCM BGA package (27mm X 27mm)
- Low Power 5V CMOS or Low Power 3.3V CMOS with 5V Tolerant Input & Outputs

DESCRIPTION

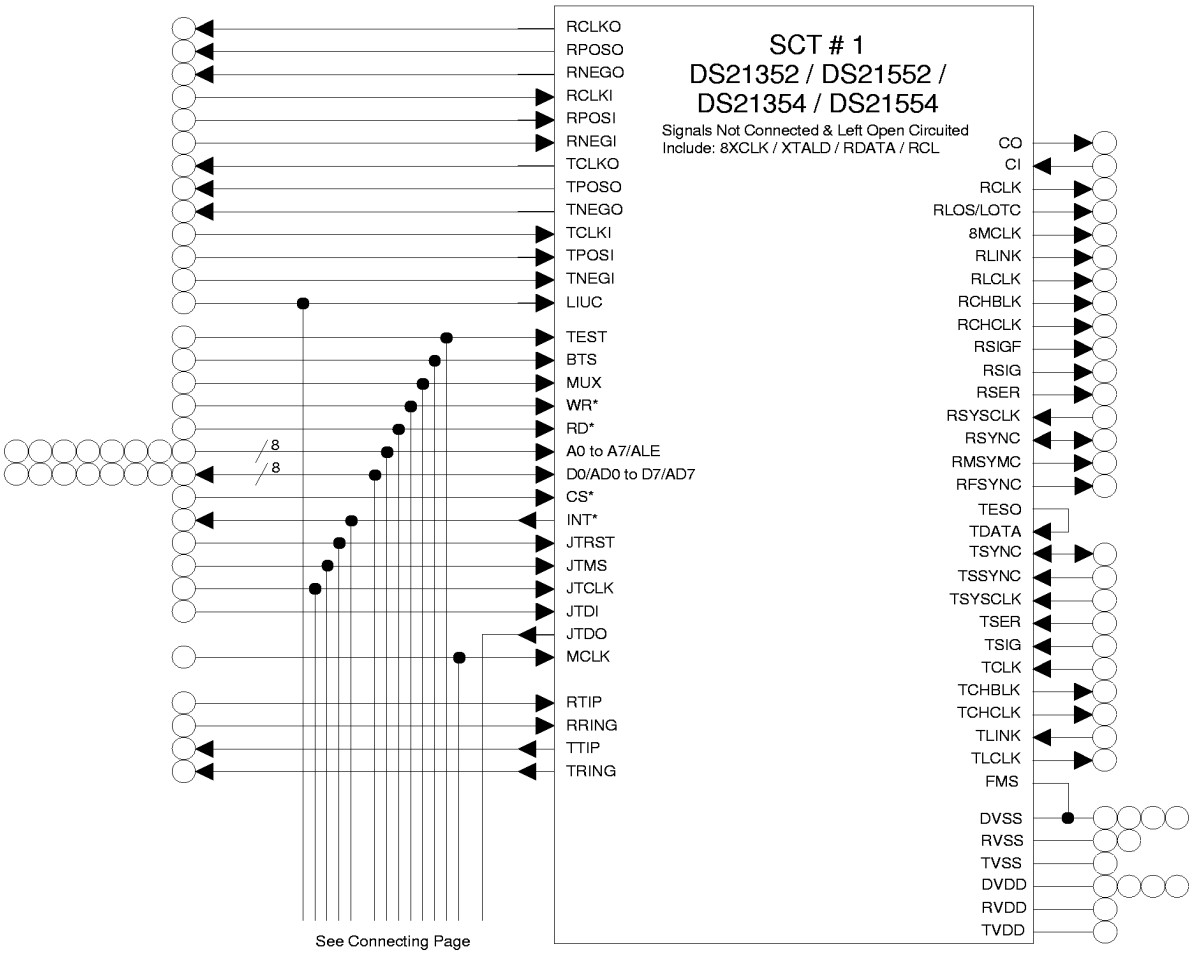
The Quad T1 and E1 Transceiver MCMs offer a high density packaging arrangement for the DS21352/DS21552 T1 Single-Chip Transceivers and the DS21354/DS21554 E1 Single-Chip Transceivers. Four silicon die of one of these devices is packaged in a Multi-Chip Module (MCM) with the electrical connections as shown in Figure 1. All of the functions available on the DS21352/DS21552 and DS21354/DS21554 are also available in the MCM packaged version however in order to minimize package size, some signals have been deleted. These differences are detailed in Table 1.

This data sheet describes the electrical connections and the mechanical dimensions only. Please see the DS21352/DS21552 and DS21354/DS21554 data sheets for full details on all of the features and the operating characteristics of the device.

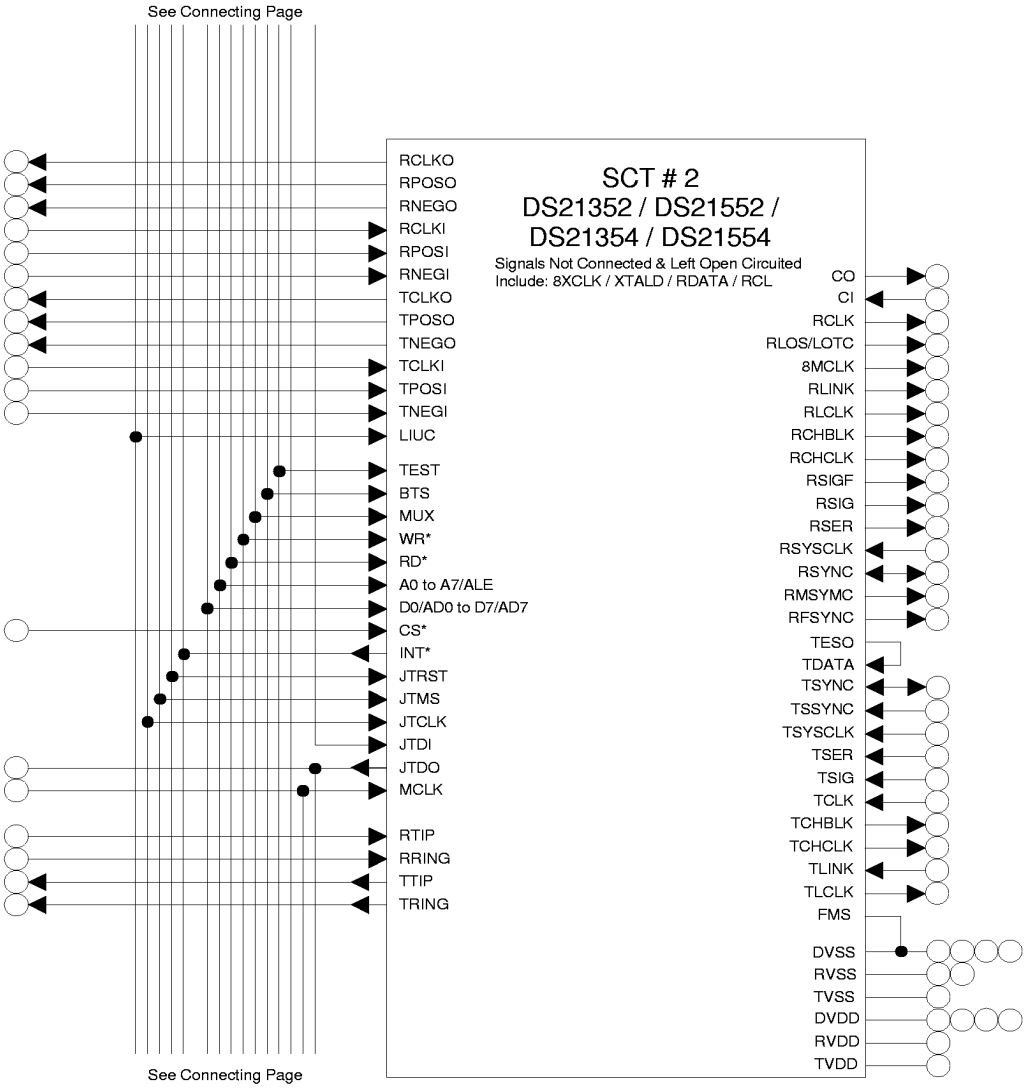
Changes from Normal DS21Q352/DS21Q552 & DS21Q354/DS21Q554 Configuration Table 1

1. The following signals are not available: XTALD / 8XCLK / TESO / TDATA / RCL / RDATA

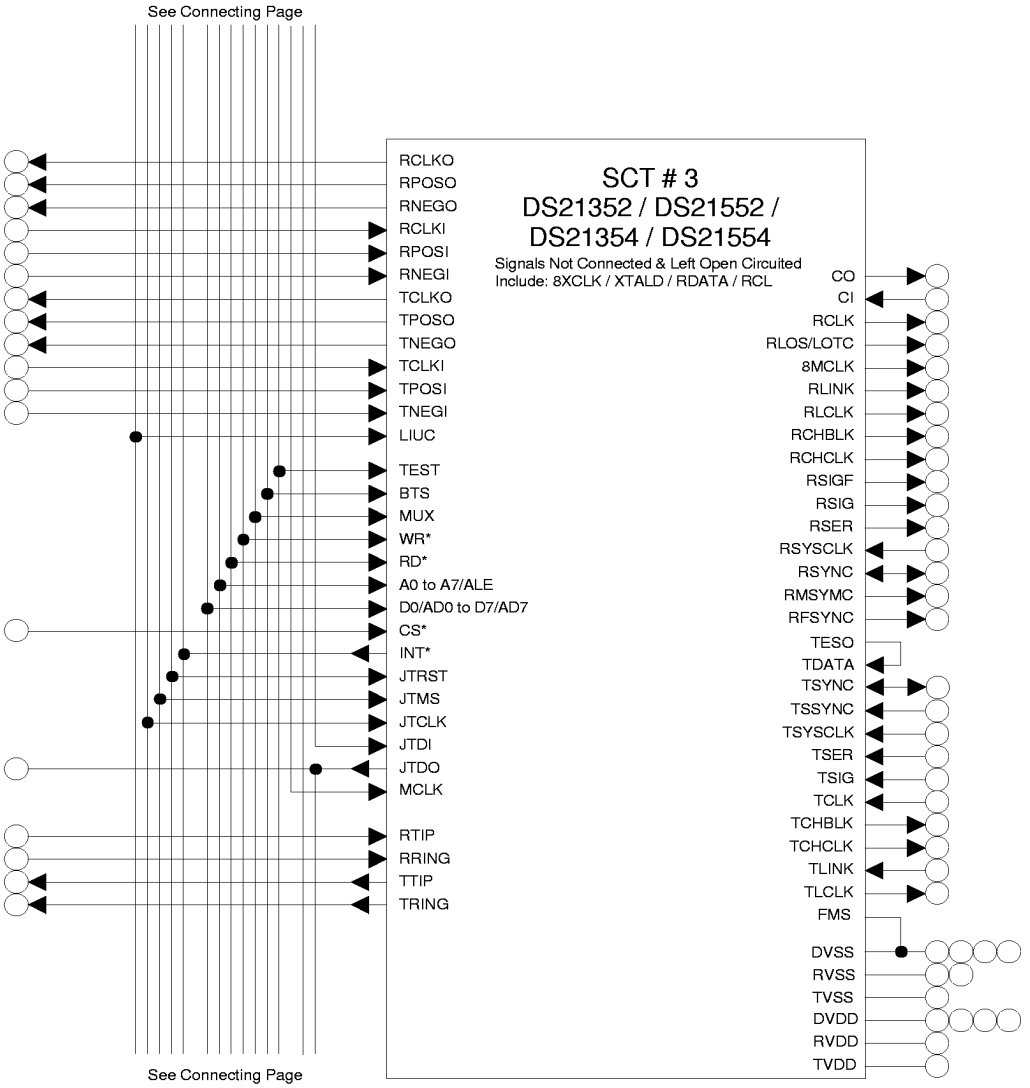
DS21Q352 / DS21Q552 / DS21Q354 / DS21Q554 Schematic Figure 1



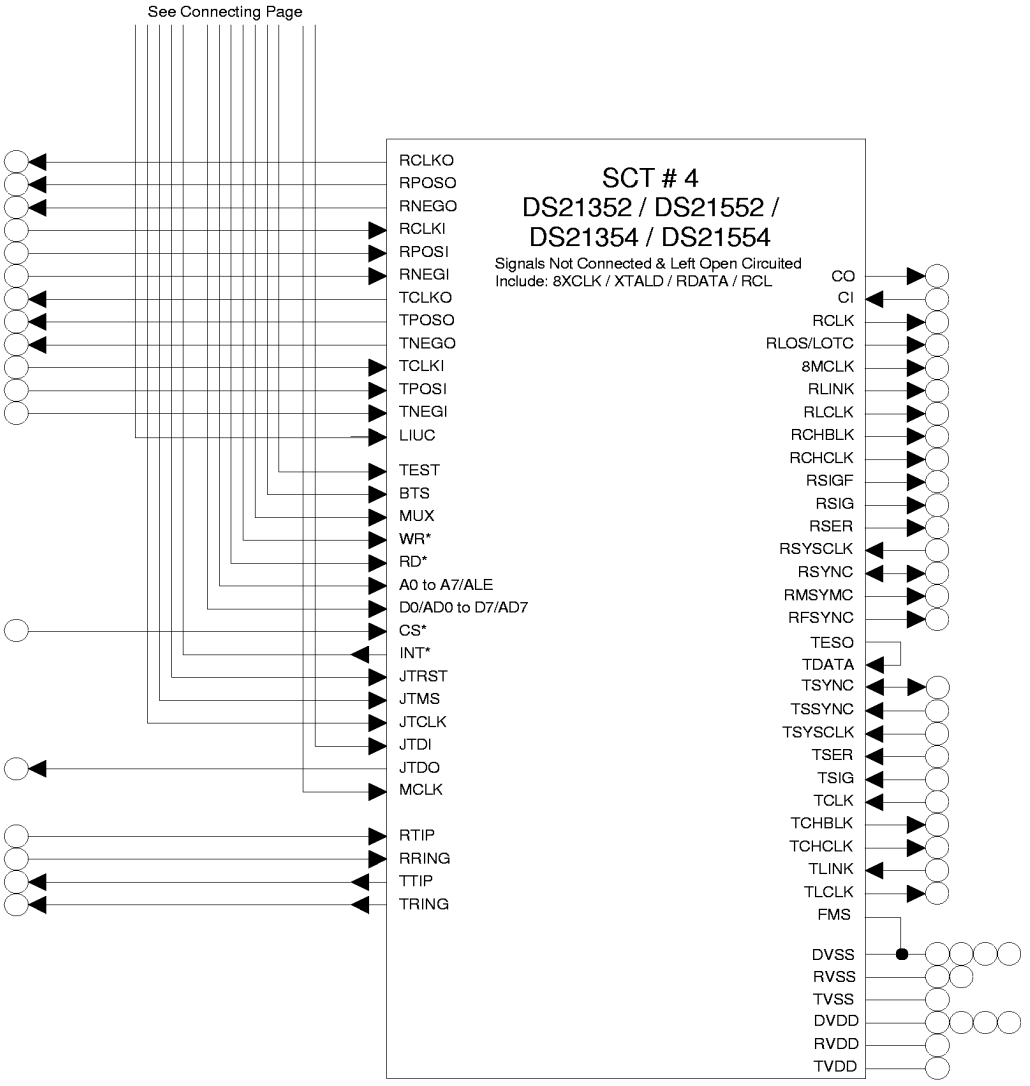
DS21Q352 / DS21Q552 / DS21Q354 / DS21Q554 Schematic Figure 1 (continued)



DS21Q352 / DS21Q552 / DS21Q354 / DS21Q554 Schematic Figure 1 (continued)



DS21Q352 / DS21Q552 / DS21Q354 / DS21Q554 Schematic Figure 1 (continued)



Lead Description Sorted by Symbol (leads are not finalized) Table 2

Lead	Symbol	I/O	Description
	8MCLK1	O	8.192 MHz Clock Based on RCLK1.
	8MCLK2	O	8.192 MHz Clock Based on RCLK2.
	8MCLK3	O	8.192 MHz Clock Based on RCLK3.
	8MCLK4	O	8.192 MHz Clock Based on RCLK4.
	A0	I	Address Bus Bit 0 (lsb).
	A1	I	Address Bus Bit 1.
	A2	I	Address Bus Bit 2.
	A3	I	Address Bus Bit 3.
	A4	I	Address Bus Bit 4.
	A5	I	Address Bus Bit 5.
	A6	I	Address Bus Bit 6.
	A7/ALE	I	Address Bus Bit 7 (msb) / Address Latch Enable.
	BTS	I	Bus Type Select (0 = Intel / 1 = Motorola),
	CI1	I	Carry Input for Interleaved Bus Operation for SCT1.
	CI2	I	Carry Input for Interleaved Bus Operation for SCT2.
	CI3	I	Carry Input for Interleaved Bus Operation for SCT3.
	CI4	I	Carry Input for Interleaved Bus Operation for SCT4.
	CO1	O	Carry Output for Interleaved Bus Operation for SCT1.
	CO2	O	Carry Output for Interleaved Bus Operation for SCT2.
	CO3	O	Carry Output for Interleaved Bus Operation for SCT3.
	CO4	O	Carry Output for Interleaved Bus Operation for SCT4.
	CS1*	I	Chip Select for SCT1.
	CS2*	I	Chip Select for SCT2.
	CS3*	I	Chip Select for SCT3.
	CS4*	I	Chip Select for SCT4.
	D0/AD0	I/O	Data Bus Bit 0/ Address/Data Bus Bit 0 (lsb).
	D1/AD1	I/O	Data Bus Bit 1/ Address/Data Bus Bit 1.
	D2/AD2	I/O	Data Bus Bit 2/Address/Data Bus Bit 2.
	D3/AD3	I/O	Data Bus Bit 3/Address/Data Bus Bit 3.
	D4/AD4	I/O	Data Bus Bit 4/Address/Data Bus Bit 4.
	D5/AD5	I/O	Data Bus Bit 5/Address/Data Bus Bit 5.
	D6/AD6	I/O	Data Bus Bit 6/Address/Data Bus Bit 6.
	D7/AD7	I/O	Data Bus Bit 7/Address/Data Bus Bit 7 (msb).
	DVDD	–	Digital Positive Supply.
	DVDD	–	Digital Positive Supply.
	DVDD	–	Digital Positive Supply.
	DVDD	–	Digital Positive Supply.
	DVDD	–	Digital Positive Supply.
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	DVDD	–	Digital Positive Supply.
	DVDD	–	Digital Positive Supply.
	DVDD	–	Digital Positive Supply.
	DVDD	–	Digital Positive Supply.
	DVDD	–	Digital Positive Supply.
	DVSS	–	Digital Signal Ground.
	DVSS	–	Digital Signal Ground.
	DVSS	–	Digital SIgnal Ground.
	DVSS	–	Digital Signal Ground.

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	DVSS	–	Digital Signal Ground
	INT*	O	Interrupt for all four SCTs.
	JTCLK	I	JTAG Clock.
	JTDI	I	JTAG Data Input.
	JTDO2	O	JTAG Data Output from SCT2.
	JTDO3	O	JTAG Data Output from SCT3.
	JTDO4	O	JTAG Data Output from SCT4.
	JTMS	I	JTAG Test Mode Select.
	JTRST*	I	JTAG Reset.
	LIUC	I	Line Interface Connect for all Four SCTs.
	MCLK1	I	Master Clock for SCT1 and SCT3.
	MCLK2	I	Master Clock for SCT2 and SCT4.
	MUX	I	Mux Bus Select.
	RCHBLK1	O	Receive Channel Block for SCT1.
	RCHBLK2	O	Receive Channel Block for SCT2.
	RCHBLK3	O	Receive Channel Block for SCT3.
	RCHBLK4	O	Receive Channel Block for SCT4.
	RCHCLK1	O	Receive Channel Clock for SCT1.
	RCHCLK2	O	Receive Channel Clock for SCT2.
	RCHCLK3	O	Receive Channel Clock for SCT3.
	RCHCLK4	O	Receive Channel Clock for SCT4.
	RCL1	O	Receive Carrier Loss for SCT1.
	RCL2	O	Receive Carrier Loss for SCT2.
	RCL3	O	Receive Carrier Loss for SCT3.
	RCL4	O	Receive Carrier Loss for SCT4.
	RCLKI1	I	Receive Clock Input for the LIU on SCT1.
	RCLKI2	I	Receive Clock Input for the LIU on SCT2.
	RCLKI3	I	Receive Clock Input for the LIU on SCT3.
	RCLKI4	I	Receive Clock Input for the LIU on SCT4.
	RCLKO1	O	Receive Clock Output from the LIU on SCT1.
	RCLKO2	O	Receive Clock Output from the LIU on SCT2.
	RCLKO3	O	Receive Clock Output from the LIU on SCT3.
	RCLKO4	O	Receive Clock Output from the LIU on SCT4.
	RD*(DS*)	I	Read Input (Data Strobe)
	RFSYNC1	O	Receive Frame Sync (before the receive elastic store) for SCT1.
	RFSYNC2	O	Receive Frame Sync (before the receive elastic store) for SCT2.
	RFSYNC3	O	Receive Frame Sync (before the receive elastic store) for SCT3.
	RFSYNC4	O	Receive Frame Sync (before the receive elastic store) for SCT4.
	RLCLK1	O	Receive Link Clock for SCT1.
	RLCLK2	O	Receive Link Clock for SCT2.
	RLCLK3	O	Receive Link Clock for SCT3.
	RLCLK4	O	Receive Link Clock for SCT4.
	RLINK1	O	Receive Link Data for SCT1.
	RLINK2	O	Receive Link Data for SCT2.
	RLINK3	O	Receive Link Data for SCT3.
	RLINK4	O	Receive Link Data for SCT4.

	RLOS/LOTC1	O	Receive Loss Of Sync / Loss Of Transmit Clock for SCT1.
	RLOS/LOTC2	O	Receive Loss Of Sync / Loss Of Transmit Clock for SCT2.
	RLOS/LOTC3	O	Receive Loss Of Sync / Loss Of Transmit Clock for SCT3.
	RLOS/LOTC4	O	Receive Loss Of Sync / Loss Of Transmit Clock for SCT4.
	RMSYNC1	O	Receive Multiframe Sync for SCT1.
	RMSYNC2	O	Receive Multiframe Sync for SCT2.
	RMSYNC3	O	Receive Multiframe Sync for SCT3.
	RMSYNC4	O	Receive Multiframe Sync for SCT4.
	RNEGI1	I	Receive Negative Data for the Framer on SCT1.
	RNEGI2	I	Receive Negative Data for the Framer on SCT2.
	RNEGI3	I	Receive Negative Data for the Framer on SCT3.
	RNEGI4	I	Receive Negative Data for the Framer on SCT4.
	RNEGO1	O	Receive Negative Data from the LIU on SCT1.
	RNEGO2	O	Receive Negative Data from the LIU on SCT2.
	RNEGO3	O	Receive Negative Data from the LIU on SCT3.
	RNEGO4	O	Receive Negative Data from the LIU on SCT4.
	RPOSI1	I	Receive Positive Data for the Framer on SCT1.
	RPOSI2	I	Receive Positive Data for the Framer on SCT2.
	RPOSI3	I	Receive Positive Data for the Framer on SCT3.
	RPOSI4	I	Receive Positive Data for the Framer on SCT4.
	RPOSO1	O	Receive Positive Data from the LIU on SCT1.
	RPOSO2	O	Receive Positive Data from the LIU on SCT2.
	RPOSO3	O	Receive Positive Data from the LIU on SCT3.
	RPOSO4	O	Receive Positive Data from the LIU on SCT4.
	RRING1	I	Receive Analog Ring Input for SCT1.
	RRING2	I	Receive Analog Ring Input for SCT2.
	RRING3	I	Receive Analog Ring Input for SCT3.
	RRING4	I	Receive Analog Ring Input for SCT4.
	RSER1	O	Receive Serial Data for SCT1.
	RSER2	O	Receive Serial Data for SCT2.
	RSER3	O	Receive Serial Data for SCT3.
	RSER4	O	Receive Serial Data for SCT4.
	RSIG1	O	Receive Signaling Output for SCT1.
	RSIG2	O	Receive Signaling Output for SCT2.
	RSIG3	O	Receive Signaling Output for SCT3.
	RSIG4	O	Receive Signaling Output for SCT4.
	RSIGF1	O	Receive Signaling Freeze Output for SCT1.
	RSIGF2	O	Receive Signaling Freeze Output for SCT2.
	RSIGF3	O	Receive Signaling Freeze Output for SCT3.
	RSIGF4	O	Receive Signaling Freeze Output for SCT4.
	RSYNC1	I/O	Receive Sync for SCT1.
	RSYNC2	I/O	Receive Sync for SCT2.
	RSYNC3	I/O	Receive Sync for SCT3.
	RSYNC4	I/O	Receive Sync for SCT4.
	RSYSCLK1	I	Receive System Clock for SCT1.
	RSYSCLK2	I	Receive System Clock for SCT2.
	RSYSCLK3	I	Receive System Clock for SCT3.
	RSYSCLK4	I	Receive System Clock for SCT4.
	RTIP1	I	Receive Analog Tip Input for SCT1.
	RTIP2	I	Receive Analog Tip Input for SCT2.
	RTIP3	I	Receive Analog Tip Input for SCT3.
	RTIP4	I	Receive Analog Tip Input for SCT4.
	RVDD	–	Receive Analog Positive Supply.
	RVDD	–	Receive Analog Positive Supply.
	RVDD	–	Receive Analog Positive Supply.
	RVDD	–	Receive Analog Positive Supply.
	RVSS	–	Receive Analog Signal Ground

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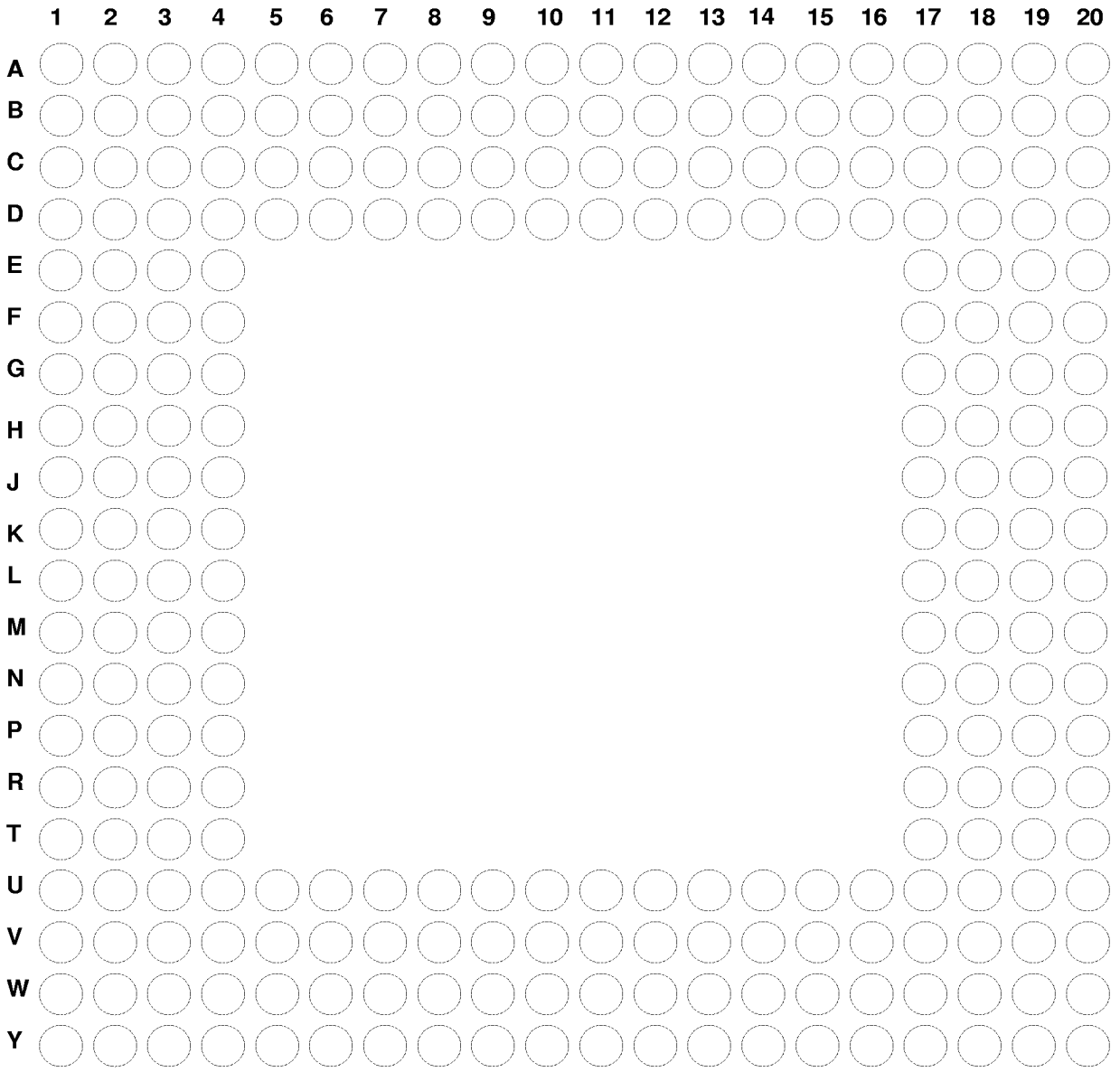
	RVSS	–	Receive Analog Signal Ground
	RVSS	–	Receive Analog Signal Ground
	RVSS	–	Receive Analog Signal Ground
	TCHBLK1	O	Transmit Channel Block for SCT1.
	TCHBLK2	O	Transmit Channel Block for SCT2.
	TCHBLK3	O	Transmit Channel Block for SCT3.
	TCHBLK4	O	Transmit Channel Block for SCT4.
	TCHCLK1	O	Transmit Channel Clock for SCT1.
	TCHCLK2	O	Transmit Channel Clock for SCT2.
	TCHCLK3	O	Transmit Channel Clock for SCT3.
	TCHCLK4	O	Transmit Channel Clock for SCT4.
	TCLK1	I	Transmit Clock for SCT1.
	TCLK2	I	Transmit Clock for SCT2.
	TCLK3	I	Transmit Clock for SCT3.
	TCLK4	I	Transmit Clock for SCT4.
	TCLKI1	I	Transmit Clock Input for the LIU on SCT1.
	TCLKI2	I	Transmit Clock Input for the LIU on SCT2.
	TCLKI3	I	Transmit Clock Input for the LIU on SCT3.
	TCLKI4	I	Transmit Clock Input for the LIU on SCT4.
	TCLKO1	O	Transmit Clock Output from the Framer on SCT1.
	TCLKO2	O	Transmit Clock Output from the Framer on SCT2.
	TCLKO3	O	Transmit Clock Output from the Framer on SCT3.
	TCLKO4	O	Transmit Clock Output from the Framer on SCT4.
	TEST	I	Test (0 = normal operation / 1 = tri-state all outputs).
	TLCLK1	O	Transmit Link Clock for SCT1.
	TLCLK2	O	Transmit Link Clock for SCT2.
	TLCLK3	O	Transmit Link Clock for SCT3.
	TLCLK4	O	Transmit Link Clock for SCT4.
	TLINK1	I	Transmit Link Data for SCT1.
	TLINK2	I	Transmit Link Data for SCT2.
	TLINK3	I	Transmit Link Data for SCT3.
	TLINK4	I	Transmit Link Data for SCT4.
	TNEGI1	I	Transmit Negative Data Input for the LIU on SCT1.
	TNEGI2	I	Transmit Negative Data Input for the LIU on SCT2.
	TNEGI3	I	Transmit Negative Data Input for the LIU on SCT3.
	TNEGI4	I	Transmit Negative Data Input for the LIU on SCT4.
	TNEGO1	O	Transmit Negative Data Output from Framer on SCT1.
	TNEGO2	O	Transmit Negative Data Output from Framer on SCT2.
	TNEGO3	O	Transmit Negative Data Output from Framer on SCT3.
	TNEGO4	O	Transmit Negative Data Output from Framer on SCT4.
	TPOSI1	I	Transmit Positive Data Input for the LIU on SCT1.
	TPOSI2	I	Transmit Positive Data Input for the LIU on SCT2.
	TPOSI3	I	Transmit Positive Data Input for the LIU on SCT3.
	TPOSI4	I	Transmit Positive Data Input for the LIU on SCT4.
	TPOSO1	O	Transmit Positive Data Output from Framer on SCT1.
	TPOSO2	O	Transmit Positive Data Output from Framer on SCT2.
	TPOSO3	O	Transmit Positive Data Output from Framer on SCT3.
	TPOSO4	O	Transmit Positive Data Output from Framer on SCT4.
	TRING1	O	Transmit Analog Ring Output for SCT1.
	TRING2	O	Transmit Analog Ring Output for SCT2.
	TRING3	O	Transmit Analog Ring Output for SCT3.
	TRING4	O	Transmit Analog Ring Output for SCT4.
	TSER1	I	Transmit Serial Data for SCT1.

	TSER2	I	Transmit Serial Data for SCT2.
	TSER3	I	Transmit Serial Data for SCT3.
	TSER4	I	Transmit Serial Data for SCT4.
	TSIG1	I	Transmit Signaling Input for SCT1.
	TSIG2	I	Transmit Signaling Input for SCT2.
	TSIG3	I	Transmit Signaling Input for SCT3.
	TSIG4	I	Transmit Signaling Input for SCT4.
	TSSYNC1	I	Transmit System Sync for SCT1.
	TSSYNC2	I	Transmit System Sync for SCT2.
	TSSYNC3	I	Transmit System Sync for SCT3.
	TSSYNC4	I	Transmit System Sync for SCT4.
	TSYNC1	I/O	Transmit Sync for SCT1.
	TSYNC2	I/O	Transmit Sync for SCT2.
	TSYNC3	I/O	Transmit Sync for SCT3.
	TSYNC4	I/O	Transmit Sync for SCT4.
	TSYSCLK1	I	Transmit System Clock for SCT1.
	TSYSCLK2	I	Transmit System Clock for SCT2.
	TSYSCLK3	I	Transmit System Clock for SCT3.
	TSYSCLK4	I	Transmit System Clock for SCT4.
	TTIP1	O	Transmit Analog Tip Output for SCT1.
	TTIP2	O	Transmit Analog Tip Output for SCT2.
	TTIP3	O	Transmit Analog Tip Output for SCT3.
	TTIP4	O	Transmit Analog Tip Output for SCT4.
	TVDD	–	Transmit Analog Positive Supply.
	TVDD	–	Transmit Analog Positive Supply.
	TVDD	–	Transmit Analog Positive Supply.
	TVDD	–	Transmit Analog Positive Supply.
	TVSS	–	Transmit Analog Signal Ground.
	TVSS	–	Transmit Analog Signal Ground.
	TVSS	–	Transmit Analog Signal Ground.
	TVSS	–	Transmit Analog Signal Ground.
	WR* (R/W*)	I	Write Input (Read/Write).

DS21Q352 / DS21Q552 / DS21Q354 / DS21Q554 PCB Land Pattern Figure 2

The diagram shown below is the lead pattern that will be placed on the target PCB. This is the same pattern that would be seen as viewed through the MCM from the top. The leads are yet to be assigned.



DS21Q352 / DS21Q552 / DS21Q354 / DS21Q554 Mechanical Dimensions