DisplayPort 1:1 Buffer

FEATURES

- **Supports Data Rates up to 2.7 Gbps**
- **Supports Dual-Mode DisplayPort**
- **Output Waveform Mimics Input Waveform Characteristics**
- **Enhanced ESD: 12 KV on all pins**
- **Enhanced Commercial Temperature Range: 0°C to 85°C**
- **36 Pin 6 × 6 QFN Package**

APPLICATIONS

- **Personal Computer Market**
  - **Desktop PC**
  - **Notebook PC**
  - **Docking Station**
  - **Standalone Video Card**

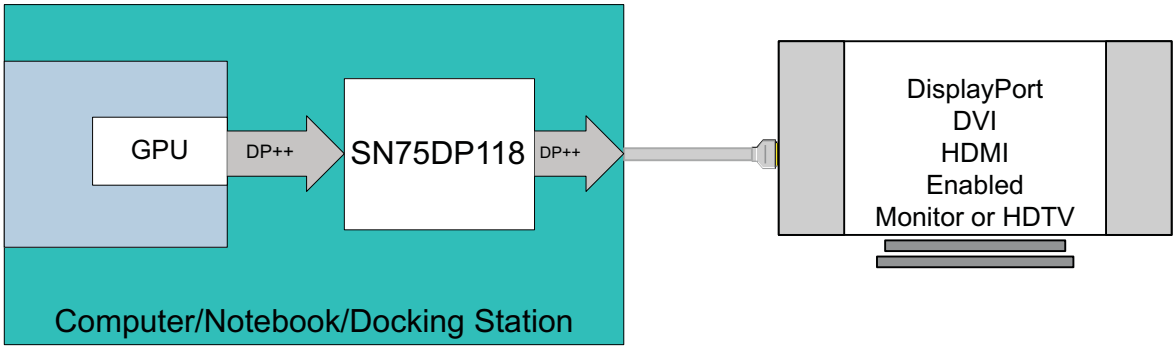
DESCRIPTION

The SN75DP118 is a one Dual-Mode DisplayPort input to one Dual-Mode DisplayPort output. The output follows the input signal in a manner that provides the highest level of signal integrity while supporting the EMI benefits of spread spectrum clocking. The SN75DP118 data rates of up to 2.7 Gbps through each link for a total throughput of up to 10.8 Gbps can be realized.

In addition to the DisplayPort high speed signal lines, the SN75DP118 also supports the Hot Plug Detect (HPD) and Cable Adapter Detect (CAD) channels.

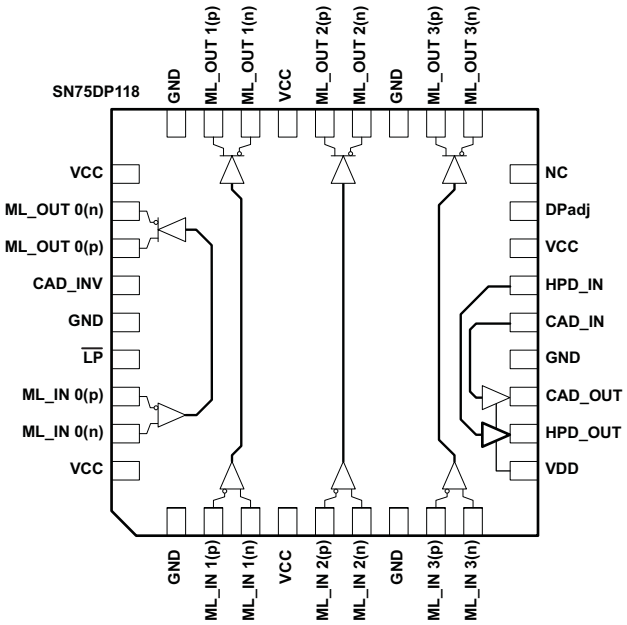
The SN75DP118 is characterized for operation over ambient air temperature of 0°C to 85°C.

TYPICAL APPLICATION

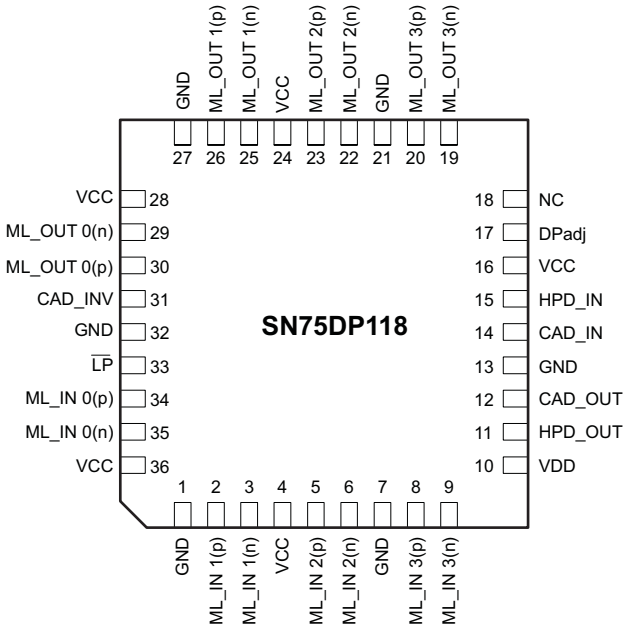


These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DATA FLOW BLOCK DIAGRAM



PACKAGE



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
SIGNAL	NO.		
MAIN LINK INPUT PINS			
ML_IN 0	34, 35	I	DisplayPort Main Link Channel 0 Differential Input
ML_IN 1	2, 3	I	DisplayPort Main Link Channel 1 Differential Input
ML_IN 2	5, 6	I	DisplayPort Main Link Channel 2 Differential Input
ML_IN 3	8, 9	I	DisplayPort Main Link Channel 3 Differential Input
MAIN LINK OUTPUT PINS			
ML_OUT 0	30, 29	O	DisplayPort Main Link Port A Channel 0 Differential Output
ML_OUT 1	26, 25	O	DisplayPort Main Link Port A Channel 1 Differential Output
ML_OUT 2	23, 22	O	DisplayPort Main Link Port A Channel 2 Differential Output
ML_OUT 3	20, 19	O	DisplayPort Main Link Port A Channel 3 Differential Output
HOT PLUG DETECT PINS0			
HPD_OUT	11	O	Hot Plug Detect Output to the DisplayPort Source
HPD_ IN	15	I	Hot Plug Detect Input from the DisplayPort Connector
CABLE ADAPTER DETECT PINS			
CAD _OUT	12	O	Cable Adapter Detect Output to the DisplayPort Source
CAD _ IN	14	I	Cable Adapter Detect Input from the DisplayPort Connector
CONTROL PINS			
$\overline{LP}$	33	I	Low Power Select Bar
CAD_INV	31	I	Output Port Priority selection
DP_{adj}	17	I	DisplayPort Main Link Output Gain Adjustment
NC	16		Not Connected
SUPPLY AND GROUND PINS			
VCC	4, 16, 24, 28, 36		Primary Supply Voltage
VDD	10		HPD and CAD Output Voltage
GND	1, 7, 13, 21, 27, 32		Ground

Table 1. Control Pin Lookup

SIGNAL	LEVEL (1)	STATE	DESCRIPTION
$\overline{LP}$	H	Normal Mode	Normal operational mode for device
	L	Low Power Mode	Device is forced into a Low Power state causing the outputs to go to a high impedance state, All other inputs are ignored.
CAD_INV	H	CAD Inverted	The CAD output logic is inverted from the CAD input
	L	CAD not Inverted	The CAD output logic follows the CAD input
DP_{adj}	4.53 kΩ	Increased Gain	Main Link DisplayPort Output will have an increased voltage swing
	6.49 kΩ	Nominal Gain	Main Link DisplayPort Output will have a nominal voltage swing
	10 kΩ	Decreased Gain	Main Link DisplayPort Output will have a decreased voltage swing

(1) (H) Logic High; (L) Logic Low

ORDERING INFORMATION

PART NUMBER	PART MARKING	PACKAGE(1)
SN75DP118RHHR	DP118	36-pin QFN Reel (large)
SN75DP118RHHT	DP118	36-pin QFN Reel (small)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE	UNIT
Supply Voltage Range(2)	V_{CC}, V_{DD}	–0.3 to 5.5	V
Voltage Range	Main Link I/O (ML_IN x, ML_OUT x) Differential Voltage	1.5	V
	HPD and CAD I/O	–0.3 to VCC + 0.3	V
	Control I/O	–0.3 to VCC + 0.3	V
Electrostatic discharge	Human body model(3)	±12000	V
	Charged-device model(4)	±1000	V
	Machine model(5)	±200	V
Continuous power dissipation		See Dissipation Rating Table	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-B.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101-A.
(5) Tested in accordance with JEDEC Standard 22, Test Method A115-A.

DISSIPATION RATINGS

PACKAGE	PCB JEDEC STANDARD	T_A < 25°C	DERATING FACTOR(1) ABOVE T_A = 25°C	T_A = 85°C POWER RATING
36-pin QFN (RHH)	Low-K	759 mW	7.5 mW/°C	303 mW
	High-K	2127 mW	21.2 mW/°C	851 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX(1)	UNIT
$R_{\theta JB}$	Junction-to-board thermal resistance	4x4 Thermal vias under powerpad		28.11		°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance			32.77		°C/W
P_D	Device power dissipation	$\overline{LP}$ = 5.5 V; ML: V_{PP} = 1200 mV, 2.7 Gbps, PRBS; HPD_IN/CAD_IN/CAD_INV = 5.5 V; V_{CC} = 5.5 V, V_{DD} = 5.25 V; Temp = 85°C; DP_{adj} = 6.49 kΩ		240	280	mW
P_{SD}	Device power dissipation under low power	$\overline{LP}$ = 0V; HPD_IN/CAD_IN/CAD_INV = 5.5V ; V_{CC} = 5.5V , V_{DD} = 5.2 V; Temp = 85°C; DP_{adj} = 6.49 kΩ			40	µW

(1) Maximum Rating is simulated under worse case condition.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{DD}	HPD and CAD Output reference voltage	1.62		5.25	V
T_A	Operating free-air temperature	0		85	°C
MAIN LINK DIFFERENTIAL PINS					
V_{ID}	Peak-to-peak input differential voltage	0.15		1.40	V
d_R	Data rate			2.7	Gbps
R_t	Termination resistance	45	50	55	Ω
$V_{O(term)}$	Output termination voltage	0		2	V
HPD, CAD, AND CONTROL PINS					
V_{IH}	High-level input voltage	2		5.5	V
V_{IL}	Low-level input Voltage	0		0.8	V

DEVICE POWER

The SN75DP118 is designed to operate off of a single 5V supply.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current	$\overline{LP}$ = 5.5 V; ML: V_{PP} = 1200 mV, 2.7 Gbps, PRBS; HPD_IN/CAD_IN/CAD_INV = 5.5 V; V_{CC} = 5.5 V, V_{DD} = 5.25 V; Temp = 85°C; DP_{adj} = 6.49 kΩ		50	55	mA
I_{DD}	Supply current	V_{DD} = 5.5 V		0.1	2	mA
I_{SD}	Shutdown current	$\overline{LP}$ = 0 V; HPD_IN/CAD_IN/CAD_INV = 5.5 V; V_{CC} = 5.5 V, V_{DD} = 5.25 V; Temp = 85°C; DP_{adj} = 6.49 kΩ		4	10	µA

HOT PLUG AND CABLE ADAPTER DETECT

The SN75DP118 has a built in level shifter for the HPD and CAD outputs. The output voltage level of the HPD and CAD pins is defined by the voltage level of the VDD pin. The state of the HPD pin will also set the active state of the device. If HPD is low the device will enter low power mode. Once HPD goes high, the device will come out of low power mode and enter active mode. If HPD goes LOW for a period of time exceeding $t_{T(HPD)}$, the device will enter the low power mode.

ELECTRICAL CHARACTERISTICS

over recommended operating (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH5}	High-level output voltage	I_{OH} = –100 µA, V_{DD} = 5V	4.5		5	V
$V_{OH3.3}$		I_{OH} = –100 µA, V_{DD} = 3.3 V	3		3.3	V
$V_{OH2.5}$		I_{OH} = –100 µA, V_{DD} = 2.5 V	2.25		2.5	V
$V_{OH1.8}$		I_{OH} = –100 µA, V_{DD} = 1.8 V	1.62		1.8	V
V_{OL}	Low-level output voltage	I_{OH} = 100 µA	0		0.4	V
I_H	High-level input current	V_{IH} = 2 V, V_{CC} = 5.5 V	–10		10	µA
I_L	Low-level input current	V_{IL} = 0.8 V, V_{CC} = 5.5 V	–10		10	µA

SWITCHING CHARACTERISTICS

over recommended operating (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PD(CAD)}$	Propagation delay	V_{DD} = 5 V		20	30	ns
$t_{PD(HPD)}$	Propagation delay	V_{DD} = 5 V		70	110	ns
$t_{T(HPD)}$	HPD logic switch time	V_{DD} = 5 V	200		400	ms
$t_{M(HPD)}$	Minimum output pulse duration	V_{DD} = 5 V	100			ns
$t_{Z(HPD)}$	Low power to high-level propagation delay	V_{DD} = 5 V		70	110	ns

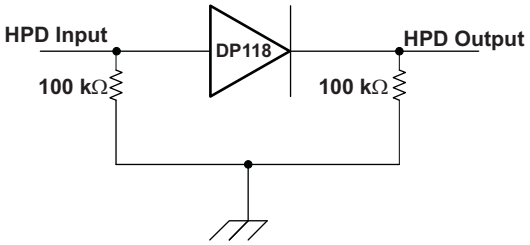


Figure 1. HPD Test Circuit

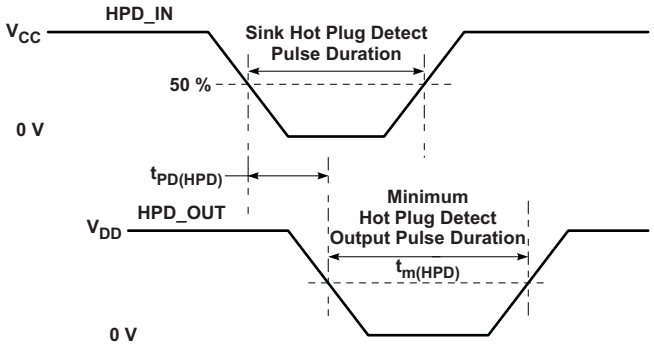


Figure 2. HPD Timing Diagram #1

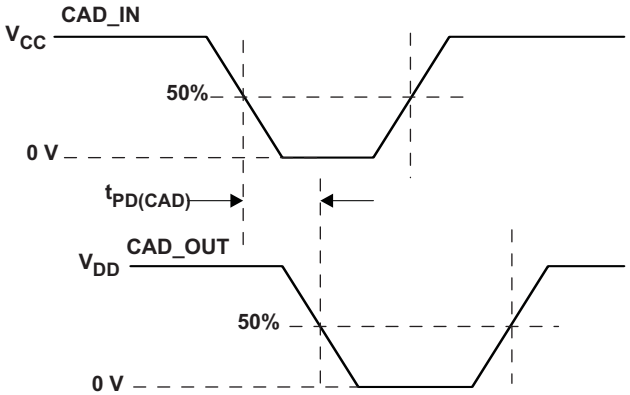


Figure 3. CAD Timing Diagram

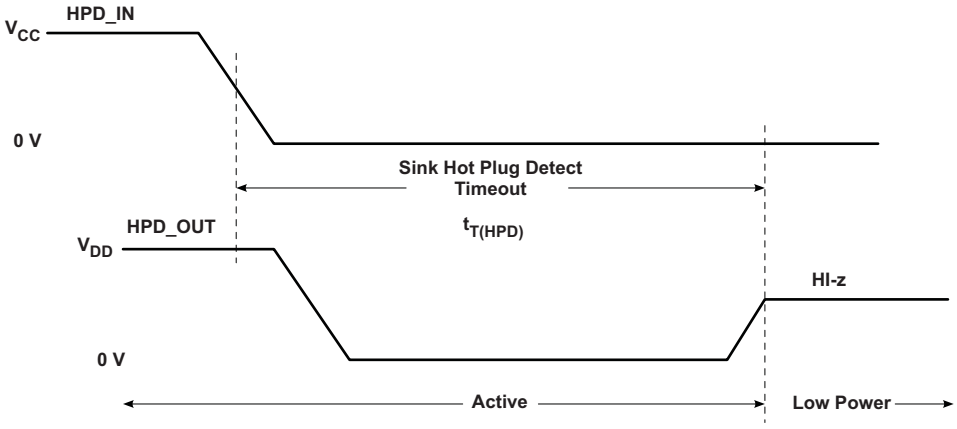


Figure 4. HPD Timing Diagram Number 2

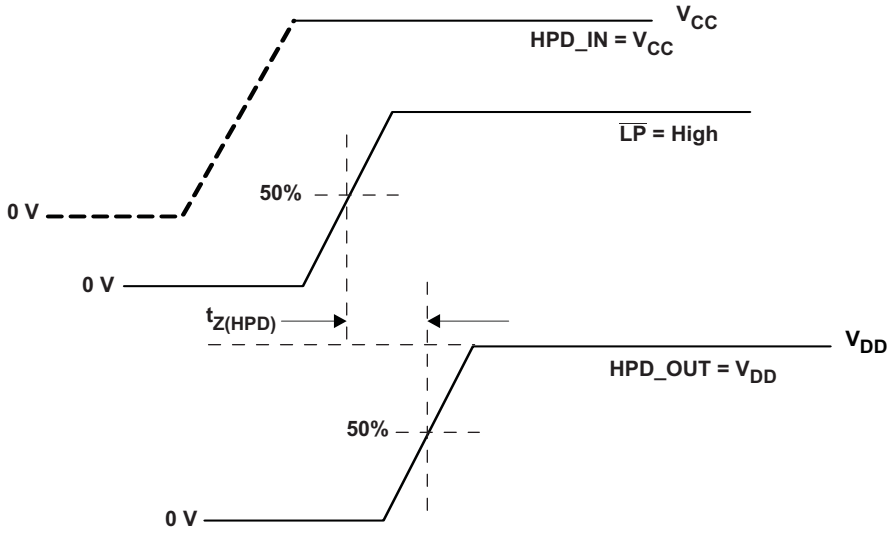


Figure 5. HPD Timing Diagram Number 3

MAIN LINK PINS

The main link I/O of the SN75DP118 is designed to track the magnitude and frequency characteristics of the input waveform and replicate them on the output. A feature has also been incorporated in the SN75DP118 to either increase of decrease the output amplitude via the resistor connected between the DP_{adj} pin and ground.

ELECTRICAL CHARACTERISTICS

over recommended operating (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\Delta V_{I/O(2)}$	Difference between input and output voltages ($V_{OD} – V_{ID}$)	V_{ID} = 200 mV, DP_{adj} = 6.5 kΩ	0	30	60	mV
$\Delta V_{I/O(3)}$		V_{ID} = 300 mV, DP_{adj} = 6.5 kΩ	–24	11	36	
$\Delta V_{I/O(4)}$		V_{ID} = 400 mV, DP_{adj} = 6.5 kΩ	-45	-15	15	
$\Delta V_{I/O(6)}$		V_{ID} = 600 mV, DP_{adj} = 6.5 kΩ	-87	-47	-22	
R_{INT}	Input termination impedance		45	50	55	Ω
V_{Iterm}	Input termination voltage		0		2	V

SWITCHING CHARACTERISTICS

over recommended operating (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{R/F(DP)}$	Output edge rate (20% - 80%)	Input edge rate = 80 ps (20% – 80%)		115		ps
t_{PD}	Propagation delay time	F = 1MHz, V_{ID} = 400 mV	200	240	280	ps
$t_{SK(1)}$	Intra-pair skew	F = 1MHz, V_{ID} = 400 mV			20	ps
$t_{SK(2)}$	Inter-pair skew	F = 1MHz, V_{ID} = 400 mV			40	ps
$t_{DPJIT(PP)}$	Peak-to-peak output residual jitter	dR = 2.7Gbps, V_{ID} = 400 mV, PRBS7		25	35	ps

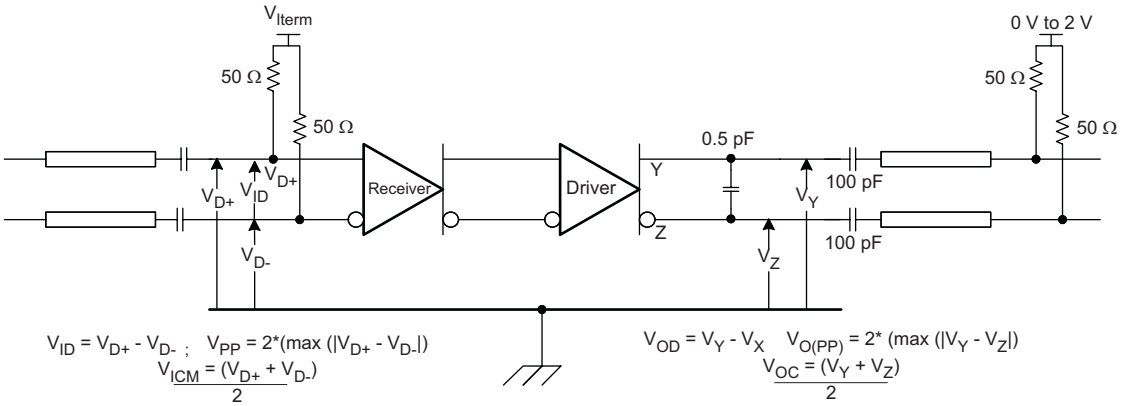


Figure 6. Main Link Test Circuit

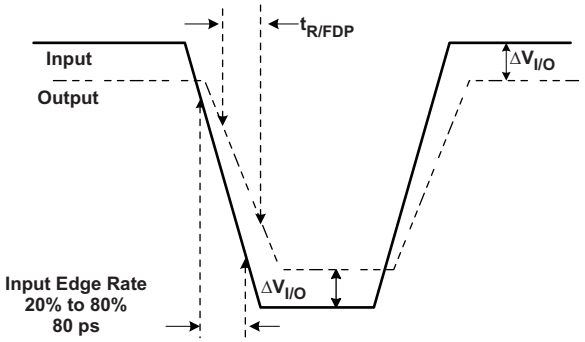


Figure 7. Main Link $\Delta V_{I/O}$ and Edge Rate Measurements

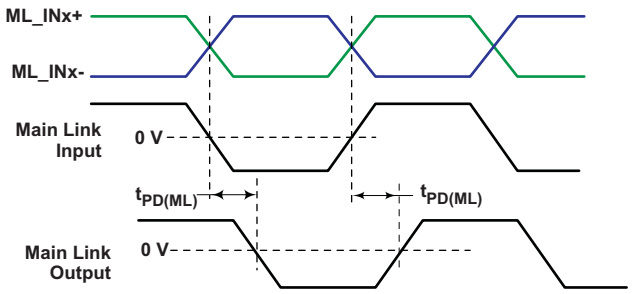


Figure 8. Main Link Delay Measurements

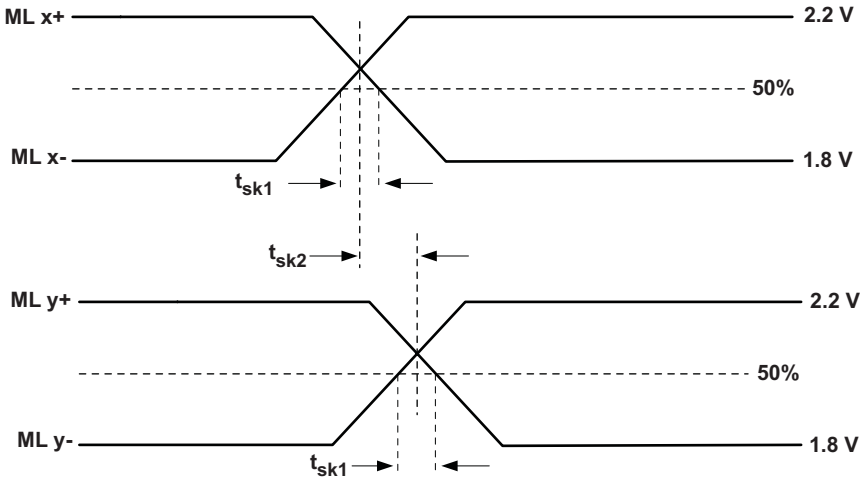


Figure 9. Main Link Skew Measurements

TYPICAL CHARACTERISTICS

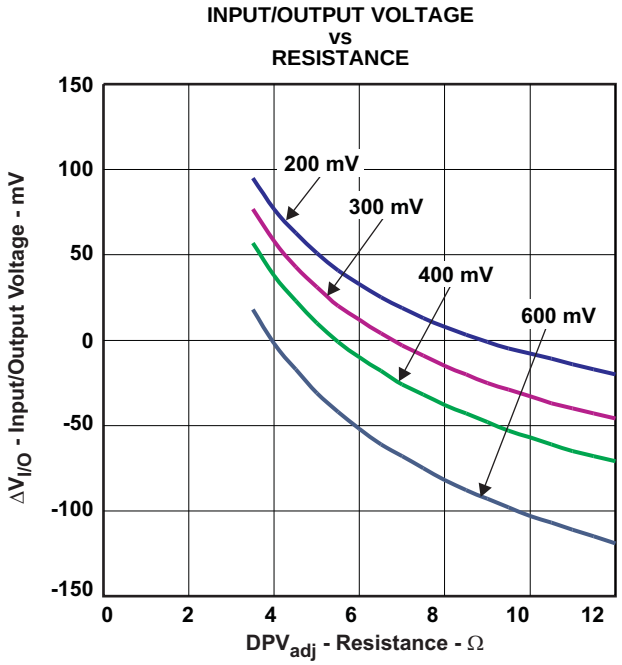


Figure 10.

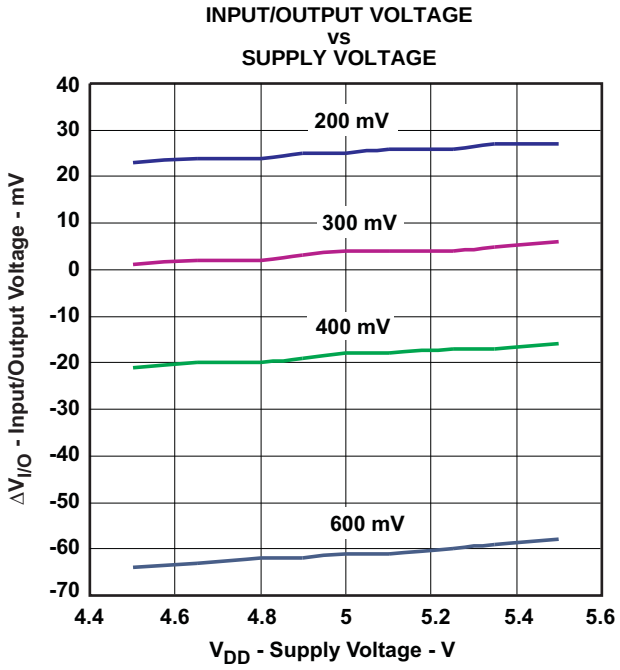


Figure 11.

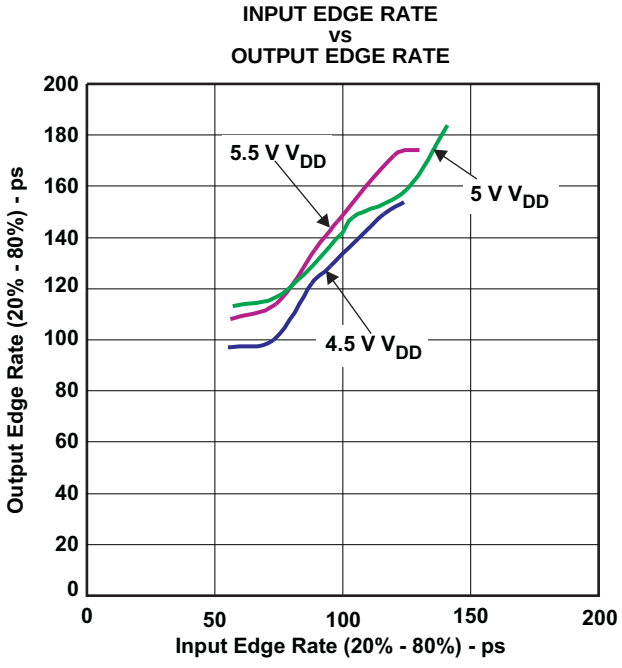


Figure 12.

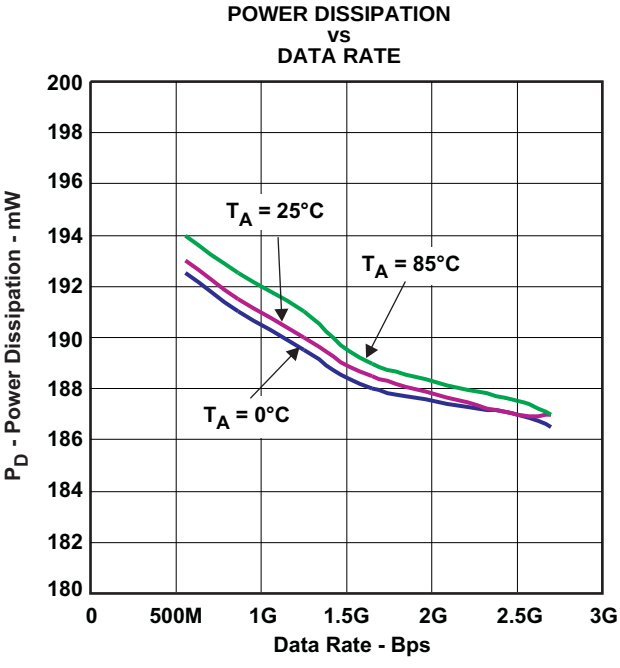


Figure 13.

APPLICATION INFORMATION

Power Logic

The power logic of the SN75DP118 is tied to the state of the HPD input pin as well as the low power pin. When HPD_IN is LOW the SN75DP118 enters the low power state. In this state the outputs are high impedance and the device shuts down to optimize power conservation. When HPD_IN goes high the device enters the normal operational state.

Several key factors were taken into consideration with this digital logic implementation of channel selection, as well as HPD repeating. This logic is described in the following scenarios.

Scenario 1. Low Power State to Active State:

- There are two possible cases for this scenario depending on the state of the low power pin.
  - Case one: In this case HPD_IN is initially LOW and the low power pin is also LOW. In this initial state the device is in a low power mode. Once the HPD input goes to a HIGH state the device remains in the low power mode, with both the main link and auxiliary I/O in a high impedance state (Figure 14).
  - Case two: In this case HPD_IN is initially LOW and the low power pin is HIGH. In this initial state the device is in a low power mode. Once the HPD input goes to a HIGH state the device comes out of the low power mode and enters active mode, enabling the main link and auxiliary I/O. The HPD output to the source is enabled and follows the logic state of the input HPD (Figure 15). This is specified as $t_{Z(HPD)}$.

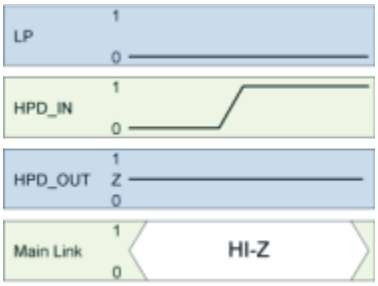


Figure 14.

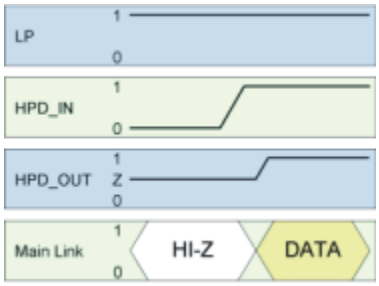


Figure 15.

Scenario 2. HPD Changes:

- In this case the HPD input is initially HIGH. The HPD output logic state follows the state of the HPD input. If the HPD input pulses LOW, as may be the case if the sink device is requesting an interrupt, the HPD output to the source will also pulse Low for the same duration of time with a slight delay (Figure 16). The delay of this signal through the SN75DP118 is specified as $t_{PD(HPD)}$. If the duration of the LOW pulse is less then $t_{M(HPD)}$ it may not be accurately repeated to the source. If the duration of the LOW pulse exceeds $t_{T(HPD)}$ the device determines that an unplug event has occurred and enters the low power state (Figure 17). Once the HPD input goes high again the device returns to the active state as indicated in scenario 1.

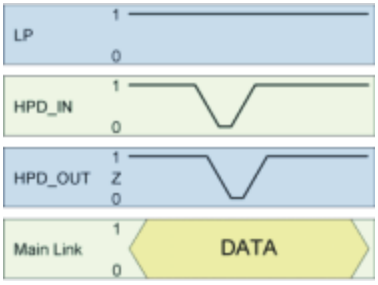


Figure 16.

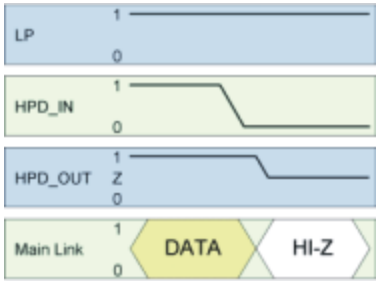


Figure 17.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75DP118RHHR	ACTIVE	VQFN	RHH	36	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 85	DP118	Samples
SN75DP118RHHT	ACTIVE	VQFN	RHH	36	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 85	DP118	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

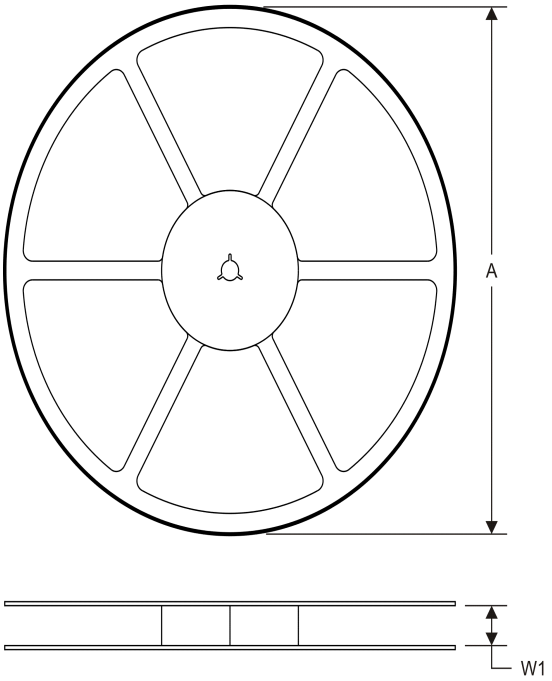
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

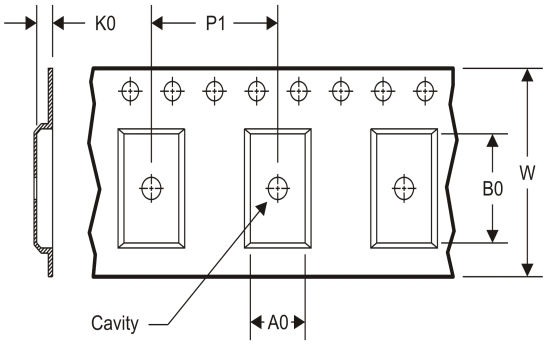
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



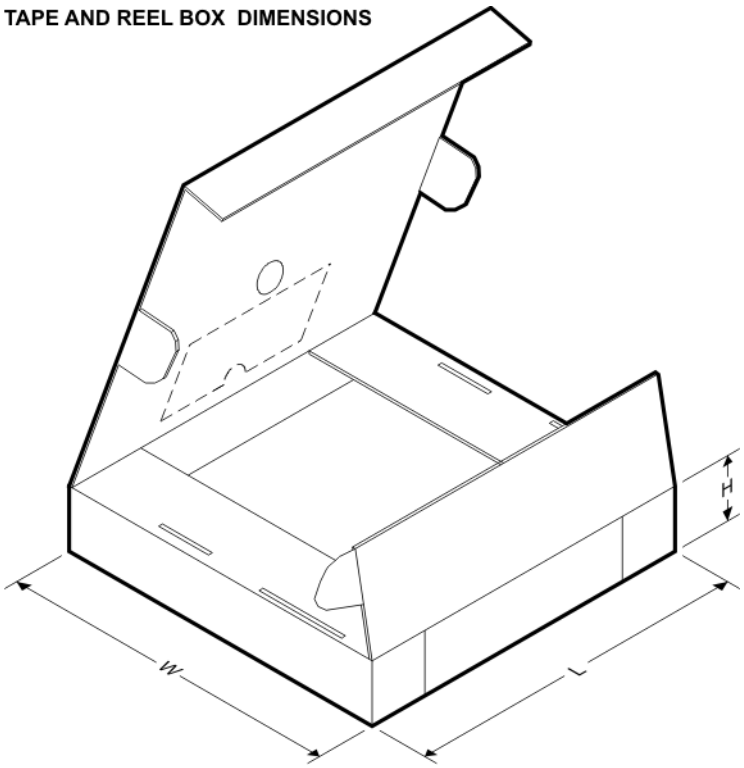
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75DP118RHHR	VQFN	RHH	36	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
SN75DP118RHHT	VQFN	RHH	36	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

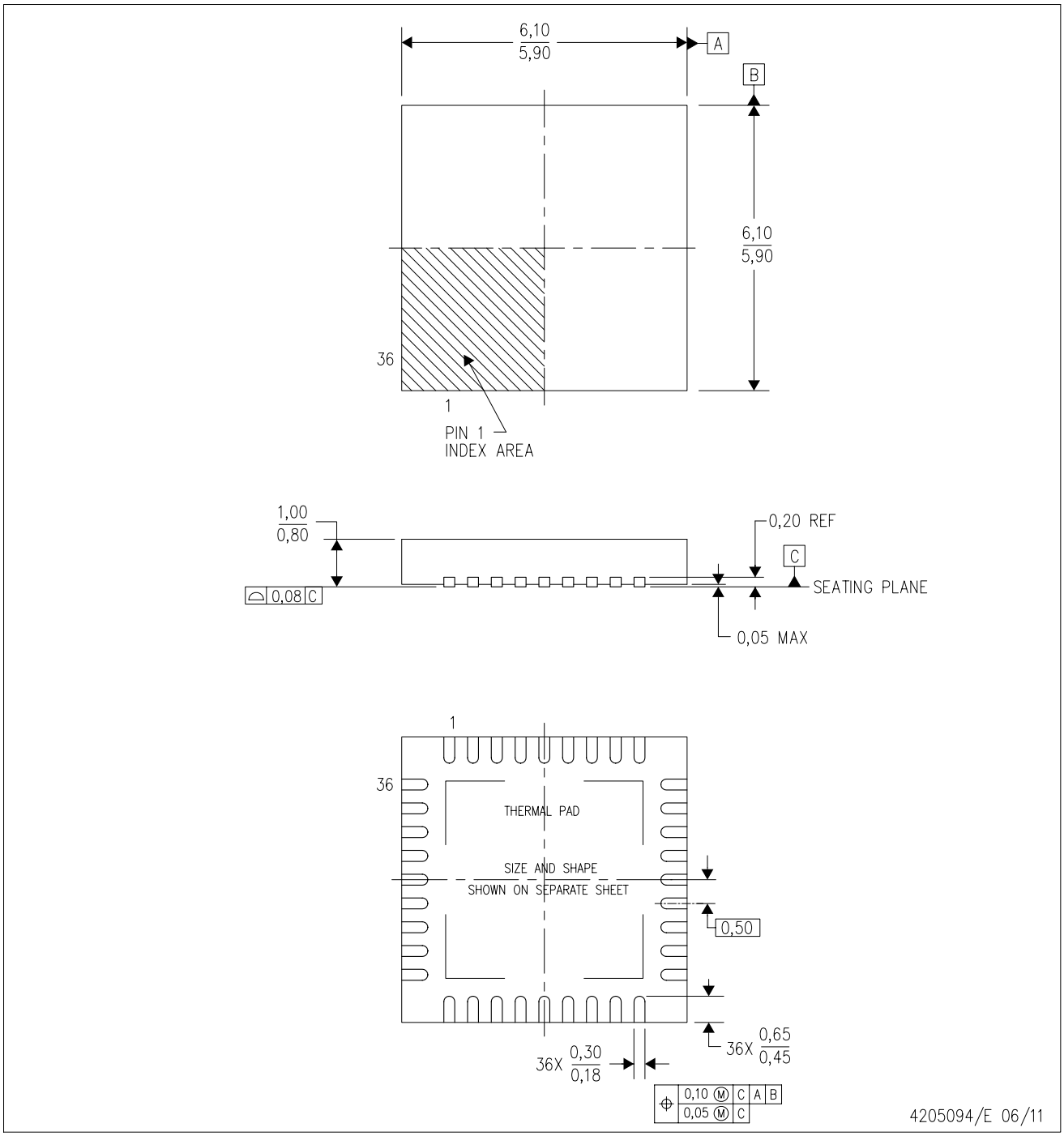
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75DP118RHHR	VQFN	RHH	36	2500	367.0	367.0	38.0
SN75DP118RHHT	VQFN	RHH	36	250	210.0	185.0	35.0

RHH (S–PVQFN–N36) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

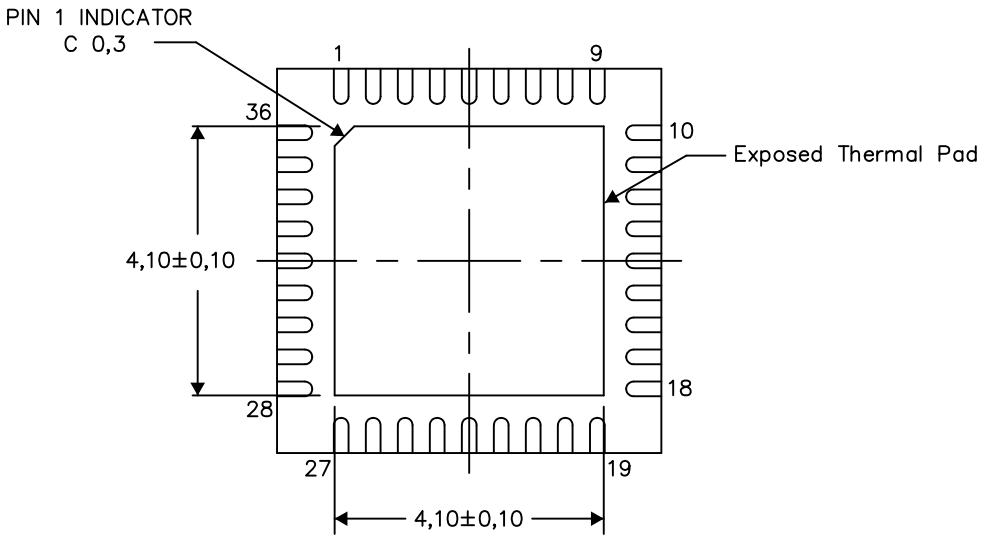
RHH (S–PVQFN–N36) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



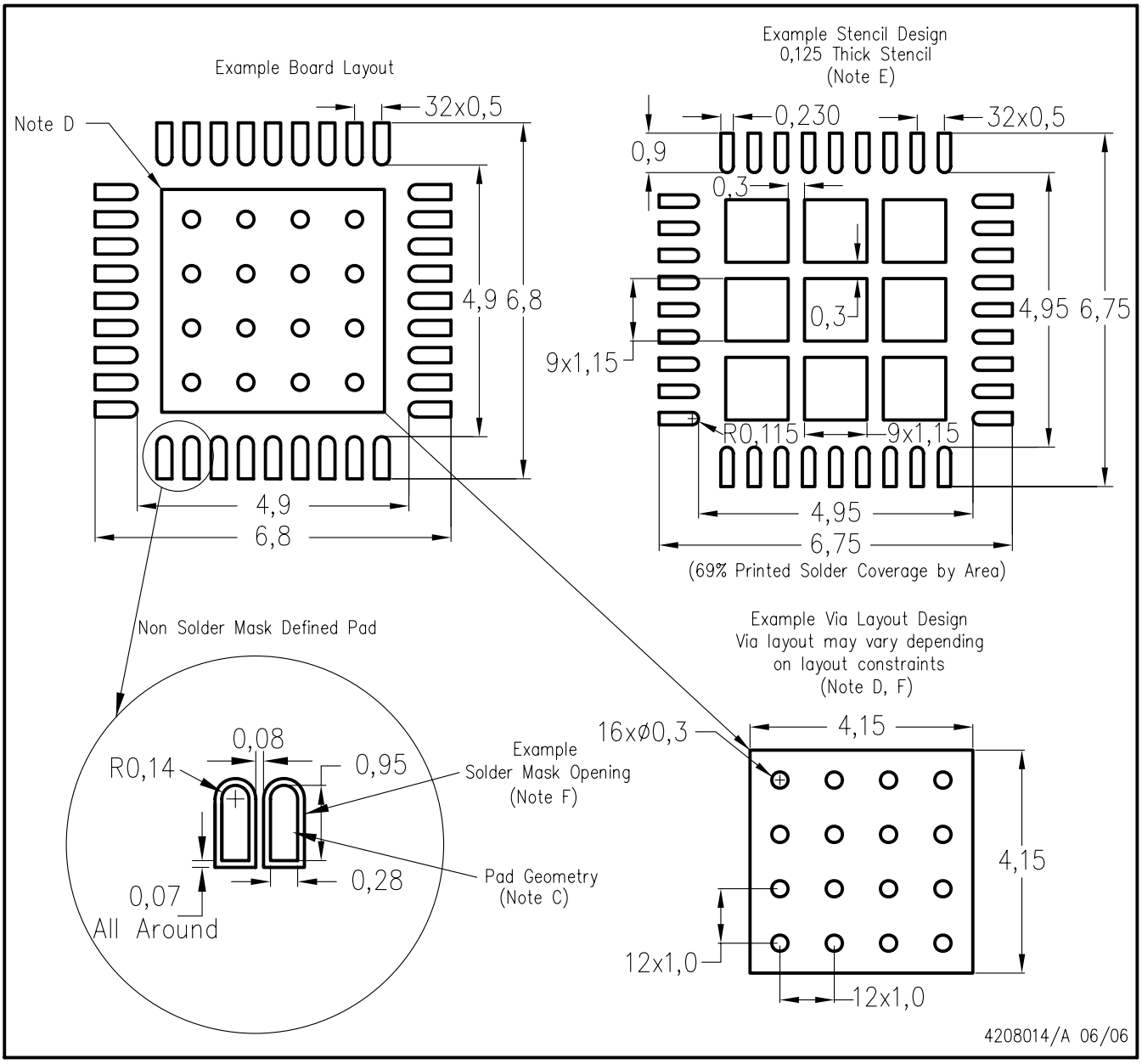
Bottom View

Exposed Thermal Pad Dimensions

4206362–3/M 11/13

NOTE: All linear dimensions are in millimeters

RHH (S–PQFP–N36)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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