SLLS162D - JULY 1993 - REVISED SEPTEMBER 2003

9**∏** 3A

- Meets or Exceeds the Standard EIA-485
- **Designed for High-Speed Multipoint** Transmission on Long Bus Lines in Noisy **Environments**
- Supports Data Rates up to and Exceeding **Ten Million Transfers Per Second**
- Common-Mode Output Voltage Range of -7 V to 12 V
- **Positive- and Negative-Current Limiting**
- Low Power Consumption . . . 1.5 mA Max (Output Disabled)
- **Functionally Interchangeable With SN75174**

description

The SN65LBC174 and SN75LBC174 are monolithic, quadruple, differential line drivers with 3-state outputs. Both devices are designed to meet the requirements of the Electronics Industry Association Standard EIA-485. These devices are optimized for balanced multipoint bus transmission at data rates up to and exceeding 10 million bits per second. Each driver features wide positive and negative common-mode output voltage ranges, current limiting, and thermalshutdown protection, making it suitable for party-line applications in noisy environments. Both devices are designed using LinBiCMOS™, facilitating ultralow power consumption and inherent robustness.

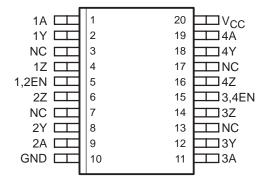
Both the SN65LBC174 and SN75LBC174 provide positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. These devices offer optimum performance when used SN75LBC173 or SN75LBC175 the quadruple line receivers. The SN65LBC174 and SN75LBC174 are available in the 16-terminal DIP package (N) and the 20-terminal wide-body small outline intergrated circuit (SOIC) package (DW).

(TOP VIEW) 16 V_{CC} 1A [1Y [15**∏** 4A 2 1Z **∏** 14 **1** 4Y 3 13 \ 4Z 1,2EN □ 4 2Z [5 12 3,4EN 11 3Z 2Y ∏ 6 10 3Y 7 2А П

N PACKAGE

DW PACKAGE (TOP VIEW)

GND [8



NC - No internal connection

FUNCTION TABLE (each driver)

INPUT	ENABLE	OUTPUTS			
	LINADEL	Υ	Z		
Н	Н	Н	L		
L	Н	L	Н		
Х	L	Z	Z		

H = high level,L = low level,

X = irrelevant.Z = high impedance (off)

The SN75LBC174 is characterized for operation over the commercial temperature range of 0°C to 70°C. The SN65LBC174 is characterized over the industrial temperature range of -40°C to 85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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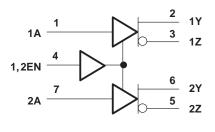
SLLS162D - JULY 1993 - REVISED SEPTEMBER 2003

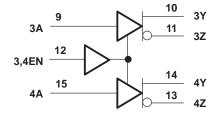
logic symbol[†]

1,2EN 4 ΕN 2 1Y 3 1Z ∇ 6 2Y 5 2Z 12 3,4EN EN \triangleright 10 **3**Y 3A 11 ∇ 3Z 14 4Y 15 13 4Z

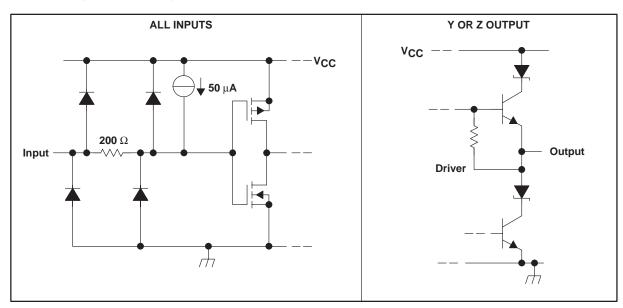
Terminal numbers shown are for the N package.

logic diagram (positive logic)





schematic of inputs and outputs



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN65LBC174, SN75LBC174 QUADRUPLE LOW-POWER DIFFERENTIAL LINE DRIVERS

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absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V _{CC} (see Note 1)		0.3 V to 7 V
Output voltage range, VO		–10 V to 15 V
		0.3 V to V _{CC} +0.5 V
Continuous total power dissipation		Internally limited‡
Operating free-air temperature range, TA:	SN65LBC174	–40°C to 85°C
	SN75LBC174	0°C to 70°C
Storage temperature range, T _{stq}		–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) fror	n case for 10 seconds	260°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, VCC	4.75	5	5.25	V	
High-level input voltage, VIH		2			V
Low-level input voltage, V _{IL}				0.8	V
Voltage of any bus forminal (constraint or common mode) \/a	Y or Z			12	V
Voltage at any bus terminal (separately or common-mode), VO	Y OI Z			-7	V
High-level output current, IOH	Y or Z			-60	mA
Low-level output current, IOL	Y or Z			60	mA
Continuous total power dissipation		See Dissipation Rating			g Table
Operation from air temperature T.	SN65LBC174	-40		85	°C
Operating free-air temperature, T _A	SN75LBC174	0		70	C

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25^{\circ}C$ POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW	585 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW



[‡] The maximum operating junction temperature is internally limited. Use the Dissipation Rating Table to operate below this temperature. NOTE 1: All voltage values are with respect to GND.

SN65LBC174, SN75LBC174 QUADRUPLE LOW-POWER DIFFERENTIAL LINE DRIVERS

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST (CONDITIONS	MIN	TYP [†]	MAX	UNIT	
VIK	Input clamp voltage	$I_{I} = -18 \text{ mA}$				-1.5	V	
		$R_L = 54 \Omega$,	SN65LBC174	1.1	1.8	5		
11/2-1	Differential and and make as ‡	See Figure 1	SN75LBC174	1.5	1.8	5	V	
IVODI	Differential output voltage [‡]	$R_L = 60 \Omega$,	SN65LBC174	1.1	1.7	5	v	
		See Figure 2	SN75LBC174	1.5	1.7	5		
Δ V _{OD}	Change in magnitude of common-mode output voltage§					±0.2	V	
Voc	Common-mode output voltage	R _L = 54 Ω,	See Figure 1			3 -1	V	
Δ VOC	Change in magnitude of common-mode output voltage§					±0.2	V	
IO	Output current with power off	$V_{CC} = 0$,	$V_0 = -7 \text{ V to } 12 \text{ V}$			±100	μА	
loz	High-impedance-state output current	$V_O = -7 \text{ V to } ^{-1}$	12 V			±100	μА	
lН	High-level input current	V _I = 2.4 V				-100	μΑ	
IIL	Low-level input current	V _I = 0.4 V				-100	μΑ	
los	Short-circuit output current	$V_0 = -7 \text{ V to } 1$	12 V			±250	mA	
la a	Supply current (all drivers)	No load	Outputs enabled			7	m A	
Icc	Supply current (all univers)	INU IUAU	Outputs disabled			1.5	mA	

[†] All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^{\circ}\text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST C	MIN	TYP	MAX	UNIT	
t _d (OD)	Differential output delay time	Di - 54 O	See Figure 3	2	11	20	ns
t _t (OD)	Differential output transition time	$R_L = 54 \Omega$,	10	15	25	ns	
^t PZH	Output enable time to high level	R _L = 110 Ω,	See Figure 3		20	30	ns
tPZL	Output enable time to low level	R _L = 110 Ω,	See Figure 5		21	30	ns
^t PHZ	Output disable time from high level	R _L = 110 Ω,	See Figure 4		48	70	ns
^t PLZ	Output disable time from low level	$R_L = 110 \Omega$,	See Figure 5		21	30	ns

[‡] The minimum V_{OD} specification does not fully comply with EIA-485 at operating temperatures below 0°C. The lower output signal should be used to determine the maximum signal transmission distance.

^{§ ∆|}V_{OD}| and ∆|V_{OC}| are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

PARAMETER MEASUREMENT INFORMATION

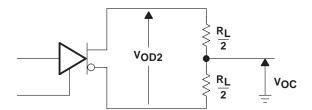


Figure 1. Differential and Common-Mode Output Voltages

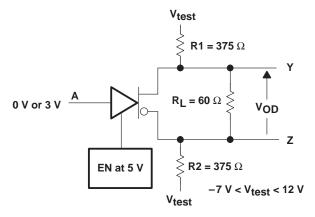
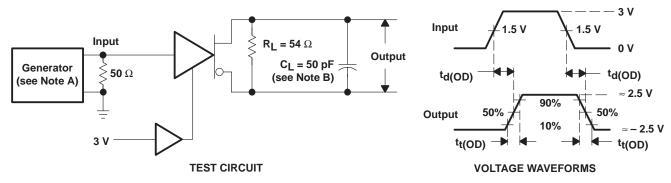


Figure 2. Driver V_{OD} Test Circuit



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle = 50%, $t_f \leq$ 5 ns, $t_f \leq$ 7 ns, $t_f \leq$ 8 ns, $t_f \leq$ 8 ns, $t_f \leq$ 9 ns, $t_$

B. C_L includes probe and stray capacitance.

Figure 3. Time Waveforms for Driver Differential Output Test Circuit Delay and Transition

PARAMETER MEASUREMENT INFORMATION

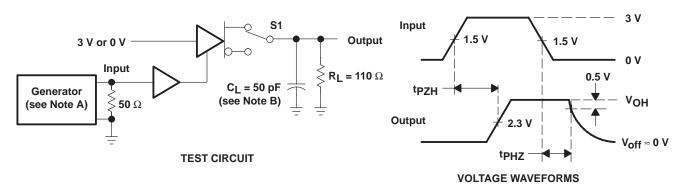
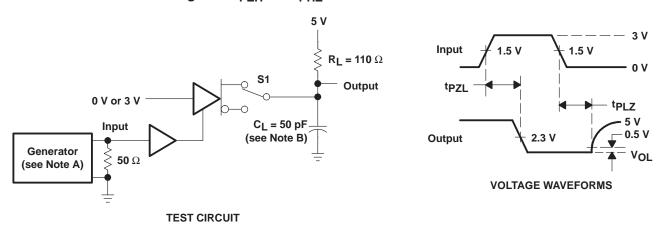


Figure 4. tpzH and tpHZ Test Circuit and Waveforms

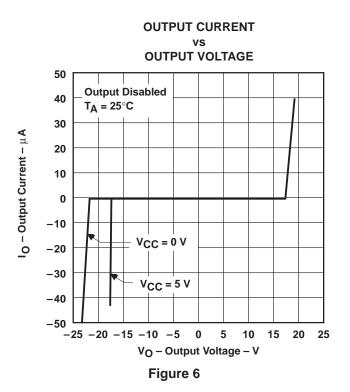


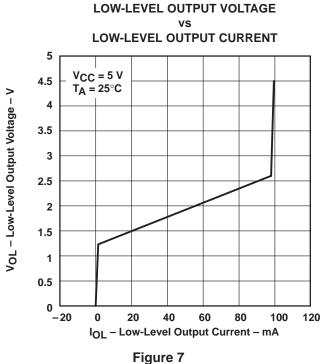
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle = 50%, $t_f \leq$ 5 ns, $Z_O = 50 \ \Omega$.

B. C_L includes probe and stray capacitance.

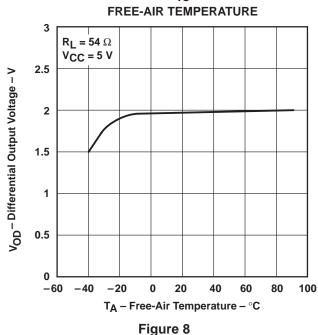
Figure 5. tpzL and tpLZ Test Circuit and Waveforms

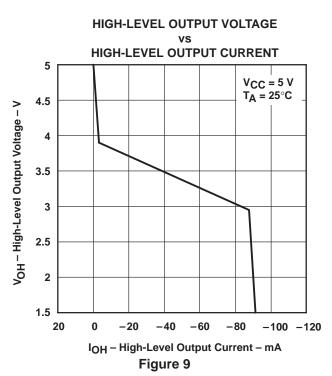
TYPICAL CHARACTERISTICS





DIFFERENTIAL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE





TYPICAL CHARACTERISTICS

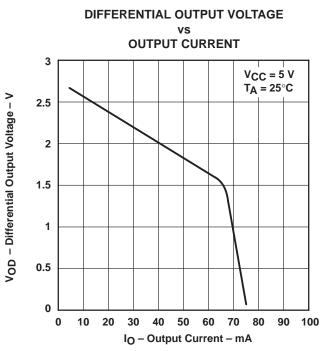
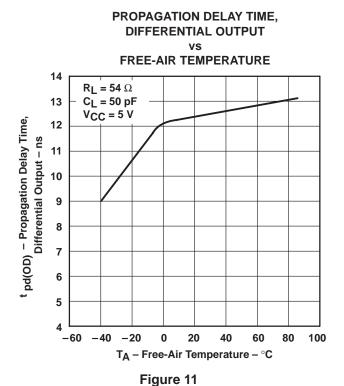


Figure 10







14-May-2013

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Top-Side Markings	Samples
SN65LBC174DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	(3) Level-1-260C-UNLIM	-40 to 85	SN65LBC174	Samples
SN65LBC174DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SN65LBC174	Samples
SN65LBC174DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SN65LBC174	Samples
SN65LBC174DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SN65LBC174	Samples
SN65LBC174N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN65LBC174N	Samples
SN65LBC174NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN65LBC174N	Samples
SN75LBC174DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75LBC174	Samples
SN75LBC174DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75LBC174	Samples
SN75LBC174DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75LBC174	Samples
SN75LBC174DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75LBC174	Samples
SN75LBC174N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75LBC174N	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



PACKAGE OPTION ADDENDUM

14-May-2013

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sh/Rr): Til defines "Green" to mean Ph-Free (RoHS compatible) and free of Browing (Rr) and Antimony (Sh) based flame retardants (Br or Sh do not exceed 0.1% by weight

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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OTHER QUALIFIED VERSIONS OF SN75LBC174:

Military: SN55LBC174

NOTE: Qualified Version Definitions:

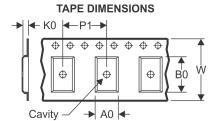
• Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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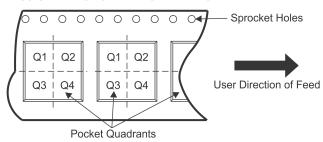
TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

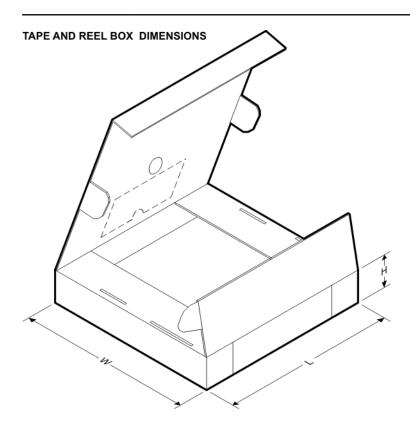
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC174DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN75LBC174DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC174DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN75LBC174DWR	SOIC	DW	20	2000	367.0	367.0	45.0

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



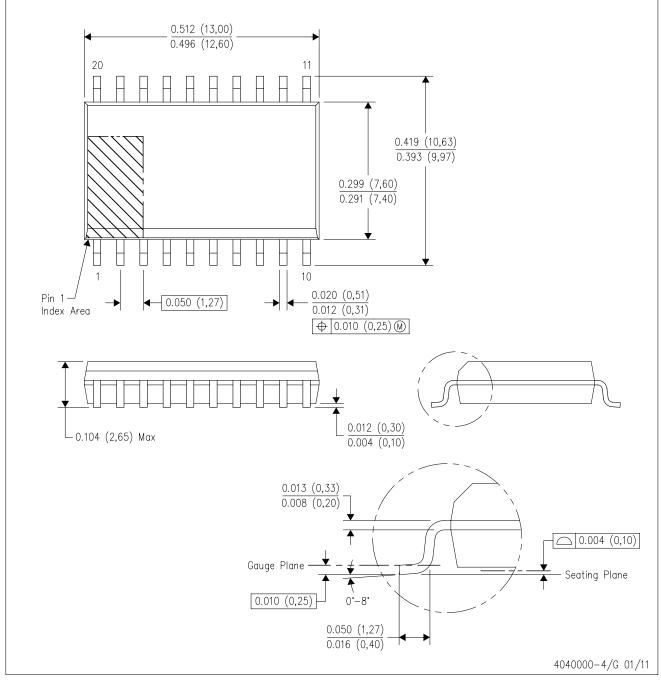
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



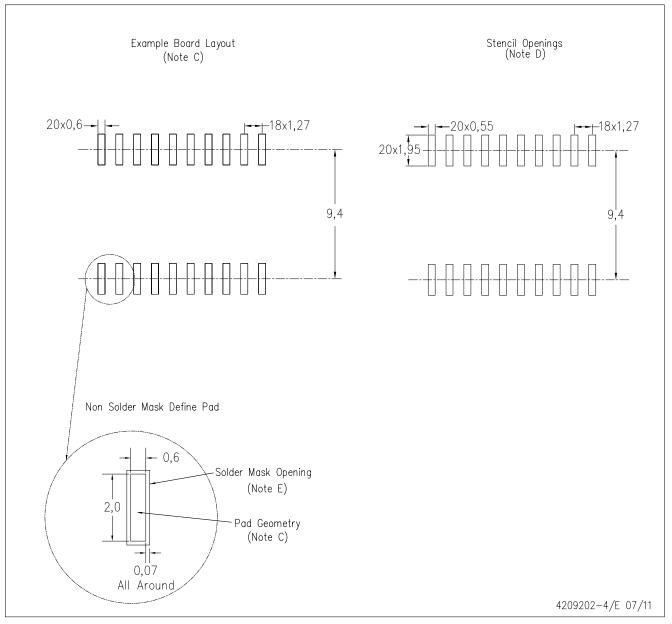
NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC—7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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Products Applications

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