



High-Speed, Low r_{ON} , SPST Analog Switch (1-Bit Bus Switch with Level-Shifter)

FEATURES

- SC-70 5-Lead Package
- 5- Ω Switch Connection Between Two Ports
- Minimal Propagation Delay Through The Switch
- Low I_{CC}
- Zero Bounce In Flow-Through Mode
- Control Inputs Compatible with TTL Level

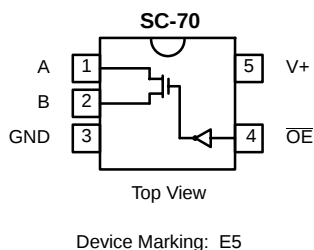
DESCRIPTION

The DG2302 is a high-speed, 1-bit, low power, TTL-compatible bus switch. Using sub-micron CMOS technology, DG2302 achieves low on-resistance and negligible propagation delay.

The DG2302 consist of a bi-directional input/output pins A and

B. When the output enable ($\overline{OE}$) is low, the input/output pins are connected. When the $\overline{OE}$ is high, the switch is open and a high-impedance state exists between input/output pins A and B.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

**TRUTH TABLE**

$\overline{OE}$	B	Function
L	A	Connect
H	HiZ State	Disconnect

ORDERING INFORMATION

Temp Range	Package	Part Number
-40 to 85°C	SC70-5	DG2302DL



ABSOLUTE MAXIMUM RATINGS

Reference to GND

V+ -0.3 to +6 V

 $\overline{OE}$, A, B^a -0.3 to (V+ + 0.3 V)Continuous Current (Any terminal) ± 50 mAPeak Current ± 200 mA
(Pulsed at 1 ms, 10% duty cycle)

Storage Temperature (D Suffix) -65 to 150°C

Power Dissipation (Packages)^b5-Pin SC70^c 250 mW

Notes:

a. Signals on A, or B or $\overline{OE}$ exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

b. All leads welded or soldered to PC Board.

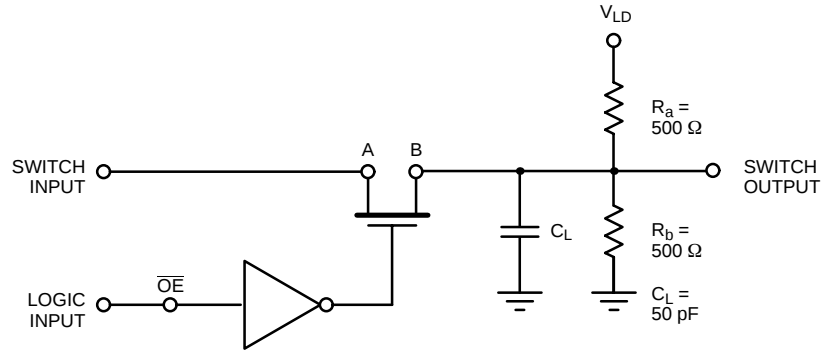
c. Derate 3.1 mW/°C above 70°C

SPECIFICATIONS (V+ = 5.0 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 5 V, ±10%, VIN = 0.8 or 2.0 V ^e	Temp ^a	Limits -40 to 85°C			Unit
				Min ^b	Typ ^c	Max ^b	
DC Characteristics							
On-Resistance	rON	V+ = 4.5 V, VA = 0 V, IB = 64 mA	Full			7	Ω
		V+ = 4.5 V, VA = 0 V, IB = 30 mA	Full			7	
		V+ = 4.5 V, VA = 2.4 V, IB = 15 mA	Full			50	
Switch Off Leakage Current	I(off)	V+ = 5.5 V, VA = 1 V/4.5 V, VB = 4.5 V/1 V	Full	-10		10	μA
Switch-On Leakage Current	I(on)	V+ = 5.5 V, VA = VB = 1 V/4.5 V	Full	-10		10	
Input High Voltage	VIH		Full	2.0			V
Input Low Voltage	VIL		Full			0.8	
Input Current	IIL or IIH	$\overline{V_{OE}} = 0$ or V+	Full	-1		1	μA
Dynamic Characteristics							
Prop Delay Bus-to-Bus ^f	tPHL	VLD = Open (Figure 1 and 2)	Full			1	ns
	tPLH		Full			1	
Output Enable Time ^d	tPZL	VLD = 7 V, V+ = 4.5 V to 5.5 V (Figure 1 and 2)	Full		5.0		
	tPZH	VLD = Open, V+ = 4.5 V to 5.5 V (Figure 1 and 2)	Full		5.0		
Output Disable Time ^d	tPLZ	VLD = 7 V, V+ = 4.5 V to 5.5 V (Figure 1 and 2)	Full		3.9		
	tPHZ	VLD = Open, V+ = 4.5 V to 5.5 V (Figure 1 and 2)	Full		1.0		
Input Capacitance	Cin		Room		3.5		pF
Channel-Off Capacitance ^d	C(off)	$\overline{V_{OE}} = 0$ or V+, f = 1 MHz	Room		5		
Channel-On Capacitance ^d	CON		Room		11		
Power Supply							
Power Supply Range	V+			4.0		5.5	V
Power Supply Current	I+	$\overline{V_{OE}} = 0$			0.9	1.5	mA
		$\overline{V_{OE}} = V+$				1.0	μA

Notes:

- Room = 25°C, Full = as determined by the operating suffix.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Typical values are for design aid only, not guaranteed nor subject to production testing.
- Guarantee by design, nor subjected to production test.
- V_{IN} = input voltage to perform proper function.
- Guaranteed by design and not production tested. The bus switch propagation delay is a function of the RC time constant contributed by the on-resistance and the specified load capacitance with an ideal voltage source (zero output impedance) driving the switch.

AC LOADING AND WAVEFORMS



Input driven by 50-Ω source terminated in 50 Ω
 C_L includes load and stray capacitance
 Input PRR = 1.0 MHz, $t_W = 50$ ns

Figure 1. AC Test Circuit

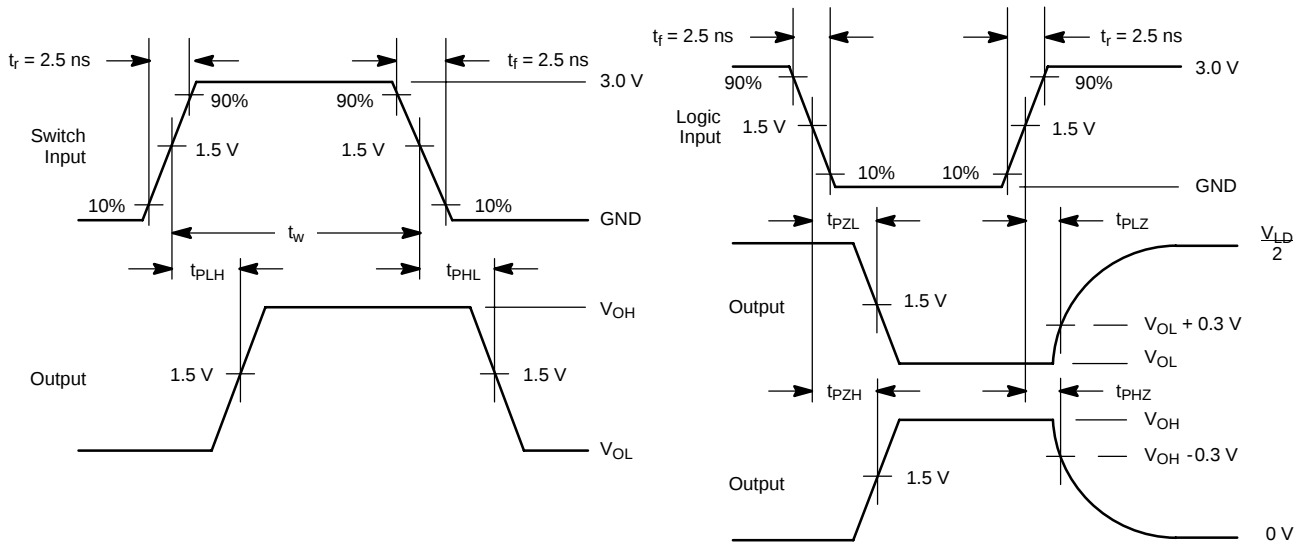


Figure 2. AC Waveforms

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

