



CY3273

Cypress Low Voltage Powerline Communication Evaluation Kit Guide

Doc. # 001-55382 Rev. *A

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Contents



1. Introduction	5
1.1 Introduction to the Cypress PLC Solution	5
1.2 Using the Cypress PLC Solution	5
1.3 Kit Contents	7
1.3.1 Additional Requirements	7
1.4 Document Revision History	8
1.5 Documentation Conventions	8
2. PLC LV Evaluation Board	9
2.1 Features.....	9
2.2 Functional Overview	9
2.2.1 Operating Conditions	9
2.3 Hardware Description	10
2.3.1 Power Supply Circuit.....	11
2.3.2 Transmit Amplifier and Filtering Circuit	11
2.3.3 Transmit and Receive Coupling Circuit.....	11
2.3.4 Cypress Powerline Communication Transceiver and User Controls.....	11
2.4 Setting Up the PLC LV Board	12
2.4.1 I2C Header Settings.....	12
2.4.2 Setting Up Manual Addressing on PLC Boards	13
2.4.3 Setting Up I2C Address of the Node	14
2.4.4 Jumper Settings for the PLC LV Boards	14
A. Appendix	17
A.1 Schematics	17
A.1.1 Board Overview.....	17
A.1.2 User Interface.....	18
A.1.3 Transmit and Receive Filters	19
A.1.4 Power Supply	20
A.2 Layout	21
A.2.1 Top Layer	21
A.2.2 Ground Layer	22
A.2.3 Power Layer	23
A.2.4 Bottom Layer.....	24
A.2.5 Top Silkscreen	25
A.2.6 Bottom Silkscreen	26
A.3 Bill of Materials	27

1. Introduction



1.1 Introduction to the Cypress PLC Solution

Cypress's Powerline Communication Solution (PLC) enables transmission of command and control data over high voltage and low voltage powerlines. This solution is developed for low bandwidth powerline communication.

The CY3273 PLC Low Voltage (LV) Evaluation Board demonstrates the ability of the Cypress PLC family of devices to transmit data at 2400 bps over low voltage (12V to 24V AC/DC) powerlines.

This guide includes the following chapters:

- Chapter 1 provides a brief overview of the Cypress PLC solution. It describes the contents of the CY3273 evaluation kit and lists additional requirements to run the example projects, which are not included as part of the PLC evaluation kit.
- Chapter 2 gives the functional and high level hardware description of the Cypress PLC LV boards. It also describes the setup and operating procedure of the PLC LV board. It describes features such as manual addressing, connection of USB-I2C bridge, and jumper settings with examples.

1.2 Using the Cypress PLC Solution

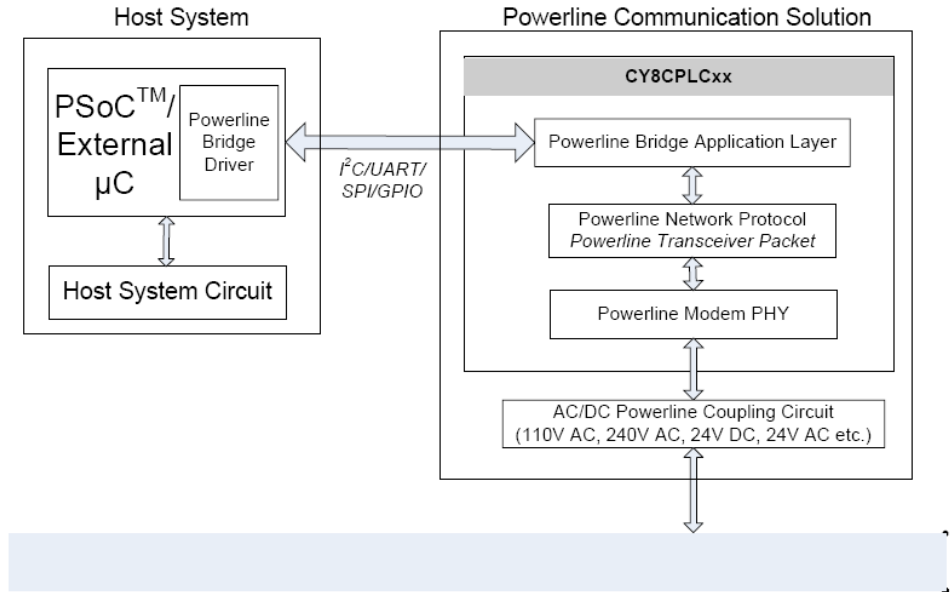
Powerlines are available everywhere in the world and makes them one of the most widely available communication medium for PLC technology. The pervasiveness of powerlines also makes it difficult to predict its characteristics and noise. Because of the variability of the quality of powerline, implementing robust communication over powerline has been an engineering challenge for years. With this in mind, the Cypress PLC solution is designed to enable secure, reliable, and robust communication over powerline. Some of the features of Cypress PLC are:

- Integrated powerline PHY modem with optimized amplifiers to work with rugged low voltage powerlines.
- Powerline optimized network protocol that supports bidirectional communication with acknowledgement based signaling and multiple retries.
- Support for 8-bit packet CRC and 4-bit header CRC for error detection and data packet retransmission.
- Carrier Sense Multiple Access (CSMA) scheme that minimizes collisions between packet transmissions on the powerline.

The Cypress PLC solution consists of four key elements as shown in [Figure 1-1](#).

- Powerline Bridge Application Layer
- Powerline Network Protocol Layer
- Physical Layer FSK Modem
- Power Amplification and Coupling Circuits

Figure 1-1. Cypress PLC Solution Block Diagram



The powerline bridge application layer allows a host system to communicate with the CY8CPLC10 through I²C powerline bridge messages. This layer translates these messages into packets defined by the powerline network protocol.

The powerline bridge application layer allows an external host microcontroller to communicate to the PLC solution using an I²C interface.

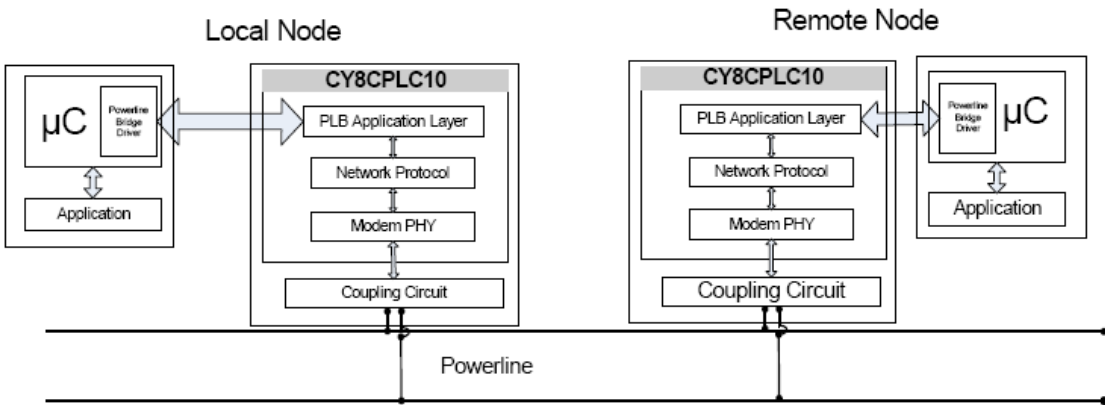
A powerline node interfaced via I2C to a host system is defined as a local node, whereas a node at the opposite end of the powerline is defined as a remote node.

Cypress's powerline optimized Network Protocol performs the functions of the data link, network and transport layers in an ISO/OSI Equivalent Model.

The Network Protocol implemented on the CY8CPLC10 chip aids bidirectional half-duplex communication, multiple masters - slave configurations, implements networking commands and addressing including group broadcasts.

A two node system level diagram is shown in [Figure 1-2](#).

Figure 1-2. PLC System Level Block Diagram – Two Nodes



1.3 Kit Contents

The PLC LV evaluation kit consists of the following:

- CY3273 Quick Start Guide
- CY3273 PLC LV Evaluation Board
- CD containing:
 - CY8CPLC10 Data Sheet
 - Packet Test Software – PLC Control Panel Application
 - CY3273 Evaluation Board User Guide
 - CY3273 Board Altium Design Project
 - CY3273 Board BOM
 - Application Note – *Using CY8CPLC10 in Powerline Communication (PLC) Applications*
 - CY3273 Board Schematics
 - CY3273 Board Gerbers
- 12V Power Supply
- LV Daisy Chain Cable
- USB-I2C Bridge
- Five Wire Ribbon Cable for I2C communication, External Reset, and Powering External Board
- Retractable USB Cable

1.3.1 Additional Requirements

The following Cypress Demonstration Kit is used in the example applications in this user guide. This kit is available for purchase from <http://www.cypress.com>.

CY3210-PSoCEval1 Kit

This PSoC Evaluation Kit features an evaluation board and MiniProg programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread boarding space to meet all your evaluation needs. The MiniProg programming unit is also included with the kit. It programs PSoC devices directly on the evaluation board, or on other boards via a 5-pin header. This programming unit is small and compact, and connects to a PC via a provided USB 2.0 cable.

The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- PSoC Designer Software CD
- 28 Pin CY8C29466-24PXI PDIP PSoC Device Sample
- USB 2.0 Cable
- Getting Started Guide

1.4 Document Revision History

Table 1-1. Revision History

Revision	PDF Creation Date	Origin of Change	Description of Change
**	8/13/09	IUS	New kit guide
*A	12/10/09	RARP	Content updates

1.5 Documentation Conventions

Table 1-2. Document Conventions for Guides

Convention	Usage
Courier New	Displays file locations, user entered text, and source code: C:\ ...cd\icc\
<i>Italics</i>	Displays file names and reference documentation: Read about the <i>sourcefile.hex</i> file in the <i>PSoC Designer User Guide</i> .
[Bracketed, Bold]	Displays keyboard commands in procedures: [Enter] or [Ctrl] [C]
File > Open	Represents menu paths: File > Open > New Project
Bold	Displays commands, menu paths, and icon names in procedures: Click the File icon and then click Open .
Times New Roman	Displays an equation: $2 + 2 = 4$
Text in gray boxes	Describes cautions or unique functionality of the product.

2. PLC LV Evaluation Board



2.1 Features

The key features of the CY3273 evaluation board are:

- Chip power supply derived from 12V to 24V AC/DC
- On-chip powerline bridge application layer, powerline network protocol layer, and physical layer FSK modem
- LED status indicators for Power, Powerline Transmit and Receive, and Band in Use
- Five-position DIP switches
 - Three DIP switches for node logical address selection
 - One DIP switch to configure node I²C addressing mode
 - One DIP switch to select between the external crystal and oscillator
- Integrated Powerline Modem PHY

2.2 Functional Overview

The PLC evaluation board is designed as an advanced evaluation, testing, and product development platform for low bandwidth (2400 bps) powerline communication.

Data to be transmitted is sent to the CY8CPLC10 through the I2C serial communications interface using a serial bridge driver from a host microcontroller to a PC or PSoC device. The serial bridge application on the CY8CPLC10 receives this I2C data and encapsulates it into a PLC Network packet. The on-board FSK modem modulates this packet and the coupling circuitry incorporates the resulting sinusoidal waveform onto the existing waveform on the high voltage powerline bus.

2.2.1 Operating Conditions

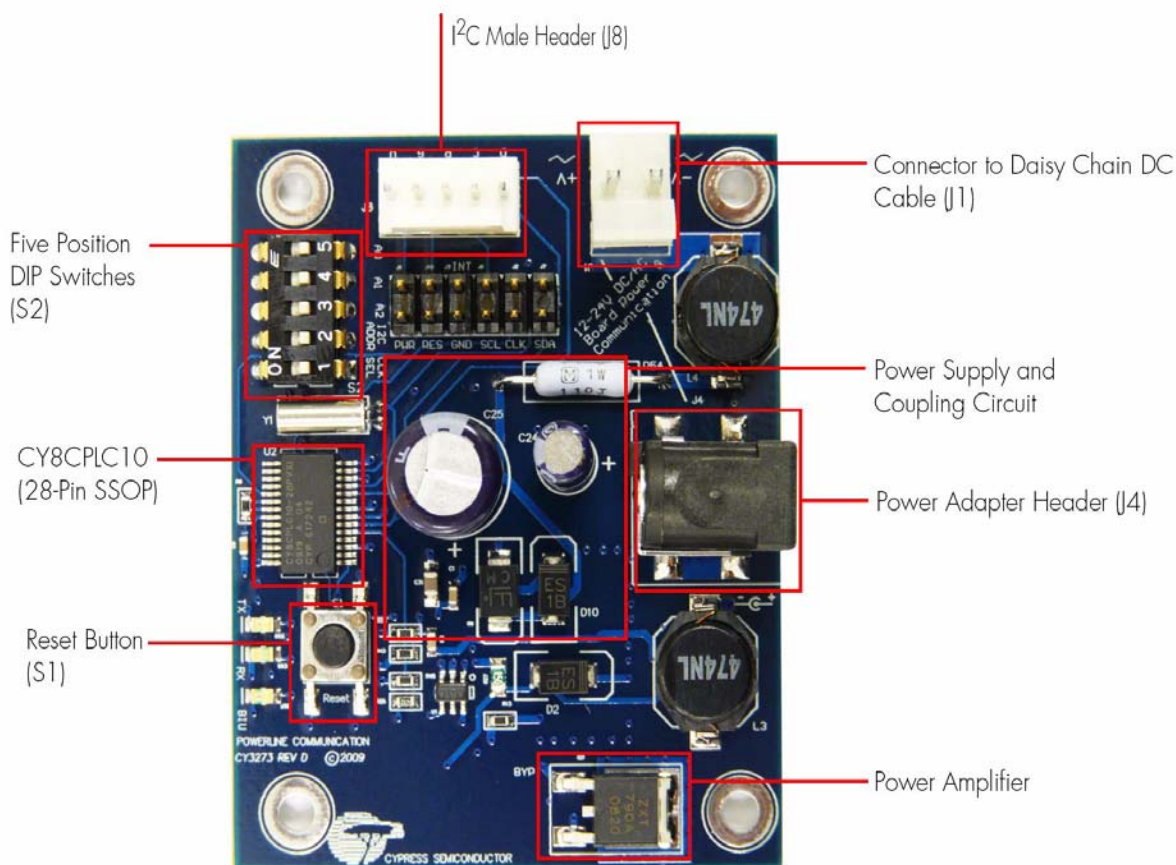
- Input Voltage: 12/24V AC/DC
- Input Current: 200 mA/150 mA
- Operating Temperature: 0°C to 40°C
- Operating Humidity Condition: 5% to 95% RH, non-condensing

2.3 Hardware Description

The low voltage PLC evaluation Board is shown in [Figure 2-1](#). The key sections are highlighted. The board identifies and isolates the power and PLC controller sections. The board is divided into four main sections:

- Power supply circuit
- Transmit amplifier
- Transmit and receive coupling circuit section
- Cypress powerline transceiver and user controls

Figure 2-1. Top View of Cypress PLC LV Evaluation Board



The communication signal flow on this LV board is:

Transmit: CY8CPL10 TX pin → Power amplifier circuitry → LV PLC circuitry → LV powerline (12V to 24V AC/DC)

Receive: LV powerline (12V to 24V AC/DC) → LV PLC circuitry → Passive low pass filtering → Centre biasing → CY8CPLC10 RX pin

The core of the PLC LV board is the CY8CPLC10 chip. The board contains an I²C connector, jumpers to control various functions, and a five-position DIP switch.

2.3.1 Power Supply Circuit

This section takes the power from the powerline and generates necessary low DC voltage for the operation of the PLC transceiver and other components on the chip.

The key components in this section are:

Table 2-1. Power Supply

Component	Description
J4	This is the connector to hook up the power adapter.
U7	5V regulator.
J1	This is a 2 pin header to connect other boards in daisy chain and power them. The cable to do this is provided with the kit. Connect a maximum of five boards in one daisy chain.
DS1	This is a blue LED that glows when the board is powered on.

2.3.2 Transmit Amplifier and Filtering Circuit

This section takes the output signal from the transceiver chip. The circuit here amplifies the signal for transmission over the powerline.

The key components in this section are as follows:

Table 2-2. Transmit Amplifier and Filtering

Component	Description
U1, Q3, Q2	This opamp and high gain transistors are used in the power amplification stage.
Q1	This transistor controls whether transmission is allowed based on the output of the TXDIS-ABLE pin

2.3.3 Transmit and Receive Coupling Circuit

This circuit couples the signal from the board on to the powerline. On the receive side, the same circuit couples the carrier on the powerline into the board, rejecting the low frequency noise on the powerline.

The key components in this section are as follows:

Table 2-3. Transmit and Receive Coupling Circuit

Component	Description
L2	This inductor grounds low frequency signals (for example, AC power) and forms a high pass with C30 and L3.
L4	This inductor along with R54 filters out the higher frequencies.
C10	This is the coupling capacitor which couples the communication signal and rejects the low frequency noise.

2.3.4 Cypress Powerline Communication Transceiver and User Controls

This section is the heart of the board. It has the CY8CPLC10 chip, which has the integrated transceiver modem, network protocol, and the application layer. It also has the I²C header to communicate to the external host processor. The DIP switches to control the addresses and the jumpers to control the functionality of the chip are located here. The red, blue, yellow, and green LEDs indicate the different status of the board when functioning. The key components and their use are as follows:

Table 2-4. Transceiver and User Controls

Component	Description
CY8CPLC10	This is Cypress's powerline transceiver device. It is a 28 pin SSOP device.
PWR LED[DS1]	This is a blue LED that glows when the board is powered on.
Tx LED[DS2]	This is an green LED that glows when the board is transmitting data on to the powerline.
Rx LED[DS3]	This is a red LED that glows when the CY8CPLC10 device is receiving data.
BIU LED [DS5]	This is a yellow LED that glows when the transmit frequency band is in use.
S1	Reset switch to reset the CY8CPLC10 device.
S2[3-5]	These dip switches are used to set up the logical address of the node in the network. This is an easy way for user to quickly assign an address from 0 to 7 to the board in a network. S1[3] is MSB and S1[5] is LSB for logical address assignment.
S2[2]	This dip switch sets the I2C slave address to establish the communication with a host processor. Setting the switch to OFF or ON will set the I2C address to external 0x01 or 0x7a respectively.
S2[1]	This dip switch controls the clock setting to the CY8CPLC10. Setting the switch to 0 or 1 will set the FSK modem clock to external 32 kHz crystal or external 24 MHz oscillator, respectively. Note that the external crystal is always required for protocol timing.

2.4 Setting Up the PLC LV Board

This section describes the components of the PLC Evaluation Board, the process of setting manual addresses on the PLC LV Board and the connection of USB-I2C Bridge and I2C Cable to the I2C header on the board.

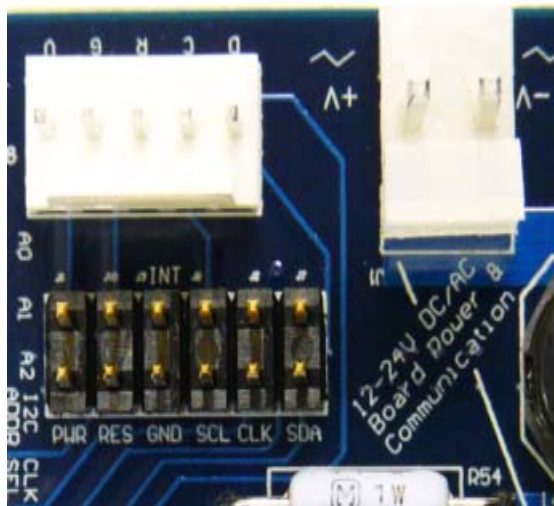
2.4.1 I2C Header Settings

J8 is a five pin header that can be used for communicating with an external board, powering an external board, and resetting the CY8CPLC10 device from an external board. A five wire ribbon cable provided with the CY3273 kit can be used to connect to J8. The description for J8 header pins is as follows:

Table 2-5. J8 I2C Header Pins

J5 Pin Name	Description
V – Vdd	The Vdd pin can provide a maximum of 50 mA at 5V to an external board. It is only to source the current. DO NOT SUPPLY POWER TO THIS PIN FOR POWERING THE CY8CPLC10 DEVICE. Note that the PWR jumper, as explained in the next section, needs to be connected to enable this functionality.
G – Gnd	The Gnd pin can provide the ground reference to an external board. This pin connects to the ground of the CY3273 board.
D – I2C Data (SDA)	The I2C Data (SDA) pin is the data line for the I2C communication. This pin is directly connected to the I2C_SDA pin on the CY8CPLC10 device. Check the next section for appropriate jumper settings for I2C communication through this pin.
C – I2C Clock (SCL)	The I2C Clock (SCL) pin is the clock line for the I2C communication. This pin is directly connected to the I2C_SCL pin on the CY8CPLC10 device. Check the next section for appropriate jumper settings for I2C communication through this pin.
R – Reset	Connecting the reset of an external board to this pin enables the resetting of the CY8CPLC10 device via the external board. Note that the RES jumper, as explained in the next section, needs to be connected to enable this functionality.

Figure 2-2. I2C Header for Communication



2.4.2 Setting Up Manual Addressing on PLC Boards

The PLC evaluation board contains a five position DIP switch. The first three switches S2[3-5] are used to manually set a logical address for the PLC chip. Logical addresses for up to eight nodes can be set up using these DIP switches.

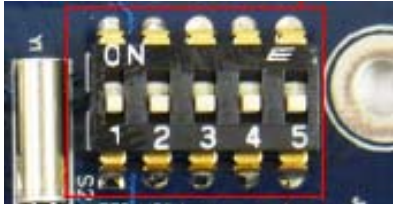
S2[3] is the MSB. S2[5] is the LSB. Set the DIP switch to the ON position for the particular bit to be '1' and OFF position for it to be '0'. For example for setting Logical address of 0X06 (see [Figure](#)).

S2[5] → OFF = 0

S2[4] → ON = 1

S2[3] → ON = 1

DIP Switches for Manual Addressing on the PLC Evaluation Boards



Note that the powerline network protocol supports 8-bit logical addressing, 16-bit extended logical addressing, and 64-bit physical addressing; all of these are supported through software. External host or PSoC microcontroller can talk to the CY8CPLC10 internal memory map to set the appropriate mode and write a particular logical address.

Manual addressing is an easy method to quickly assign a particular address between 0 and 7 to the board, which may be a node in a network.

Note After changing the address of the node, press the RESET button on the PLC LV board for the change to take effect.

2.4.3 Setting Up I²C Address of the Node

S2[1] dip switch is used to assign a specific I²C address to the node to communicate with the external microcontroller/PSoC or USB-I2C bridge. When the S2[1] switch is in OFF position, the address of the node is 0x01 and when the position is ON, the address of the node is 0x7A. For further details on I²C addressing, refer to the data sheet available on the CD.

2.4.4 Jumper Settings for the PLC LV Boards

Figure 2-3. Six Jumpers Available on Board



Table 2-6. Jumper Description

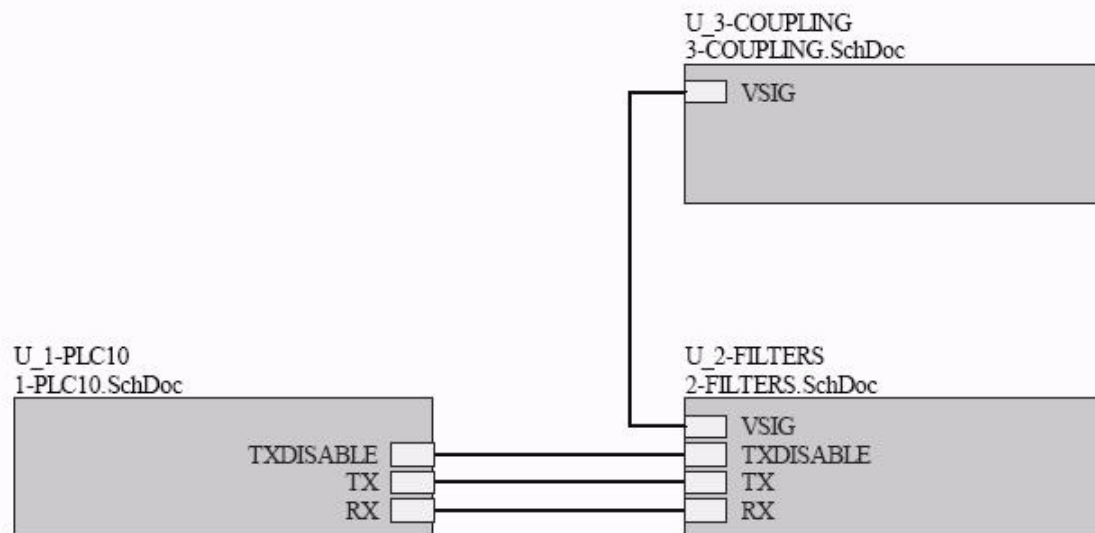
Jumper Name	Use
INT	This is not a jumper. It is a 2-pin header to connect the interrupt pin of the CY8CPLC10 device to an external host. Refer to the CY3273 board schematics to determine interrupt and ground pins for this header.
PWR	This jumper should be connected if the user wants to provide power to an external board. Once this jumper has been connected, power for the external board can be derived from the V (Vdd) and G (Gnd) connectors on the I2C header (J5). For example, if we connect another PSoC EVAL1 board with this board, the PLC board can supply power to that board as well. The CY3272 board can provide a maximum of 50 mA at 5V to an external board through the V and G pins on the I2C header (J5).
RES	This jumper is for enabling Reset of the PLC device through an external board. Once this jumper has been connected, the external board reset can be connected to the R (Reset) pin on the I2C header (J8).
SCL	This is a pull up jumper. While communicating through I2C (J8), one side has to pull up the line. When the jumper is connected, the SCL line will get pulled high. This needs to be done when the user wants the I2C link to be pulled up by the CY3273 board. This jumper does not need to be placed if the USB-I2C bridge is used for communication to the host.
SDA	This is a pull up jumper. While communicating through I2C (J8), one side has to pull up the line. When the jumper is connected, the SDA line will get pulled high. This needs to be done when the user wants the I2C link to be pulled up by the CY3273 board. This jumper does not need to be placed if the USB-I2C bridge is used for communication to the host.
CLK	This jumper is not available for use and should be left unconnected by the user.

A. Appendix

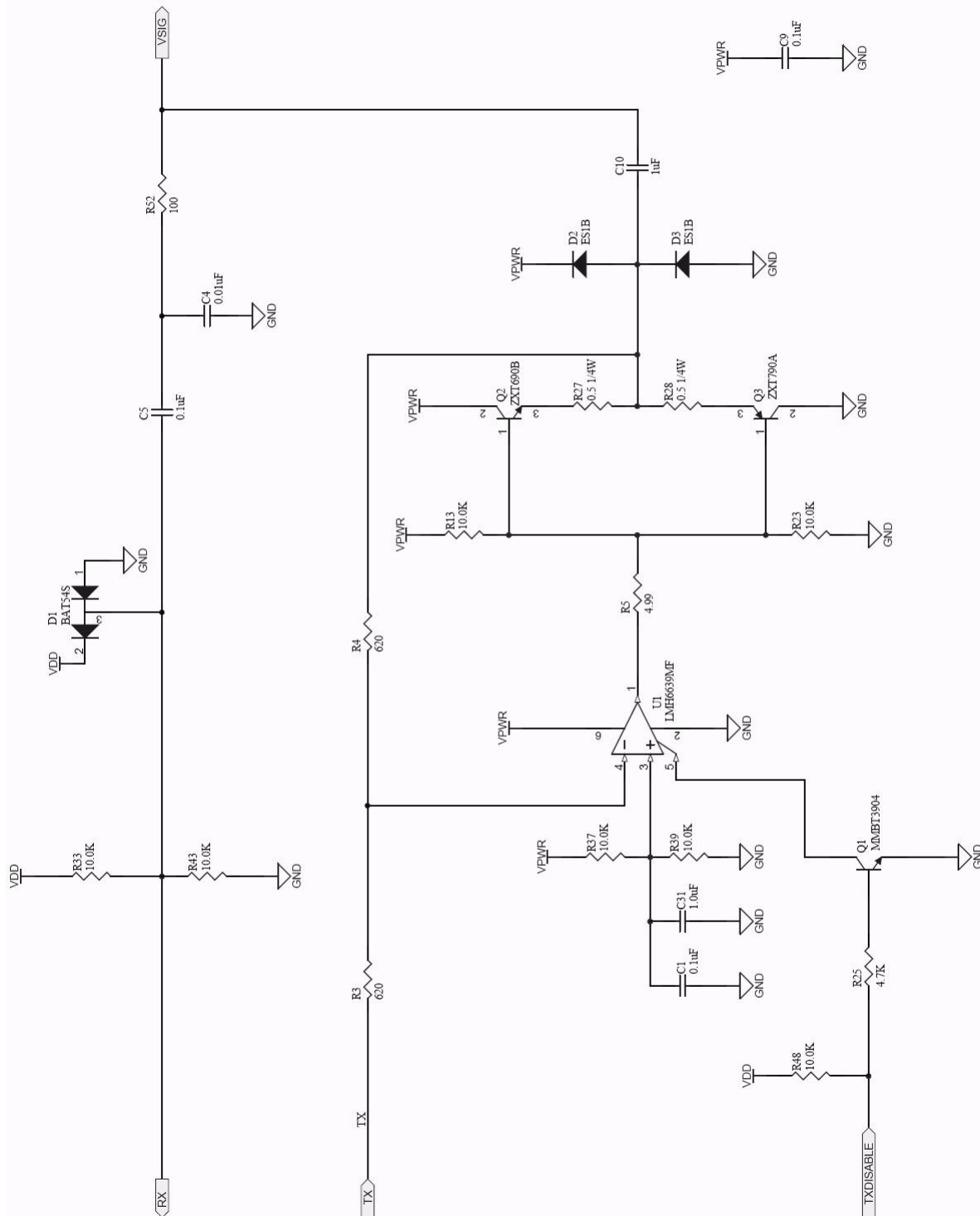


A.1 Schematics

A.1.1 Board Overview

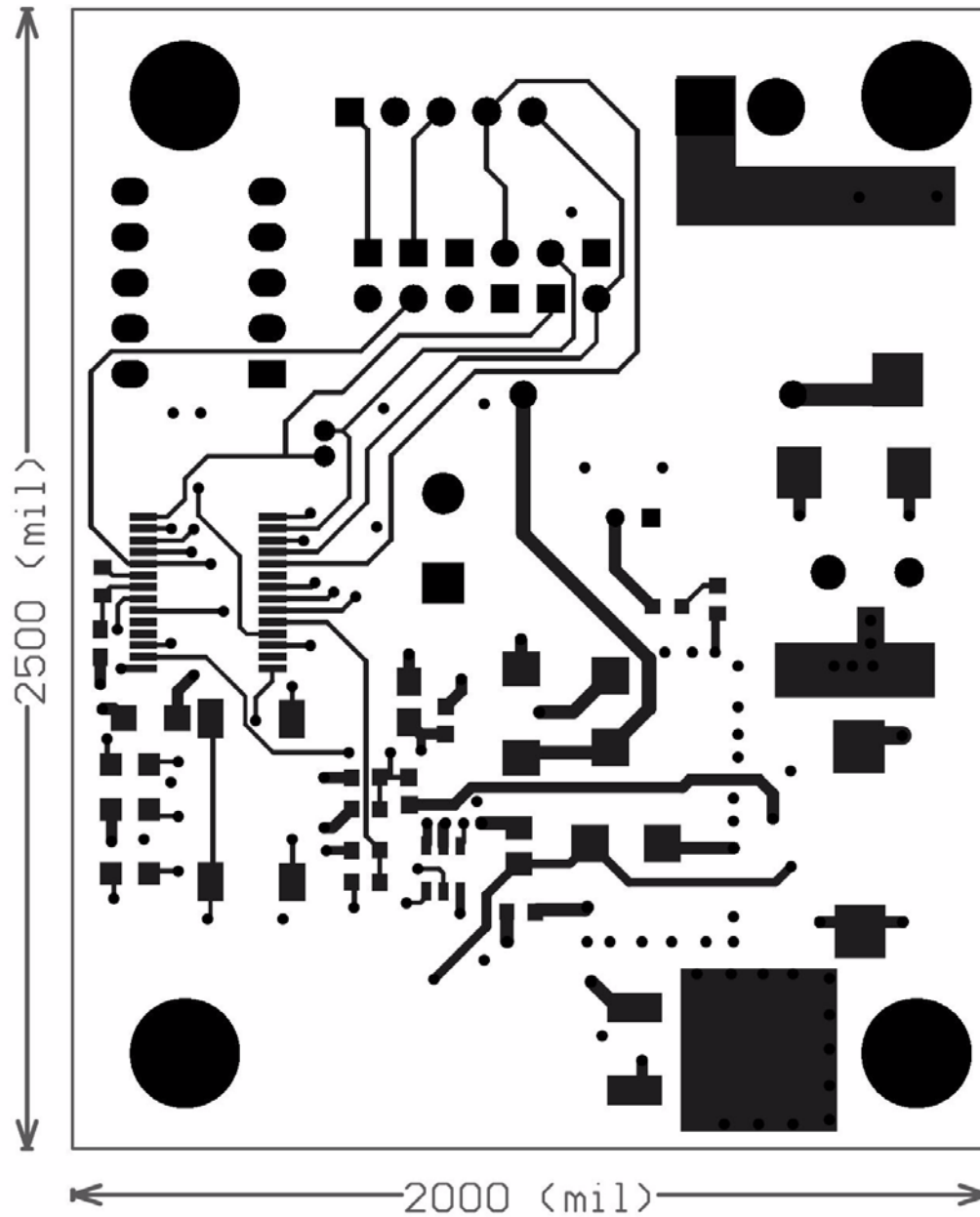


A.1.3 Transmit and Receive Filters

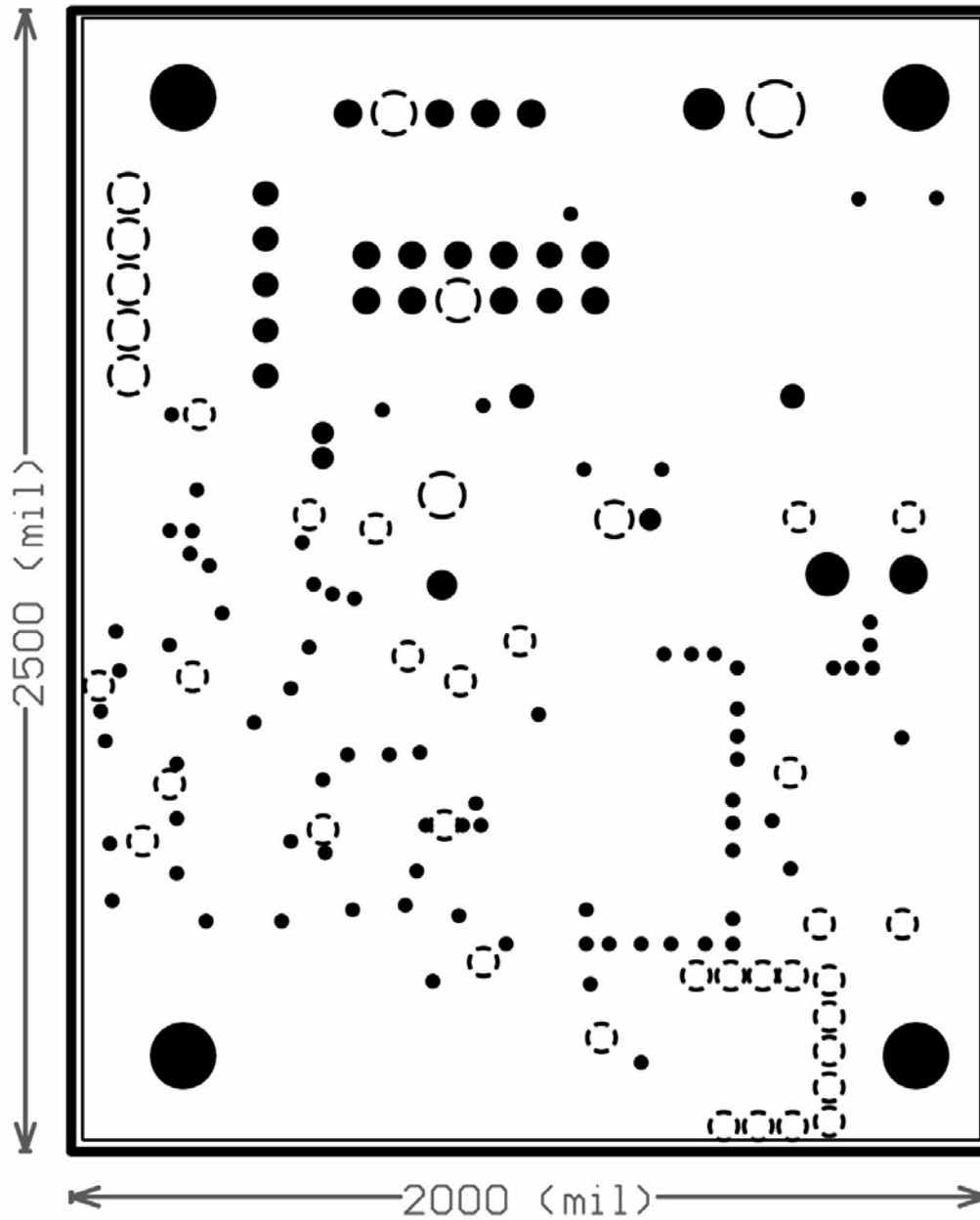


A.2 Layout

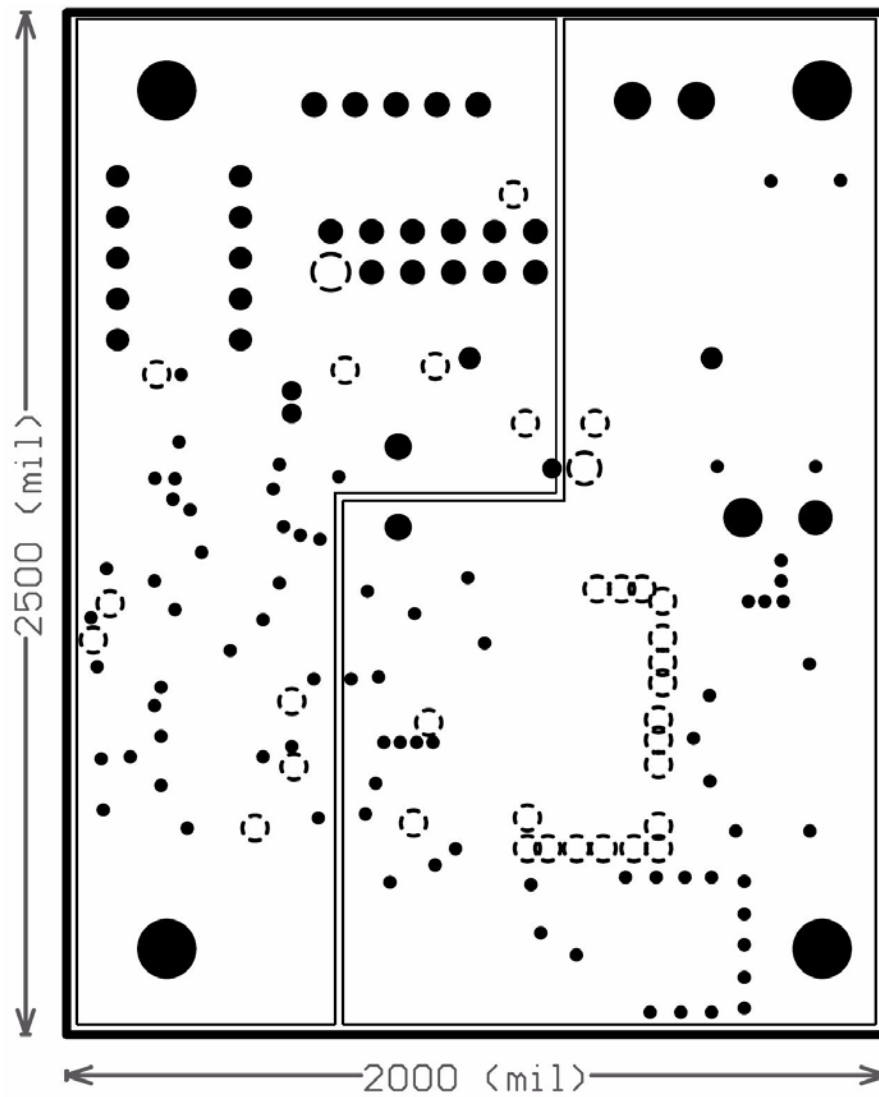
A.2.1 Top Layer



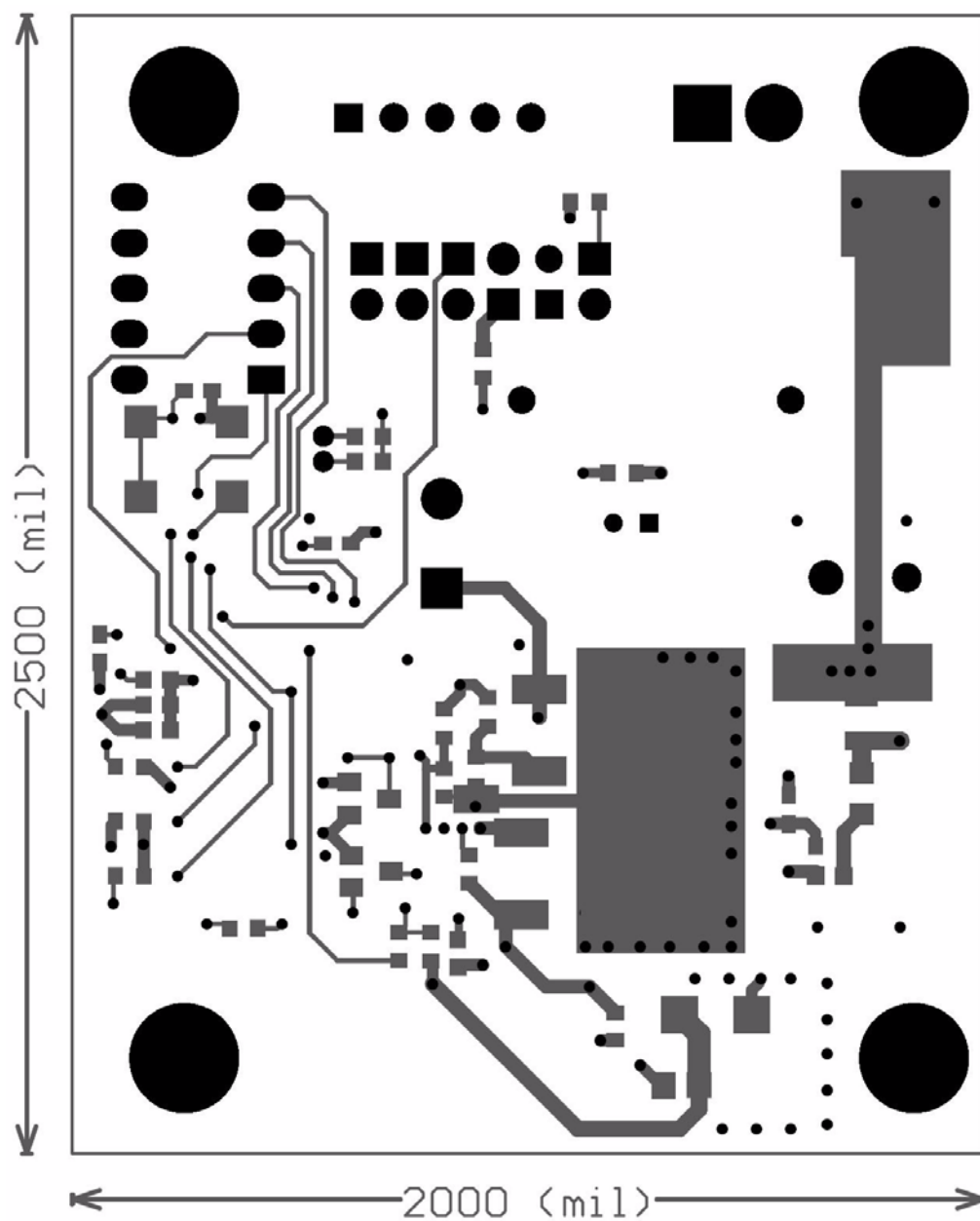
A.2.2 Ground Layer



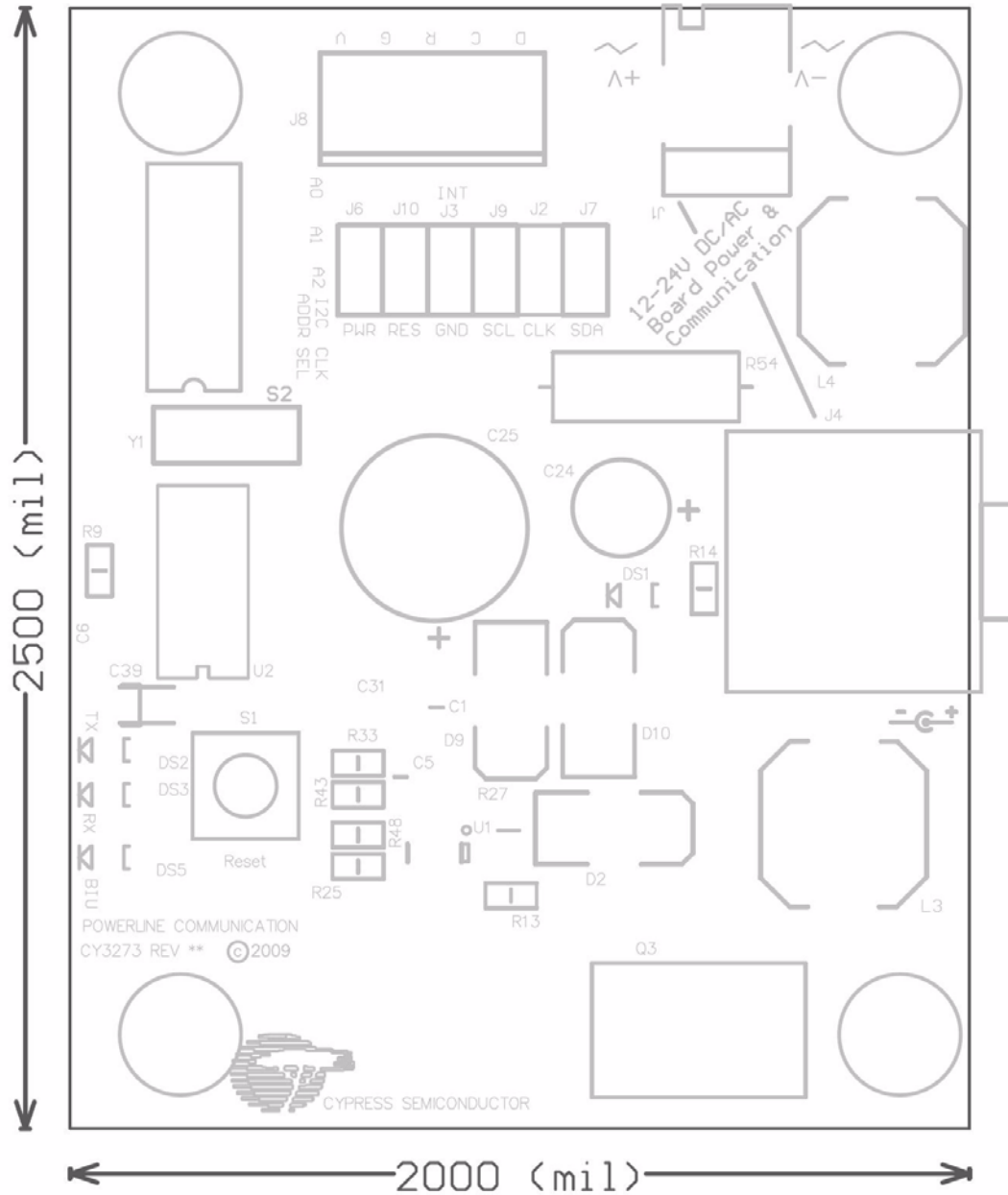
A.2.3 Power Layer



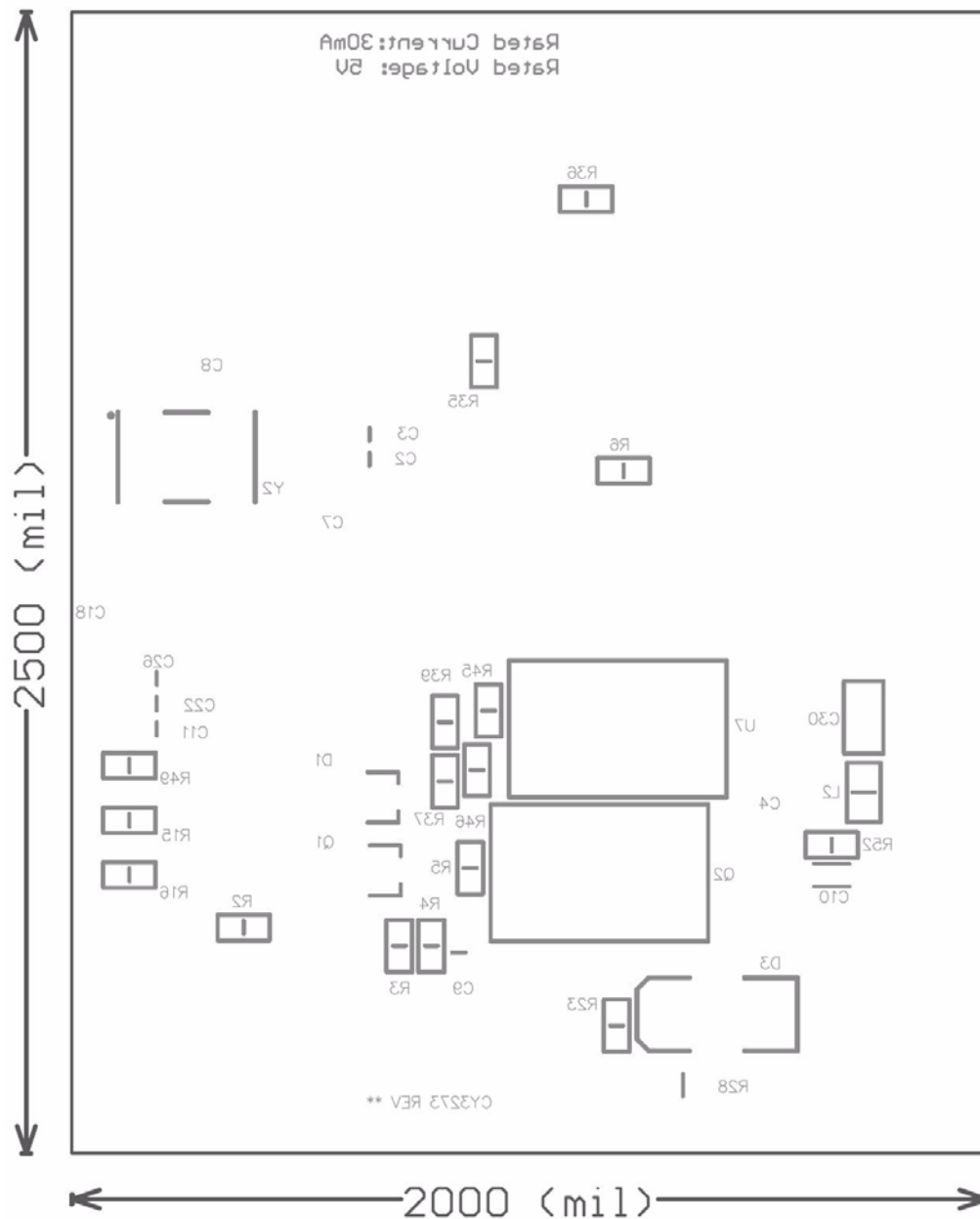
A.2.4 Bottom Layer



A.2.5 Top Silkscreen



A.2.6 Bottom Silkscreen



A.3 Bill of Materials

Description	Designator	Quantity	Value	Manufacturer	Manufacturer Part#	Digi-Key#
CAPACITOR, CERAMIC, .1UF, 25V, 5%, X7R, 0603, SMD	C1, C5, C7, C9, C11	5	.1UF	AVX	06033C104JA T2A	478-3713-1-ND
CAPACITOR, CERAMIC, 22PF, 100V, 5%, C0G, 0603, SMD	C2, C3	2	22PF	MURATA	GRM1885C2A 220JA01D	490-1335-1-ND
CAPACITOR, CERAMIC, .01UF, 25V, 5%, N0G, 0603, SMD	C4, C6, C22	3	.01UF	TDK	C1608C0G1E 103J	445-2664-1-ND
CAPACITOR, CERAMIC, .01UF, 25V X7R 0603	C8	1	0.01uF	AVX	06033C103JA T2A	06033C103J AT2A-ND
CAPACITOR CERAMIC 1UF 16V X7R 0603	C10	1	1UF	PANASONIC	GRM188R71C 105KA12D	490-3900-1-ND
CAPACITOR, CERAMIC, 1.0UF, 25V, 20%, X5S, 0603, SMD	C18	1	1UF	PANASONIC	ECJ-1V41E105M	PCC2354CT-ND
CAP 100UF 10V ALUM ELECTROLYTIC RADIAL	C24	1	100uF	PANASONIC	ECA-1AM101	P5123-ND
CAPACITOR, ELECTROLYTIC, RADIAL, 220UFD, 50VDC, 20%	C25	1	220UF	PANASONIC	ECA-1HM221	P5183-ND
CAPACITOR, CERAMIC, 100PF, 100V, 5%, C0G, 0603, SMD	C26	1	100PF	AVX	06031A101JA T2A	478-1146-1-ND
CAP CER .47UF 50V X7R 1206 T/R	C30	1	0.47UF	TDK	C3216X7R1H4 74K	445-1380-1-ND
CAPACITOR, CERAMIC, 1UF, 50V, 20%, Y5V, 0805, SMD	C31	1	1UF	MURATA	GRM21BF51H 105ZA12L	490-3903-1-ND
Capacitor 10uF,10V	C39	1	10uF, 10V	Vishay	293D106X901 0A2TE3	718-1121-1-ND
DUAL DIODE, W/SERIES CONN., SCHOTTKY, 30V, 300MA	D1	1	BAT54S	STMICRO	BAT54SFILM	497-2522-1-ND
RECTIFIER, ES1B, ULTRAFAST, 100V, 1A	D2, D3, D10	3	ES1B	DIODES INC.	ES1B	ES1B-FDICT-ND
TVS, BI-DIR., 44V, 600W, SMB	D9	1	SMBJ33CA	LITTELFUSE	SMBJ33CA	SMBJ33CAL FCT-ND
LED, BLUE CLEAR, 470NM, 0603 SMD	DS1	1	BLUE	ROHM	SML-E12BC7TT86	511-1589-1-ND
LED, CLEAR GREEN, SMD, 2012 (0805)	DS2	1	GRN	LITE-ON	LTST-C170KGKT	160-1414-1-ND
LED, SUPER RED CLEAR, SMD, 2012 (0805)	DS3	1	RED	LITE-ON	LTST-C170KRKT	160-1415-1-ND
LED, CLEAR YELLOW, SMD, 2012 (0805)	DS5	1	YEL	LITE-ON	LTST-C170KSKT	160-1416-1-ND

Description	Designator	Quantity	Value	Manufacturer	Manufacturer Part#	Digi-Key#
CONN HEADER 2POS 3.96MM VERT TIN	J1	1		MOLEX	09-65-2028	WM18823-ND
HEADER, 2-pin	J2	1	2 POS	SUL-LINS	PEC02SAAN	S1012E-02-ND
HEADER, 2-pin	J3, J6, J7, J9, J10	5	2 POS	SUL-LINS	PEC02SAAN	S1012E-02-ND
POWER JACK, 2.5X5.5MM, MALE, CLOSED, SMD	J4	1	JACK	CUI INC	PJ-002A-SMT	CP-002APJCT-ND
CONN HEADER VERT 5POS .100 TIN	J8	1	5 POS	AMP/TYCO	640456-5	A19471-ND
FERRITE BEAD, EMI FILTER, 100 OHM, 4A, 0805	L2	1	100	TDK	MPZ2012S101A	445-1567-1-ND
INDUCTOR, PWR, 470UH, 20%, DCR=1.460, 0.5A, SMD	L3	1	470UH	PULSE	P0752.474NLT	553-1071-1-ND
INDUCTOR, PWR, 470UH, 20%, DCR=1.460, 0.5A, SMD	L4	1	470UH	PULSE	P0752.474NLT	553-1071-1-ND
MOUNTING HOLES	MT1, MT2, MT3, MT4	4				
NPN, GEN., 40V, .2A, .225W, SOT23	Q1	1	MMBT3904	INFINEON	MMBT3904LT1	MMBT3904LT1INCT-ND
NPN, LO-SAT, 45V, 3A, DPAK	Q2	1	ZXT690BK	ZETEX	ZXT690BKTC	ZXT690BKCT-ND
PNP, LO-SAT, 40V, 3A, DPAK	Q3	1	ZXT790AK	ZETEX	ZXT790AK	ZXT790AKCT-ND
RESISTOR, 330, 1%, 1/10W, 0603 SMD	R2	1	330	YAGEO	RC0603FR-07330RL	311-330HRCT-ND
RESISTOR, 620, 0603, 1%, 1/10W, SMD	R3, R4	2	620	ROHM	MCR03EZPFX6200	RHM620HCT-ND
RESISTOR, 4.99, 0603, 1%, 1/10W, SMD	R5	1	4.99	YAGEO	RC0603FR-074R99L	311-4.99HRCT-ND
RESISTOR, 0.0, 5% , 1/10W, 0603 SMD	R6	1	0.0	ROHM	MCR03EZPJ000	RHM0.0GCT-ND
RESISTOR, 2.1k, 5% , 1/10W, 0603 SMD	R9	1	2.1k	Rohm	MCR03EZPFX2101	RHM2.10KHCT-ND
RESISTOR, 10.0K, 1%, 1/10W, 0603 SMD	R13, R23, R33, R43, R48	5	10K	ROHM	MCR03EZPFX1002	RHM10.0KHCT-ND
RESISTOR, 402, 0603, 1%, 1/10W, SMD	R14	1	402	ROHM	MCR03EZPFX4020	RHM402HCT-ND

Description	Designator	Quantity	Value	Manufacturer	Manufacturer Part#	Digi-Key#
RESISTOR, 1.00K, 1%, 1/10W, 0603 SMD	R15, R16, R49	3	1.00K	ROHM	MCR03EZPFX 1001	RHM1.00KH CT-ND
RESISTOR 4.70K, 1/10W 1% 0603, SMD	R25	1	4.7K	YAGEO	RC0603FR-074K7L	311-4.70KHRCT-ND
RESISTOR, 0.5, 1%, 1/4W, 2012 (0805), SMD	R27, R28	2	0.5	SUS-UMU	RL1220S-R50-F	RL12S.50FCT-ND
RESISTOR, 7.50K, 0603, 1%, 1/10W, SMD	R35, R36	2	7.50K	ROHM	MCR03EZPFX 7501	RHM7.50KH CT-ND
RESISTOR, 10K, 1%, 1/10W, 0603 SMD	R37, R39	2	10K	ROHM	MCR03EZPFX 1002	RHM10.0KH CT-ND
RESISTOR, 715, 1%, 1/10W, 0603 SMD	R45	1	715	ROHM	MCR03EZPFX 7150	RHM715HCT-ND
RESISTOR, 240, 0603, 1%, 1/10W, SMD	R46	1	240	ROHM	MCR03EZPFX 2400	RHM240HCT-ND
RESISTOR, 100.0, 0603, 1%, 1/10W, SMD	R52	1	100	ROHM	MCR03EZPFX 1000	RHM100HCT-ND
RESISTOR, 10 OHM 1W 5% METAL OXIDE	R54	1	10 Ohm, 1W	Stack-pole	RSMF 1 10 5% R	RSMF110JR CT-ND
PUSH BUTTON, NO, LIGHT TOUCH, 6MM, 160G FORCE, SMD	S1	1	N.O.	E-SWITCH	TL3301AF160 QG	EG2526CT-ND
SWITCH DIP LOW PRO 5 POS GOLD	S2	1		E-Switch	KAJ05LAGT	EG4429-ND
OP AMP, R-R W/DISABLE, 190MHZ	U1	1	LM6639	NATIONAL SEMI	LMH6639MF/NOBPB	LMH6639MF CT-ND
CY8CPLC10 Part	U2	1		Cypress	CY8CPLC10-28PVXI	
VOLT REG, ADJUSTABLE 1.2-37V, 1.5A, SMD, DPAK	U7	1	+ADJ	ST MICRO	LM317MDT-TR	497-1574-1-ND
CRYSTAL 32.768KHZ 12.5PF, CYLINDER, SERIES ECS-31X	Y1	1	32.768 KHZ	ECS INC	ECS-3X8X	X1123-ND
OSC 24.000MHZ 5.0V +/-100PPM SMD	Y2	1	24.00 MHz	Crystek	C3290-24.000	C3290-24.000-ND
	Y2 (2nd source)			Citizen	CSX750FCC2 4.000M-UT	300-7214-2-ND

