Integrated Circuit Systems, Inc.

ICS9248-151

Frequency Generator & Integrated Buffers for Celeron & PII/III™

Recommended Application:
VIA Apollo Pro 266 style chipset.

Output Features:

- 3 - CPUs @ 2.5V, up to 200MHz.
- 3 - IOAPIC @ 2.5V, ½ PCI frequency
- 9 - PCI @ 3.3V,
- 1 - 48MHz, @ 3.3V fixed.
- 1 - 24/48MHz @ 3.3V
- 2 - REF @ 3.3V, 14.318MHz.
- 3 - AGP @ 3.3V

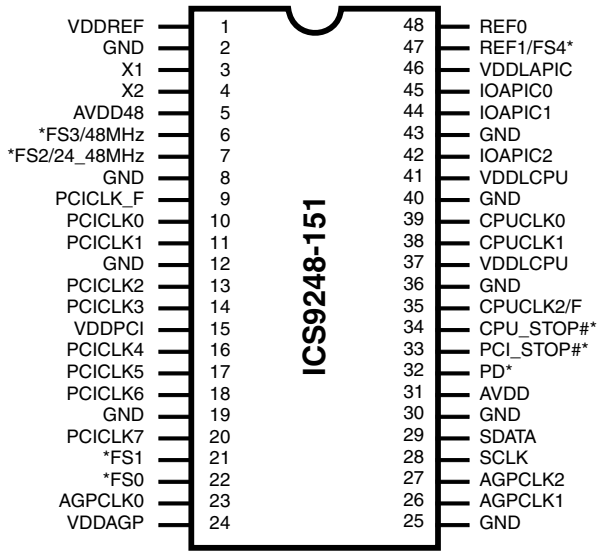
Features:

- Up to 200MHz frequency support
- Support power management: PCI, CPU stop and Power Down.
- Spread spectrum for EMI control (0 to -0.5%, ± 0.25%).
- Uses external 14.318MHz crystal

Skew Specifications:

- CPU – CPU: <175ps
- PCI – PCI: <500ps
- CPU(early)-PCI: Min=1.0ns, Max=2.5ns
- CPU Cycle to cycle jitter: < 250ps

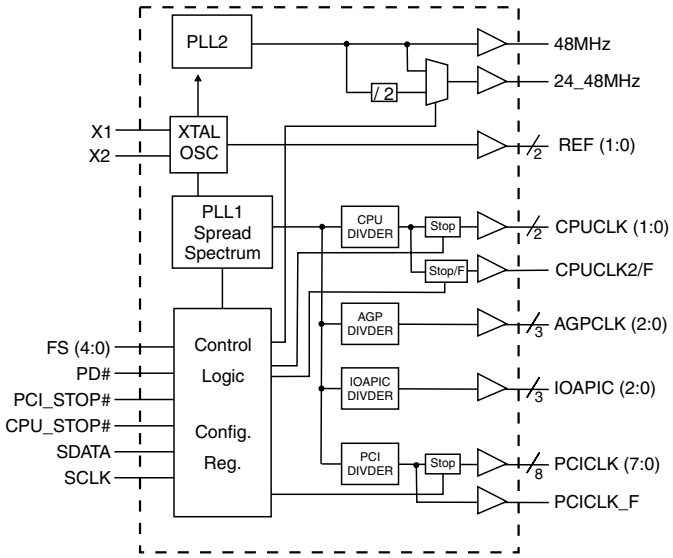
Pin Configuration



48-Pin 300mil SSOP

* Internal Pull-up Resistor of 120K to VDD

Block Diagram



Functionality

FS4	FS3	FS2	FS1	FS0	CPU (MHz)	AGP (MHz)	PCICLK (MHz)
0	0	0	0	0	200.00	80.00	40.00
0	0	0	0	1	190.00	76.00	38.00
0	0	0	1	0	180.00	72.00	36.00
0	0	0	1	1	170.00	68.00	34.00
0	0	1	0	0	166.00	66.40	33.20
0	0	1	0	1	160.00	64.00	32.00
0	0	1	1	0	150.00	75.00	37.50
0	0	1	1	1	145.00	72.50	36.25
0	1	0	0	0	140.00	70.00	35.00
0	1	0	0	1	136.00	68.00	34.00
0	1	0	1	0	130.00	65.00	32.50
0	1	0	1	1	124.00	62.00	31.00
0	1	1	0	0	66.67	66.67	33.34
0	1	1	0	1	100.00	66.67	33.33
0	1	1	1	0	118.00	78.67	39.33
0	1	1	1	1	133.33	66.67	33.34

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
2, 12, 19, 25, 30, 36, 40, 43	GND	PWR	Ground
3	X1	IN	Crystal input, has internal load cap (36pF) and feedback resistor from X2
4	X2	OUT	Crystal output, nominally 14.318MHz. Has internal load cap (36pF)
5	AVDD48MHz	PWR	Power for 24 & 48MHz output buffers and fixed PLL core.
6	FS3	IN	Frequency select pin. Latched Input. Internal Pull-up to VDD
	48MHz	OUT	48MHz output clock
7	FS2	IN	Frequency select pin. Latched Input. Internal Pull-up to VDD
	24_48MHz	OUT	24 or 48MHz output
8	AGND48MHz	PWR	Ground for 24 & 48MHz output buffers and fixed PLL core.
9	PCICLK_F	OUT	Free running PCI clock not affected by PCI_STOP# for power management.
20, 18, 17, 16, 14, 13, 11, 10	PCICLK (7:0)	OUT	PCI clock outputs. Syncheronous to CPU clocks with 1-2ns skew
15	VDDPCI	PWR	Supply for PCICLK_F and PCICLK, nominal 3.3V
21, 22	FS (1:0)[1, 2]	IN	Frequency select pin. Latched Input. Internal Pull-up to VDD
27, 26, 23	AGPCLK (2:0)	OUT	AGP outputs defined as 2X PCI. These may not be stopped.
24	VDDAGP	PWR	Power for AGP clocks
28	SCLK	IN	Clock input of I^2C input, 5V tolerant input
29	SDATA	I/O	Data pin for I^2C circuitry 5V tolerant
31	AVDD	PWR	Power for PLL core 3.3V
32	PD#	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms.
33	PCI_STOP#[1]	IN	Halts PCICLK clocks at logic 0 level, when input low (In mobile mode, MODE=0)
34	CPU_STOP#	IN	This asynchronous input halts CPUCLKs at logic "0" level when driven low.
35	CPUCLK2/F	OUT	CPUCLK either stoppable through CPU_STOP# or free running depending on I^2C selection , 0 = Free Running 1= Stoppable
37, 41	VDDLCPU	PWR	Supply for CPU clocks 2.5V nominal
38, 39	CPUCLK (1:0)	OUT	CPU clock outputs, Low if CPU_STOP#=Low
42, 44, 45	IOAPIC (2:0)	OUT	IOAPIC clock output. 14.318 MHz Powered by VDDLIOAPIC.
46	VDDLAPIC	PWR	Supply for IOAPIC, 2.5V nominal
47	FS4[1, 2]	IN	Frequency select pin. Latched Input
	REF1	OUT	14.318 MHz reference clock.
48	REF0	OUT	14.318 Mhz reference clock.

Notes:

1: Internal Pull-up Resistor of 120K to 3.3V on indicated inputs

2: Bidirectional input/output pins, input logic levels are latched at internal power-on-reset. Use 10Kohm resistor to program logic Hi to VDD or GND for logic low.

General Description

The **ICS9248-151** is a single chip clock solution for Desktop designs. It provides all necessary clock signals for such a system.

Spread spectrum may be enabled through I^2C programming. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The ICS9248-151 employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

Serial programming I^2C interface allows changing functions, stop clock programming and frequency selection.

Power Groups

AVDD, AGND = Core PLL
AVDD48, AGND48 = 24, 48MHz and fixed PLL
VDDREF, GNDREF = REF clocks, Xtal

Serial Configuration Command Bitmap

Byte0: Functionality and Frequency Select Register (default = 0)

Bit	Description										PWD
Bit 2,1 Bit 6:4	Bit 2	Bit 1	Bit 6	Bit 5	Bit 4	CPUCLK	AGPCLK	PCICLK	IOAPIC	Spread	XXXX Note1
	FS4	FS3	FS2	FS1	FS0	(MHz)	(MHz)	(MHz)	(MHz)	Precentage	
	0	0	0	0	0	200.00	80.00	40.00	20.00	+/- 0.25%	
	0	0	0	0	1	190.00	76.00	38.00	19.00	+/- 0.25%	
	0	0	0	1	0	180.00	72.00	36.00	18.00	+/- 0.25%	
	0	0	0	1	1	170.00	68.00	34.00	17.00	+/- 0.25%	
	0	0	1	0	0	166.00	66.40	33.20	16.60	+/- 0.25%	
	0	0	1	0	1	160.00	64.00	32.00	13.00	+/- 0.25%	
	0	0	1	1	0	150.00	75.00	37.50	18.75	+/- 0.25%	
	0	0	1	1	1	145.00	72.50	36.25	18.12	+/- 0.25%	
	0	1	0	0	0	140.00	70.00	35.00	17.50	+/- 0.25%	
	0	1	0	0	1	136.00	68.00	34.00	17.00	+/- 0.25%	
	0	1	0	1	0	130.00	65.00	32.50	16.25	+/- 0.25%	
	0	1	0	1	1	124.00	62.00	31.00	15.50	+/- 0.25%	
	0	1	1	0	0	66.67	66.67	33.34	16.67	+/- 0.75%	
	0	1	1	0	1	100.00	66.67	33.33	16.66	+/- 0.75%	
	0	1	1	1	0	118.00	78.67	39.33	19.66	+/- 0.25%	
	0	1	1	1	1	133.33	66.67	33.34	16.67	+/- 0.75%	
	1	0	0	0	0	66.80	66.80	33.40	16.70	+/- 0.25%	
	1	0	0	0	1	100.20	66.80	33.40	16.70	+/- 0.25%	
	1	0	0	1	0	115.00	76.67	38.33	19.16	+/- 0.25%	
	1	0	0	1	1	133.40	66.70	33.35	16.67	+/- 0.25%	
	1	0	1	0	0	66.80	66.80	33.40	16.67	+/- 0.5%	
	1	0	1	0	1	100.20	66.80	33.40	16.70	+/- 0.5%	
	1	0	1	1	0	110.00	73.33	36.67	18.33	+/- 0.25%	
	1	0	1	1	1	133.40	66.70	33.35	16.67	+/- 0.5%	
	1	1	0	0	0	105.00	70.00	35.00	17.50	+/- 0.25%	
	1	1	0	0	1	90.00	60.00	30.00	15.00	+/- 0.25%	
	1	1	0	1	0	85.00	56.67	28.33	14.16	+/- 0.25%	
	1	1	0	1	1	78.00	78.00	39.00	19.5	+/- 0.25%	
	1	1	1	0	0	66.67	66.67	33.34	16.67	0 to -0.5%	
	1	1	1	0	1	100.00	66.67	33.33	16.66	0 to -0.5%	
	1	1	1	1	0	75.00	75.00	37.50	18.75	+/- 0.25%	
	1	1	1	1	1	133.33	66.67	33.34	16.67	0 to -0.5%	
Bit 3	0 - Frequency is selected by hardware select, Latched Inputs 1 - Frequency is selected by Bit 2, 1 [6:4]										0
Bit 7	0 - Normal 1 - Spread Spectrum Enabled ± 0.25% Center Spread										1
Bit 0	0 - Running 1- Tristate all outputs										0

Note1: Default at power-up will be for latched logic inputs to define frequency, as diplayed by Bit 3.

Byte 1: CPU, Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	35	0	SEL_CPUF#; 0=CPUCLK2 will be free running 1=CPUCLK2 will not be free running
Bit 6	-	1	(Reserved)
Bit 5	-	X	FS4#
Bit 4	-	X	FS3#
Bit 3	35	1	CPUCLK2
Bit 2	38	1	CPUCLK1
Bit 1	39	1	CPUCLK0
Bit 0	42	1	IOAPIC2

Byte 2: PCI, Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	20	1	PCICLK7
Bit 6	18	1	PCICLK6
Bit 5	17	1	PCICLK5
Bit 4	16	1	PCICLK4
Bit 3	14	1	PCICLK3
Bit 2	13	1	PCICLK2
Bit 1	11	1	PCICLK1
Bit 0	10	1	PCICLK0

Byte 3: Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	X	FS2#
Bit 6	-	0	SEL24_48 0=24MHz 1=48MHz
Bit 5	6	1	48MHz
Bit 4	7	1	24_48MHz
Bit 3	9	1	PCICLK_F
Bit 2	27	1	AGPCLK2
Bit 1	26	1	AGPCLK1
Bit 0	23	1	AGPCLK0

Byte 4: Reserved , Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	(Reserved)
Bit 6	-	1	(Reserved)
Bit 5	-	1	(Reserved)
Bit 4	-	1	(Reserved)
Bit 3	-	1	(Reserved)
Bit 2	-	1	(Reserved)
Bit 1	-	1	(Reserved)
Bit 0	-	1	(Reserved)

Byte 5: Peripheral , Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	(Reserved)
Bit 6	-	1	(Reserved)
Bit 5	44	1	IOAPIC1
Bit 4	45	1	IOAPIC0
Bit 3	-	1	(Reserved)
Bit 2	-	1	(Reserved)
Bit 1	47	1	REF1
Bit 0	48	1	REF0

Byte 6: Peripheral , Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit7	-	0	Reserved (Note)
Bit6	-	0	Reserved (Note)
Bit5	-	0	Reserved (Note)
Bit4	-	0	Reserved (Note)
Bit3	-	0	Reserved (Note)
Bit2	-	1	Reserved (Note)
Bit1	-	1	Reserved (Note)
Bit0	-	0	Reserved (Note)

Note: Don't write into this register, writing into this register can cause malfunction

Notes:
1. Inactive means outputs are held LOW and are disabled from switching.
2. Latched Frequency Selects (FS#) will be inverted logic load of the input frequency select pin conditions.

Absolute Maximum Ratings

Supply Voltage ..... 5.5 V
Logic Inputs ..... GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature ..... 0°C to +70°C
Case Temperature ..... 115°C
Storage Temperature ..... –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70º C; Supply Voltage $V_{DD, VDDL}$ = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{DD}$		0.1	5	µA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5	2.0		µA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200	-100		µA
Operating Supply Current	$I_{DD3.3OP66}$	C_L = max Capacitive Loads; Select @ 66 MHz		105	180	mA
	$I_{DD3.3OP100}$	C_L = max Capacitive Loads; Select @ 100 MHz		110		
Power Down Current	$I_{DDPowerDown}$	C_L = max Capacitive Loads; PD#=Low		330	600	µA
Input frequency	F_i	V_{DD} = 3.3 V	12	14.318	16	MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27	36	45	pF
Transition Time[1]	T_{Trans}	To first crossing of target Freq.		0.9	2	ms
Settling Time[1]	T_S	From first crossing to 1% of target Freq.		0.3	3	ms
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.		< 2	3	ms
Skew	$T_{CPU-PCI}$	V_T=1.5 V; V_{TL}=1.25 V; CPU leads	1	1.9	2.5	ns
	$T_{CPU-AGP}$	V_T=1.5 V; V_{TL}=1.25 V	-250	20	+250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70º C; Supply Voltage V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current	$I_{DD2.5OP66}$	C_L = max Capacitive Loads; Select @ 66.65 MHz		19	72	mA
	$I_{DD2.5OP100}$	C_L = max Capacitive Loads; Select @ 100 MHz		25	100	
Skew	$T_{CPU-PCI}$	V_T=1.5 V; V_{TL}=1.25 V; CPU leads	1	1.9	2.5	ns
	$T_{CPU-AGP}$	V_T=1.5 V; V_{TL}=1.25 V	-250	20	+250	ps

Electrical Characteristics - CPUCLK

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2B}[1]	$V_O = V_{DD}*(0.5)$		714		Ω
Output Impedance	R_{DSN2B}[1]	$V_O = V_{DD}*(0.5)$		714		Ω
Output High Voltage	V_{OH2B}	I_{OH} = -8.0 mA	2			V
Output Low Voltage	V_{OL2B}	I_{OL} = 12 mA		0.23	0.4	V
Output High Current	I_{OH2B}	V_{OH} =1.7 V			-16	mA
Output Low Current	I_{OL2B}	V_{OL} = 0.8 V	33	40		mA
Rise Time	t_{r2B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V		0.95	1.6	ns
Fall Time	t_{f2B}[1]	V_{OH} = 2.0 V, V_{OL} = 0.4 V		1	1.6	ns
Duty Cycle	d_{t2B}[1]	V_T = 1.25 V	45	50	55	%
Skew	t_{sk2B}[1]	V_T = 1.25 V		40	175	ps
Jitter, Cycle to cycle	tjcyc-cyc1	V_T = 1.25 V		145	250	ps
Jitter, One Sigma	$t_{j1\sigma2B}$[1]	V_T = 1.25 V		60	150	ps
Jitter, Absolute	t_{jabs2B}[1]	V_T = 1.25 V	-250	160	+250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCICLK

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12	33	55	Ω
Output Impedance	R_{DSN1}[1]	$V_O = V_{DD}*(0.5)$	12	33	55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -11 mA	2.4	3.1		V
Output Low Voltage	V_{OL1}	I_{OL} = 23 mA		0.32	0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V		-72	-22	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	41	55		mA
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.4	2	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.4	2	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45	50	55	%
Skew[1]	t_{sk1}	V_T = 1.5 V		350	500	ps
Jitter, Cycle to cycle	tjcyc-cyc1	V_T = 1.5 V		190	500	ps
Jitter, One Sigma	$t_{j1\sigma2B}$[1]	V_T = 1.5 V		50	150	ps
Jitter, Absolute	t_{jabs2B}[1]	V_T = 1.5 V	-500	140	+500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - IOAPIC

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH2B}	I_{OH} = -8.0 mA	2			V
Output Low Voltage	V_{OL2B}	I_{OL} = 12 mA		0.3	0.4	V
Output High Current	I_{OH2B}	V_{OH} =1.7 V			-16	mA
Output Low Current	I_{OL2B}	V_{OL} = 0.8 V	33	40		mA
Rise Time	t_{r2B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V		1.1	1.6	ns
Fall Time	t_{f2B}[1]	V_{OH} = 2.0 V, V_{OL} = 0.4 V		1.2	1.6	ns
Duty Cycle	d_{t2B}[1]	V_T = 1.25 V	45	49	55	%
Skew	t_{sk2B}[1]	V_T = 1.25 V		215	250	ps
Jitter, Cycle to cycle	tjcyc-cyc1	V_T = 1.25 V		175	500	ps
Jitter, One Sigma	$t_{j1\sigma2B}$[1]	V_T = 1.25 V		100	500	ps
Jitter, Absolute	t_{jabs2B}[1]	V_T = 1.25 V	-500	220	+500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - AGP

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12	33	55	Ω
Output Impedance	R_{DSN1}[1]	$V_O = V_{DD}*(0.5)$	12	33	55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -11 mA	2.4	3.1		V
Output Low Voltage	V_{OL1}	I_{OL} = 23 mA		0.32	0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V		-72	-22	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	41	55		mA
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	1.2	2	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	1.2	2	ns
Duty Cycle[1]	d_{t1}	V_T = 1.4 V, CPU @ 100MHz	45	50	55	%
Skew	t_{sk1}	V_T = 1.5 V		60	175	ps
Jitter, Cycle to cycle	tjcyc-cyc1	V_T = 1.5 V		120	300	ps
Jitter, One Sigma	$t_{j1\sigma2B}$[1]	V_T = 1.5 V		30	150	ps
Jitter, Absolute	t_{jabs2B}[1]	V_T = 1.5 V	-250	90	+250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF, 24MHz, 48MHz

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	20	48	60	Ω
Output High Voltage	V_{OH5}	I_{OH} = -12 mA	2.4	3		V
Output Low Voltage	V_{OL5}	I_{OL} = 10 mA		0.26	0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V		-42	-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16	31		mA
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V; **REF**		1.3	4	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V; **REF**		1.5	4	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V; **REF**	45	53	55	%
Rise Time[1]	t_{r5}	VOL = 0.4 V, VOH = 2.4 V; **48MHz**		1.3	4	ns
Fall Time[1]	t_{f5}	VOH = 2.4 V, VOL = 0.4 V; **48MHz**		1.6	4	ns
Duty Cycle[1]	d_{t5}	VT = 1.5 V; **48MHz**	45	51	55	%
Rise Time[1]	t_{r5}	VOL = 0.4 V, VOH = 2.4 V; **24MHz**		1.5	4	ns
Fall Time[1]	t_{f5}	VOH = 2.4 V, VOL = 0.4 V; **24MHz**		1.6	4	ns
Duty Cycle[1]	d_{t5}	VT = 1.5 V; **24MHz**	45	50	55	%
Jitter, Cycle to cycle	$t_{jcyc-cyc5}$	V_T = 1.5 V; **REF**		460	1000	ps
Jitter, One Sigma	t_{j1s5}	V_T = 1.5 V; **REF**		120	500	ps
Jitter, Absolute	t_{jabs5}	V_T = 1.5 V; **REF**	-1000	340	+1000	ps
Jitter, Cycle to cycle	$t_{jcyc-cyc5}$	V_T = 1.5 V; **24, 48MHz**		250	500	ps
Jitter, One Sigma	t_{j1s5}	V_T = 1.5 V; **24, 48MHz**		75	250	ps
Jitter, Absolute	t_{jabs5}	V_T = 1.5 V; **24, 48MHz**	-500	200	+500	ps

[1]Guaranteed by design, not 100% tested in production.

General I²C serial interface information

The information in this section assumes familiarity with I²C programming.
For more information, contact ICS for an I²C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D2(H)	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Stop Bit	

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 5***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

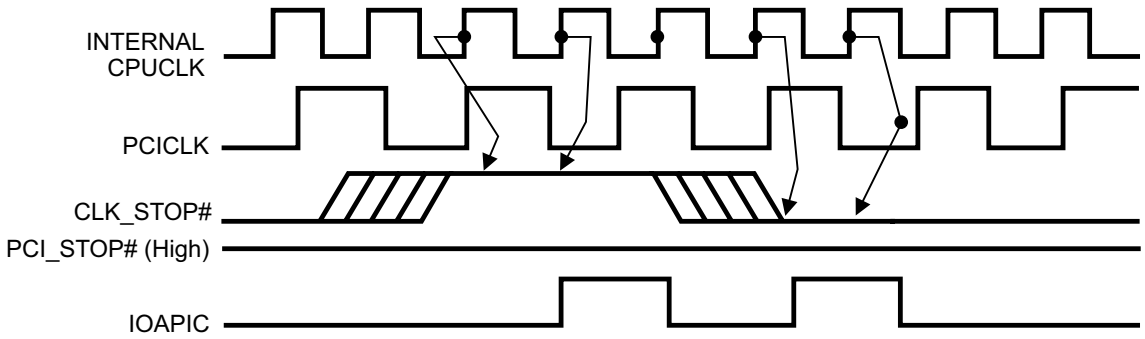
How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D3(H)	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

CLK_STOP# Timing Diagram

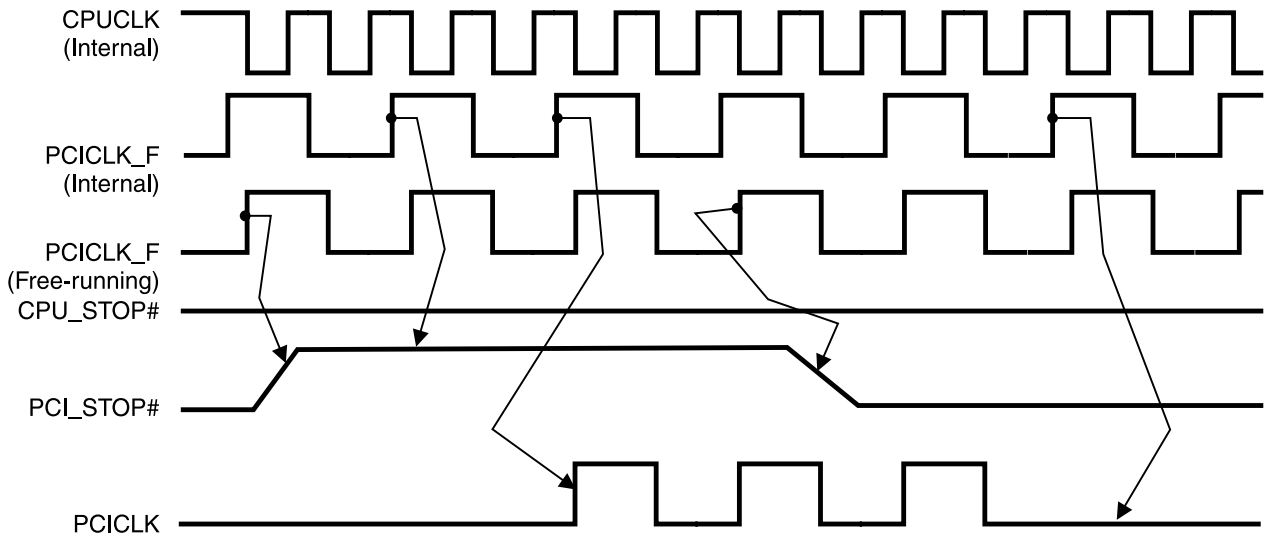
CLK_STOP# is an asychronous input to the clock synthesizer. It is used to turn off the CPU clocks for low power operation. CLK_STOP# is synchronized by the **ICS9248-151**. The minimum that the CPU clock is enabled (CLK_STOP# high pulse) is 100 CPU clocks. All other clocks will continue to run while the CPU clocks are disabled. The CPU clocks will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPU clock on latency is less than 4 CPU clocks and CPU clock off latency is less than 4 CPU clocks.



Notes:
1. All timing is referenced to the internal CPU clock.
2. CLK_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPU clocks inside the ICS9248-151.
3. IOAPIC output is Stopped Glitch Free by CLK_STOP# going low.
4. SDRAM-F output is controlled by Buffer in signal, not affected by the **ICS9248-151** CLK_STOP# signal. SDRAM's are controlled as shown.
5. All other clocks continue to run undisturbed.

PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the **ICS9248-151**. It is used to turn off the PCICLK clocks for low power operation. PCI_STOP# is synchronized by the **ICS9248-151** internally. The minimum that the PCICLK clocks are enabled (PCI_STOP# high pulse) is at least 10 PCICLK clocks. PCICLK clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.



Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248-151 device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS9248-151.
3. All other clocks continue to run undisturbed.
4. CPU_STOP# is shown in a high (true) state.

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the ICS9248-151 serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

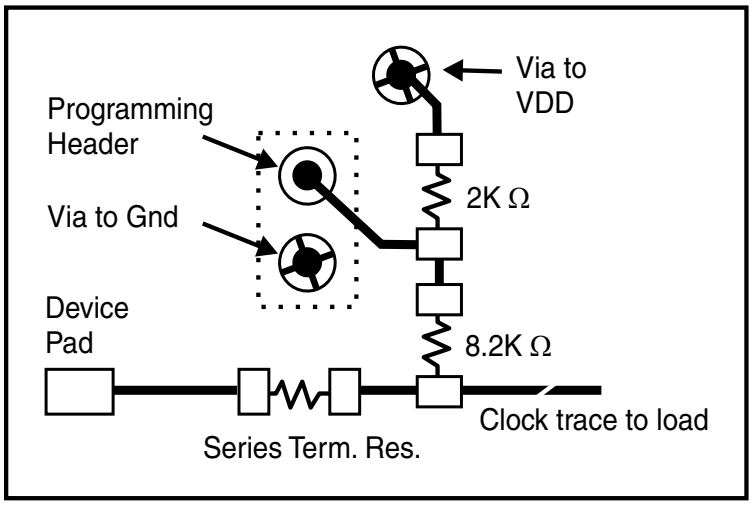
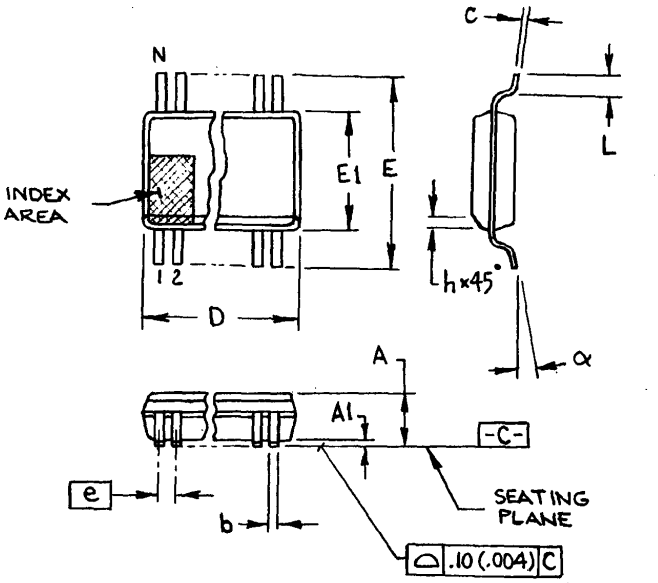


Fig. 1



300 mil SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.413	2.794	.095	.110
A1	0.203	0.406	.008	.016
b	0.203	0.343	.008	.0135
c	0.127	0.254	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.033	10.668	.395	.420
E1	7.391	7.595	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.381	0.635	.015	.025
L	0.508	1.016	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
28	9.398	9.652	.370	.380
34	11.303	11.557	.445	.455
48	15.748	16.002	.620	.630
56	18.288	18.542	.720	.730
64	20.828	21.082	.820	.830

Ordering Information

ICS9248yF-151-T

Example:

ICS XXXX y F - PPP - T

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F=SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device