NCP5010

500 mW Boost Converter for White LEDs

The NCP5010 is a fixed frequency PWM boost converter with integrated rectification optimized for constant current applications such as driving white LEDs. This device features small size, minimal external components and high−efficiency for use in portable applications and is capable of providing up to 500 mW output power to 2−5 series connected white LEDs. A single resistor sets the LED current and the CTRL pin can be pulse width modulated (PWM) to reduce the LED Current.

The device includes True−Cutoff circuitry to disconnect the load from the battery when the device is put into standby mode. To protect the device, an output overvoltage protection, and short circuit protection have been incorporated. The NCP5010 is housed in a low profile, space efficient 1.7 x 1.7 mm Flip−Chip package. The device has been optimized for use with small inductors and ceramic capacitors.

Features

- 2.7 to 5.5 V Input Voltage Range
- Efficiency: 84% for 5 LED (V_F = 3.5 V by LED) at 30 mA and 4.2 V V_{IN}
- Low Noise 1 MHz PWM DC−DC Converter
- Open LED Protection and Short Circuit Protection
- Serial LEDs Architecture for Uniform Current Matching
- 1 μA Shutdown Current Facility with True−Cutoff
- Very Small 8−Pin Flip−Chip 1.7 x 1.7 mm Package
- This is a Pb−Free Device

Typical Applications

- White LED Backlighting for Small Color LCD Displays
- Cellular Phones
- Digital Cameras
- MP3 Players
- High Efficiency Step−up Converter

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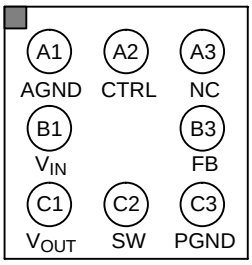
MARKING DIAGRAM

1

8−Pin Flip−Chip
FC SUFFIX
CASE 499AJ

DAX = Specific Device Code
▪ = Pb−Free Package
A = Assembly Location
Y = Year
WW = Work Week

PIN CONNECTIONS



Top View

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 16 of this data sheet.

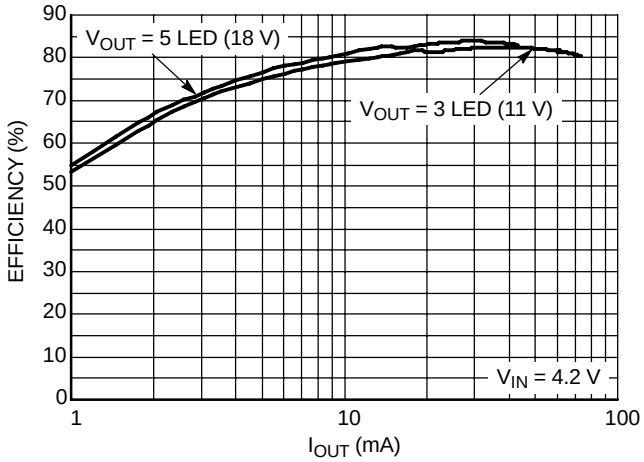


Figure 1. Efficiency vs. Output Current

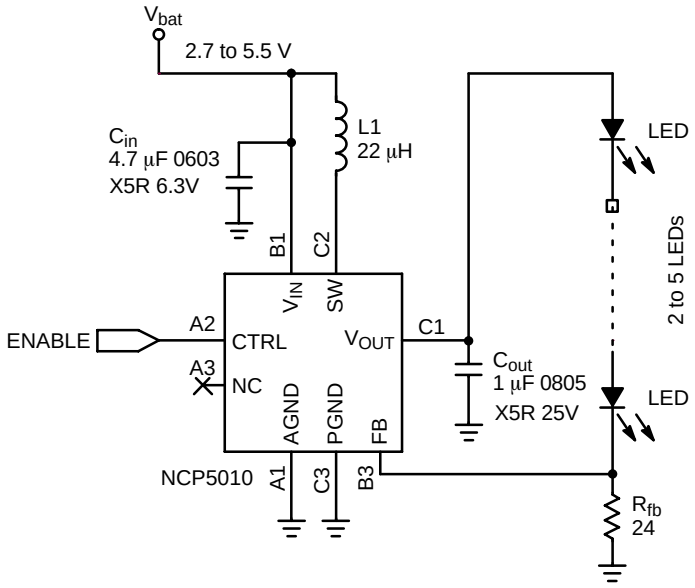


Figure 2. Typical Application Circuit

PIN FUNCTION DESCRIPTION

PIN	PIN NAME	TYPE	DESCRIPTION
A1	AGND	POWER	System ground for the analog circuitry. A high quality ground must be provided to avoid spikes and/or uncontrolled operations. This pin is to be connected to the PGND pin.
B1	V_{IN}	POWER	Power Supply Input. A ceramic capacitor with a minimum value of 1 μF/6.3 V (X5R or X7R) must be connected to this pin. This capacitor should be placed as close as possible to this pin. In addition, one end of the external inductor is to be connected at this point.
C1	V_{OUT}	POWER	DC−DC converter output. This pin should be directly connected to the load and a low ESR (<30 mΩ) 1 μF (min) 25 V bypass capacitor. This capacitor is required to smooth the current flowing into the load, thus limiting the noise created by the fast transients present in this circuit. Since this is a current regulated output, this pin has over voltage protection to protect from open load conditions. Care must be taken to avoid EMI through the PCB copper tracks connected to this pin.
A2	CTRL	INPUT	An Active High logic level on this pin enables the device. A built−in pulldown resistor disables the device if the pin is left open. This pin can also be used to control the average current into the load by applying a low frequency PWM signal. If a PWM signal is applied, the frequency should be high enough to avoid optical flicker but be no greater than 1 kHz.
C2	SW	POWER	Power switch connection for inductor. Typical application will use a coil from 10 μH to 22 μH and must be able to handle at least 350 mA. If the desired output power is above 300 mW, the inductor should have a DCR < 1.4 Ω.
A3	NC	N/A	Not Connected
B3	FB	INPUT	Feedback voltage input used to close the loop by means of a sense resistor connected between the primary LED branch and the ground. The output current tolerance is depends upon the accuracy of this resistor and a ±5% or better accuracy metal film resistor is recommended. An analog dimming signal can be applied to this point to reduce the output current. Please refer to the application section for additional details.
C3	PGND	POWER	Power ground. A high quality ground must be used to avoid spikes and/or uncontrolled operation. Care must be taken to avoid high−density current flow in a limited PCB copper track. This pin is to be connected to the AGND pin.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (Note 2)	V_{IN}	7.0	V
Over Voltage Protection	V_{OUT}	24	V
Human Body Model (HBM) ESD Rating (Note 3)	ESD HBM	2000	V
Machine Model (MM) ESD Rating (Note 3)	ESD MM	200	V
Digital Input Voltage Digital Input Current	CTRL	$-0.3 < V_{IN} < V_{bat}+0.3$ 1.0	V mA
Power Dissipation @ T_A = +85 °C	P_D	150	mW
Thermal Resistance Junction−to−Air 8−Pin Flip−Chip Package	$R_{\theta JA}$	(Note 6)	°C/W
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Operating Junction Temperature Range	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Maximum electrical ratings are defined as those values beyond which damage to the device may occur at T_A = 25°C.
2. According to JEDEC standard JESD22−A108B.
3. This device series contains ESD protection and passes the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22−A114 for all pins.
   Machine Model (MM) ±200 V per JEDEC standard: JESD22−A115 for all pins.
4. Latchup Current Maximum Rating: ±100 mA per JEDEC standard: JESD78.
5. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.
6. For the 8−Pin Flip−Chip CSP Package, the $R_{\theta JA}$ is highly dependent on the PCB Heatsink area. For example $R_{\theta JA}$ can be to 195°C/W with 50 mm total area and also 135°C/W with 500 mm. All the bumps have the same thermal resistance and need to be connected thereby optimizing the power dissipation.

ELECTRICAL CHARACTERISTICS (Limits apply for T_A between −40°C to +85°C and V_{IN} = 3.6 V, unless otherwise noted)

Pin	Symbol	Rating	Min	Typ	Max	Unit
B1	V_{IN}	Supply Voltage	2.7		5.5	V
C2	I_{PEAK_MAX}	Switch Current Limit	280	420	560	mA
	NMOS $R_{DS(on)}$	Internal Switch On Resistor		0.6	1.0	Ω
	F_{OSC}	PWM Oscillator Frequency	0.8	1.0	1.2	MHz
	M_{DUTY}	Maximum Duty Cycle	91	95		%
	E_{FF}	Efficiency (Note 7)		84		%
C1	OVP_{ON}	Overvoltage Clamp Voltage	20	22		V
C1	OVP_H	Overvoltage Clamp Hysteresis		1.0		V
C1	P_{OUT}	Output power (Note 8) V_{IN} = 3.1 V V_{IN} < 3.1 V	 500 300			mW
C1	I_{OUT}	Minimum Output Current Controlled No Skip Mode (Note 9)		1.0		mA
B3	F_{BV}	Feedback Voltage Threshold in Steady State Overtemperature range At 25°C	 475 490	 500 500	 525 510	mV
C1	F_{BVLR}	Feedback Voltage Line Regulation (Notes 9 and 10) From DC to 100 Hz		 0.2	 0.5	%/V
B1	U_{VLO}	V_{IN} Undervoltage Lockout measured at 25°C Threshold to Enable the Converter Threshold to Disable the Converter	 2.2 2.0	 2.4 2.2	 2.6 2.4	V
B1	U_{VLOH}	Undervoltage Lockout Hysteresis		200		mV
C1	I_{OUTSC}	Short Circuit Output Current		20		mA
B1	S_{CPT}	Short Circuit Protection Threshold Detected Released	 35 47	 50 67	 65 87	% of V_{IN}
B1 C2	ISTDB	Stand by Current, I_{OUT} = 0 mA, CTRL = Low V_{bat} = 4.2 V			2.0	μA
	I_Q	Quiescent Current Device Not Switching (BF = VIN) Device Switching (R_{FB} disconnected)		 0.4 1.0		mA
A2	V_{IL}	Voltage Input Logic Low			0.3	V
A2	V_{IH}	Voltage Input Logic High	1.2			V
A2	R_{CTRL}	CTRL Pin Pulldown Resistance	175		370	kΩ

7. Efficiency is defined by 100 * (P_{out} / P_{in}) at 25°C
   V_{IN} = 4.2 V with L= Coilcraft DT1608C−223
   I_{OUT} = 30 mA, Load = 5 LEDs (V_F = 3.5 V per LED) bypassed by 1 μF X5R
8. Guaranteed by design and characterized with L = 22 μH, DCR = 0.7 Ω max.
9. Load = 4 LEDs (V_F = 3.5 V by LED), C_{OUT} = 1 μF X5R, L= Coilcraft DT1608C−223.
10. V_{IN} = 3.6 V, Ripple = 0.2 V P−P, I_{OUT} = 15 mA.

TYPICAL OPERATING CHARACTERISTICS

Condition: Efficiency = 100 x (Number of LED stacked x V_{LED} x I_{LED})/P_{IN}

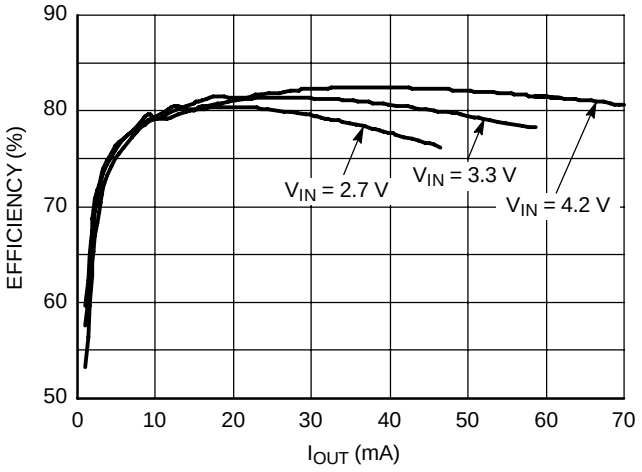


Figure 3. Efficiency vs. Current @ 3 LEDS (10.5 V)
L = Coilcraft DT1608C−223

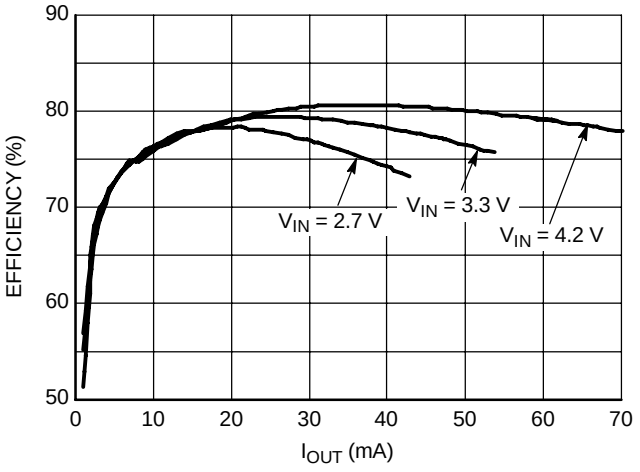


Figure 4. Efficiency vs. Current @ 3 LEDS (10.5 V)
L = TDK VLF4012AT−220

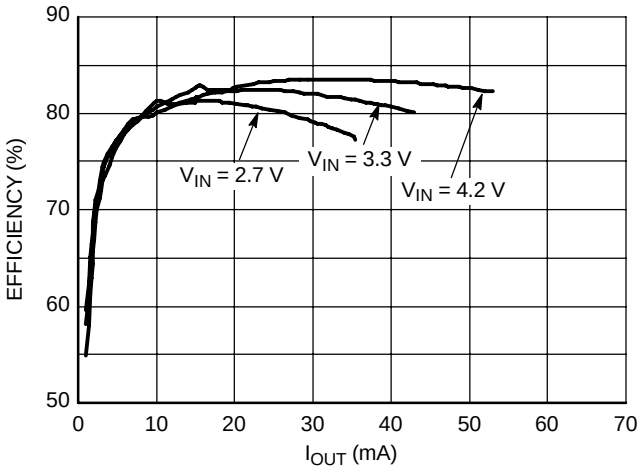


Figure 5. Efficiency vs. Current @ 4 LEDS (14 V)
L = Coilcraft DT1608C−223

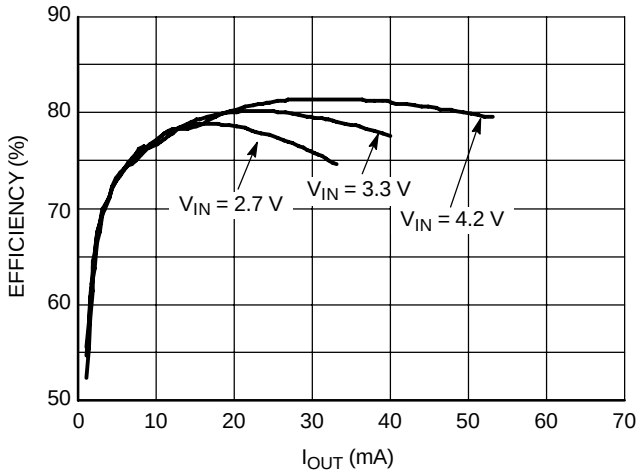


Figure 6. Efficiency vs. Current @ 4 LEDS (14 V)
L = TDK VLF4012AT−220

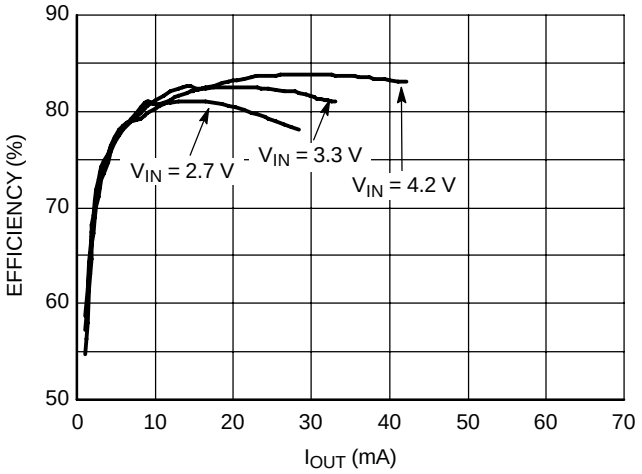


Figure 7. Efficiency vs. Current @ 5 LEDS (17.5 V)
L = Coilcraft DT1608C−223

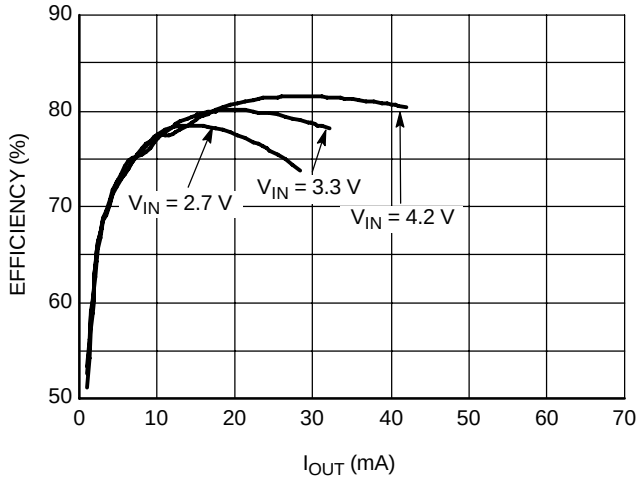


Figure 8. Efficiency vs. Current @ 5 LEDS (17.5 V)
L = TDK VLF4012AT−220

TYPICAL OPERATING CHARACTERISTICS

Condition: Efficiency = 100 x (Number of LED stacked x V_{LED} x I_{LED})/P_{IN}

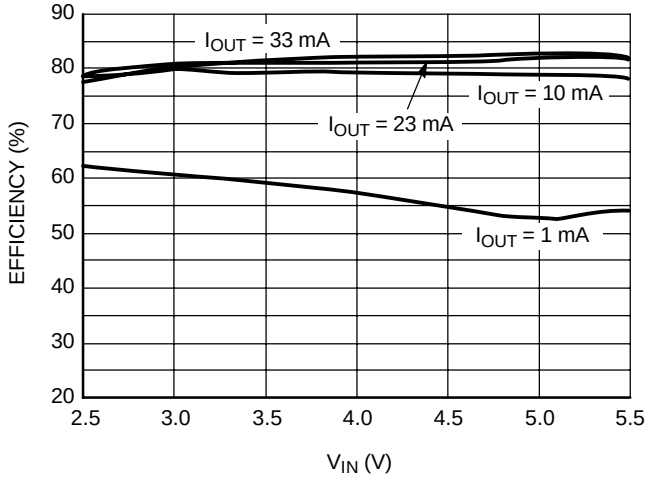


Figure 9. Efficiency vs. V_{IN} @ 3 LEDS (10.5 V)
L = Coilcraft DT1608C−223

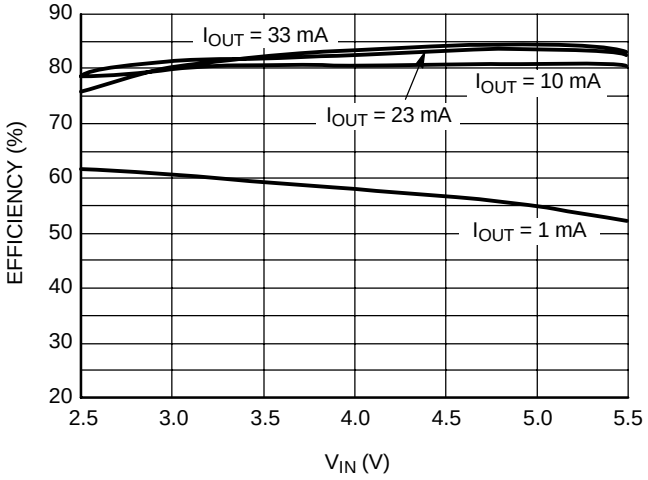


Figure 10. Efficiency vs. V_{IN} @ 4 LEDS (14 V)
L = Coilcraft DT1608C−223

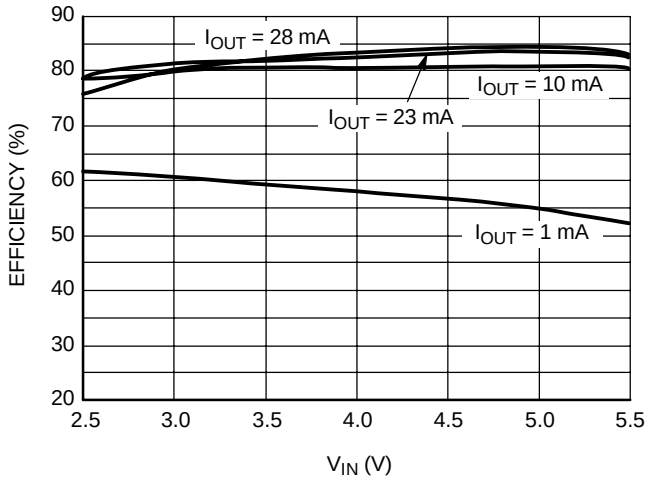


Figure 11. Efficiency vs. V_{IN} @ 5 LEDS (17.5 V)
L = Coilcraft DT1608C−223

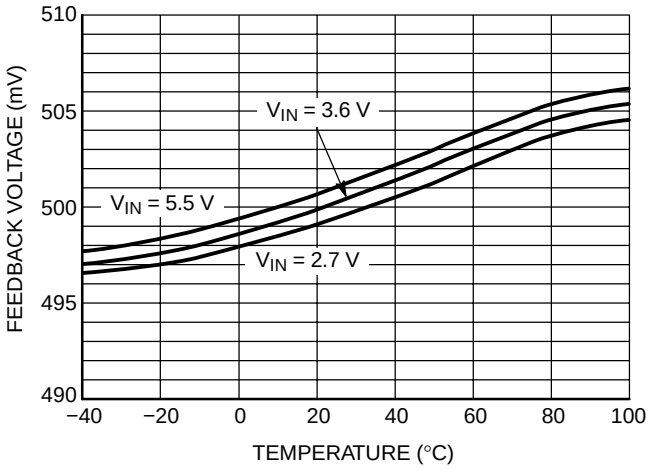


Figure 12. Feedback Voltage vs. Temperature

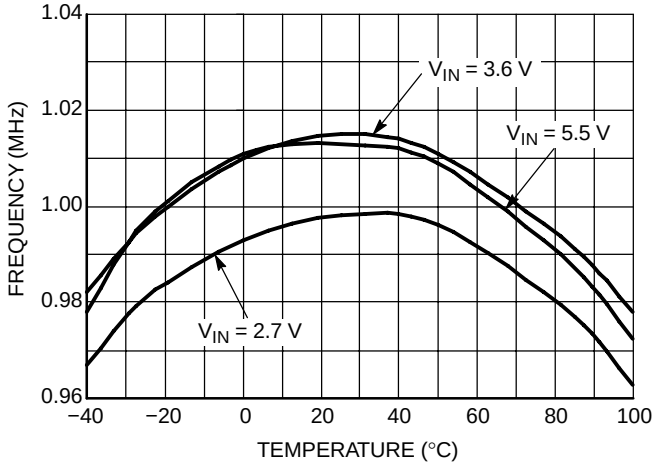


Figure 13. Oscillator Frequency vs. Temperature

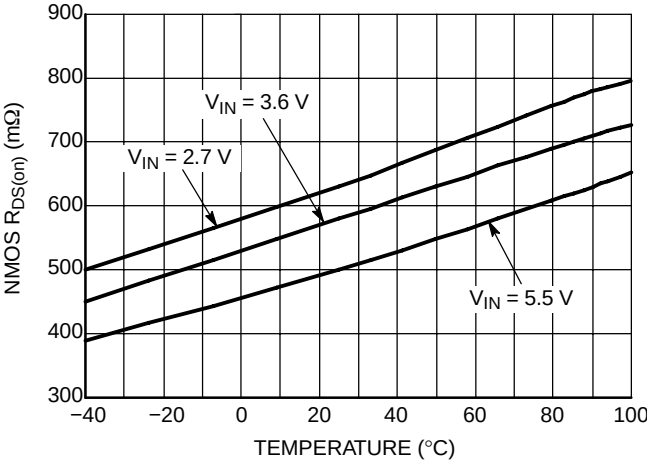


Figure 14. NMOS $R_{DS(on)}$ vs. Temperature

TYPICAL OPERATING CHARACTERISTICS

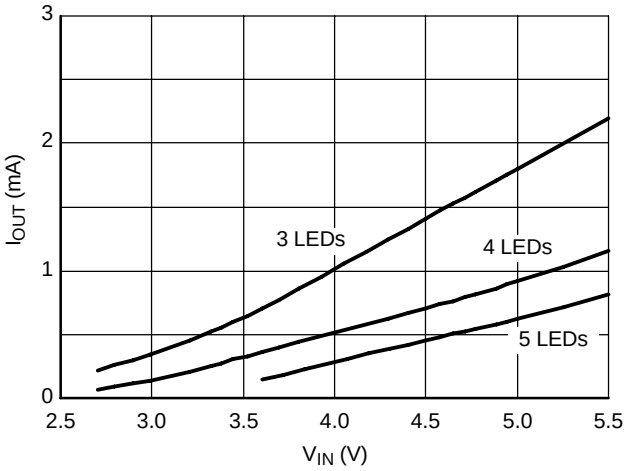


Figure 15. Typical Skip Mode Threshold vs. V_{IN} (C_{OUT} = 1 μF X5R 25 V)

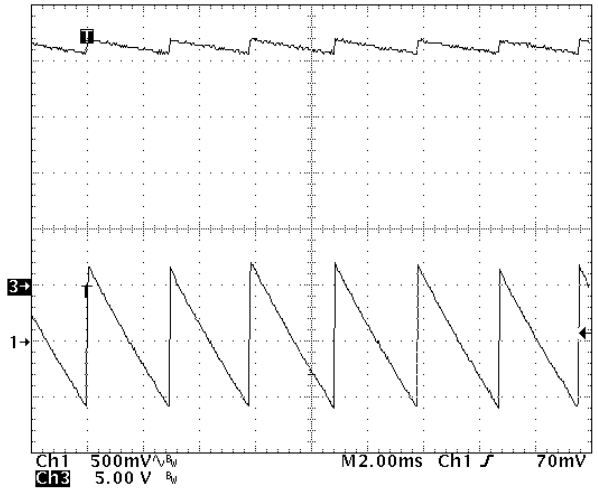


Figure 16. Typical V_{OUT} Ripple in OVP Conditions 1 V_{OUT}, 500 mV/div, AC 3 V_{OUT}, 5 V/div, DC

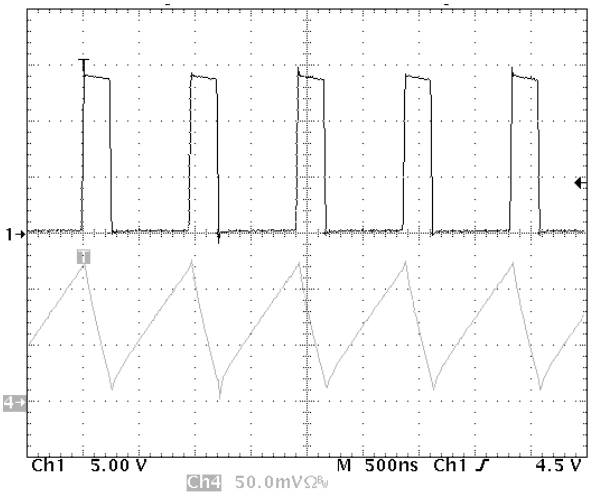


Figure 17. Continuous Current Mode (CCM) 1 SW, 5 V/div DC, 4 I_{SW}, 50 mA/div, DC, I_{OUT} = 15 mA

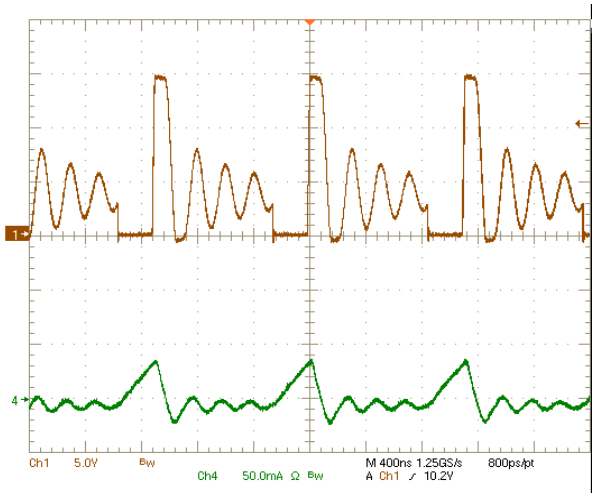


Figure 18. Discontinuous Current Mode (DCM) 1 SW, 5 V/div DC, 4 I_{SW}, 50 mA/div, DC, I_{OUT} = 1 mA

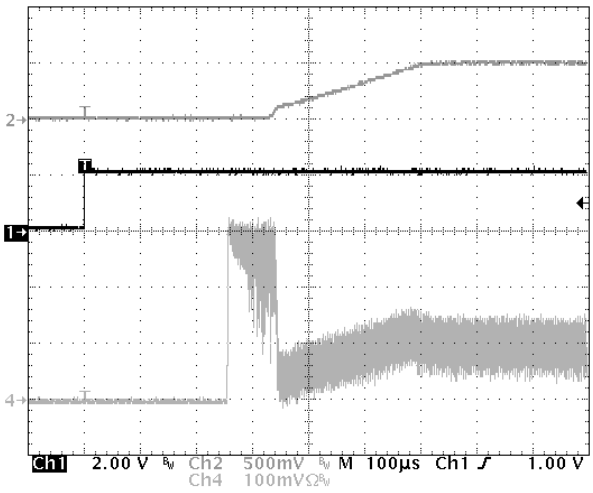


Figure 19. Startup for LED Operating, 4 LEDS R_{BF} = 22 Ω, 1 CTRL, 2 V/div DC, 2 FB, 500 mV/div DC, 4 I_L 100 mA/div, T = 100 μs/div

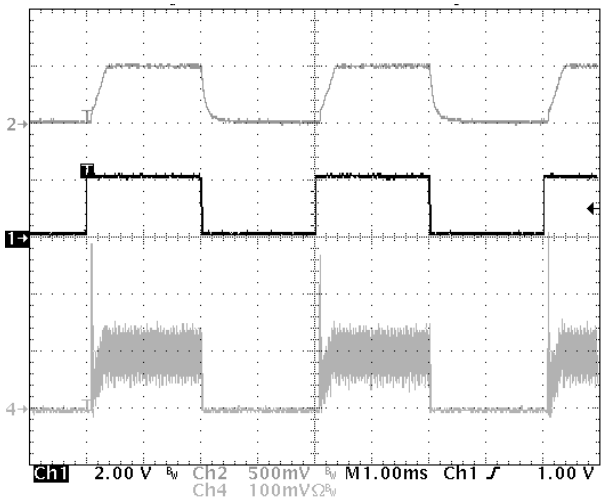


Figure 20. Duty Cycle Control Waveforms 1 CTRL, 2 V/div DC, 2 FB, 500 mV/div DC, 4 I_L 100 mA/div, T = 1 ms/div

TYPICAL OPERATING CHARACTERISTICS

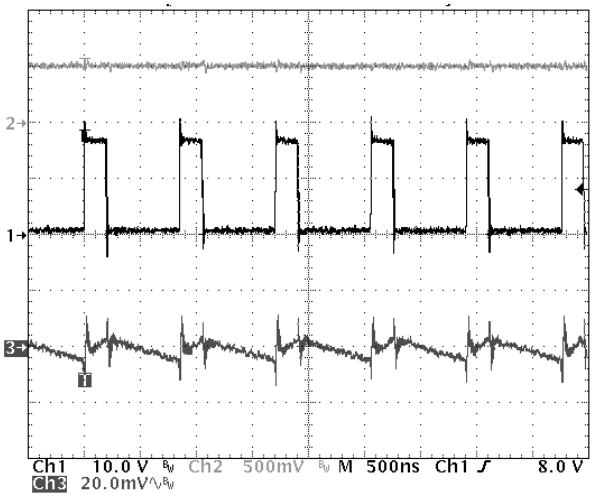


Figure 21. Typical Ripple for Voltage Operation
1 SW, 10 V/div DC, 2 FB, 500 mV/div DC, 3 V_{OUT}
20 mV/div AC, T = 500 ns/div

DETAIL OPERATING DESCRIPTION

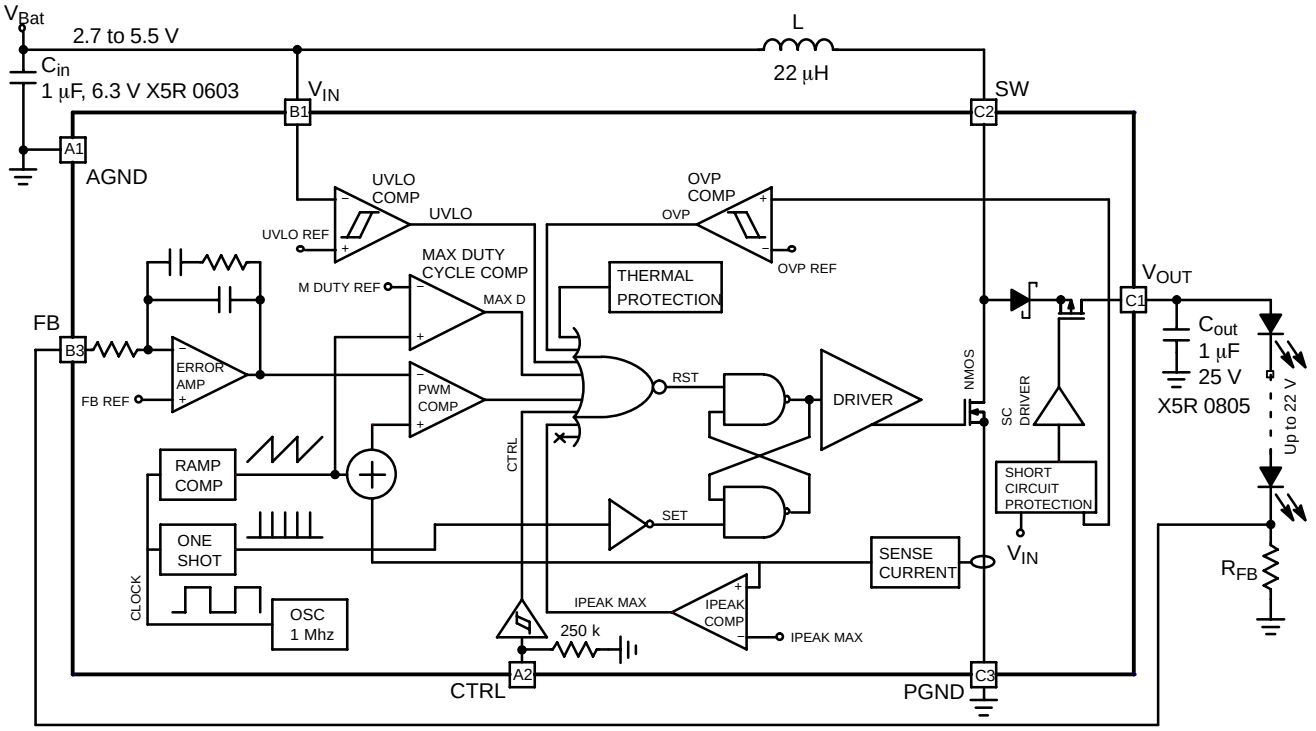


Figure 22. Functional Block Diagram

Operation

The NCP5010 DC−DC converter is based on a Current Mode PWM architecture which regulates the feedback voltage at 500 mV under normal operating conditions. The boost converter operates in two separate phases (See Figure 23). The first one is T_{ON} when the inductor is charged by current from the battery to store up energy, followed by T_{OFF} step where the power is transmitted through the internal rectifier to the load. The capacitor C_{OUT} is used to store energy during the T_{OFF} time and to supply current to the load during the T_{ON} stage thus constantly powering the load.

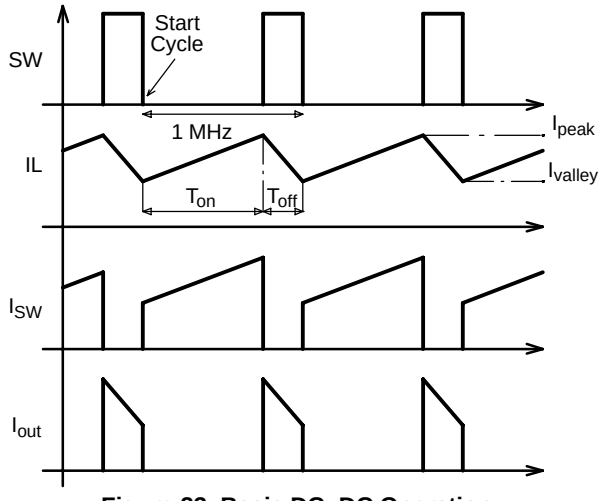


Figure 23. Basic DC−DC Operation

The internal oscillator provides a 1 MHz clock signal to trigger the PWM controller on each rising edge (SET signal) which starts a cycle. During this phase the low side NMOS switch is turned on thus increasing the current through the inductor. The switch current is measured by the SENSE CURRENT and added to the RAMP COMP signal. Then PWM COMP compares the output of the adder and the signal from ERROR AMP. When the comparator threshold is exceeded, the NMOS switch is turned off until the rising edge of the next clock cycle. In addition, there are six functions which can reset the flip−flop logic to switch off the NMOS. The MAX DUTY CYCLE COMP monitors the pulse width and if it exceeds 95% (nom) of the cycle time the switch will be turned off. This limits the switch from being on for more than one cycle. Due to IPEAK COMP, the current through the inductor is monitored and compared with the I_{PEAK_MAX} threshold set at 440 mA (nom). If the current exceeds this value, the controller is will turn off the NMOS switch for the remainder of the cycle. This is a safety function to prevent any excessive current that could overload the inductor and the power stage. The four other safety circuits are SHORT CIRCUIT PROTECTION, OVP, UVLO, and THERMAL PROTECTION. Please refer to the detail in following sections.

The loop stability is compensated by the ERROR AMP built in integrator. The gain and the loop bandwidth are fixed internally and provides a phase margin greater than 45° whatever the current supplied.

LED Current Selection

The feedback resistor (R_{FB}) determines the average maximum current through the LED string. The control loop regulated the current such that the average voltage at the FB input is 500 mV (nom). For example, should one need a 20 mA output current in the primary branch, R_{FB} should be selected according to the following equation:

$$R_{FB} = \frac{F_{BV}}{I_{OUT}} = \frac{500\ mV}{20\ mA} = 25\ \Omega$$

In white LED applications it is desirable to operate the LEDs at a specific operating current as the color will shift as the bias current is changed. As a result of this effect, it is recommended to dim the LED string by a pulse width modulation techniques. A low frequency PWM signal can be applied to the CTRL input and by varying the duty cycle the brightness of the LED can be changed. To avoid any optical flicker, the frequency must be higher than 100 Hz and preferably less than 1 kHz. Due to the soft−start function set at 600 μs (nom) with higher frequency the device remains active but the brightness can decrease. Nevertheless in this case, a dimming control using a filtered PWM signal (See Figure 33) can be used. Also for DC voltage control the same technique is suitable and the filter is takes away.

Inductor Selection

To choose the inductor there are three different electrical parameters that need to be considered, the absolute value of the inductor, the saturation current and the DCR. In normal operation, this device is intended to operate in Continuous Conduction Mode (CCM) so the following equation below can be used to calculate the peak current:

$$I_{PEAK} = \frac{I_{OUT}}{\eta(1 - D)} + \frac{V_{IN}D}{2LF}$$

In the equation above, V_{IN} is the battery voltage, I_{OUT} is the load current, L the inductor value, F the switching frequency, and the duty cycle D is given by:

$$D = \left(1 - \frac{V_{IN}}{V_{OUT}}\right)$$

η is the global converter efficiency which can vary with load current (see Figure 3 thru Figure 8). A good approximation is to use η = 0.8. Figure 24 − Figure 26 are a graphical representation of the above equations, as a function of the desired I_{OUT}, V_{IN}, and number of LEDs in series (V_F = 3.5 V nominal). The curves are limited to an I_{PEAK_MAX} of 300 mA. It is important to analyze this at worst case Vf conditions to ensure that the inductor current rated is high enough such that it not saturate.

The recommended inductor value should range between 10 μH and 22 μH. As can be seen from the curves, as the inductor size is reduced, the peak current for a given set of conditions increases along with higher current ripple so it is not possible to deliver maximum output power at lower inductor values.

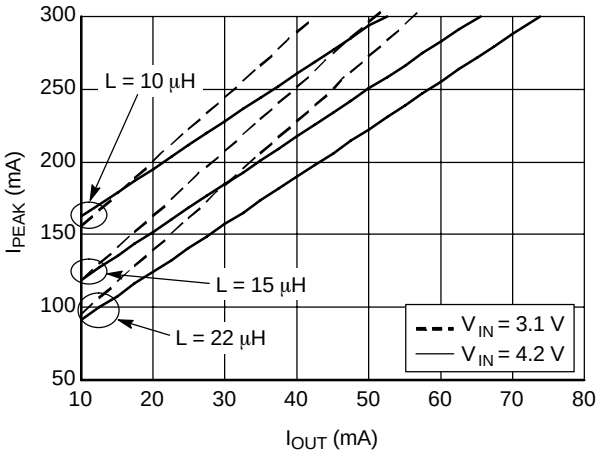


Figure 24. Peak Inductor Currents vs. I_{OUT} (mA) @ 3 LEDs, 10.5 V

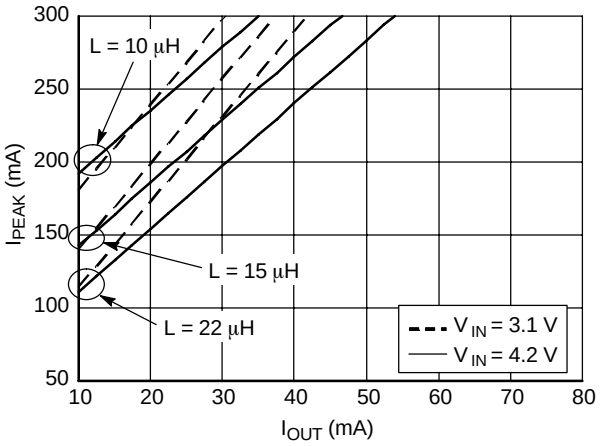


Figure 25. Peak Inductor Currents vs. I_{OUT} (mA) @ 4 LEDs, 14 V

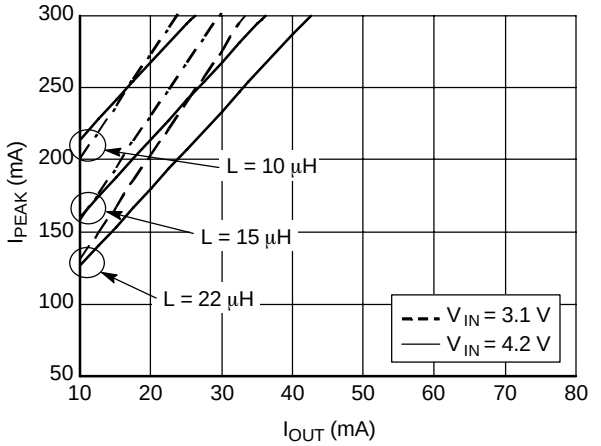


Figure 26. Peak Inductor Currents vs. I_{OUT} (mA) @ 5 LEDs, 17.5 V

Finally an acceptable DCR must be selected regarding losses in the coil and must be lower than 1.4 Ω to limit excessive voltage drop. In addition, as DCR is reduced, overall efficiency will improve. Some recommended inductors include but are not limited to:

TDK VLF4012AT−220MR51

TDK VLP4612T−220MR34

TDK VLP5610T−220MR45

Coilcraft LPO6610−223M

Coilcraft DO1605T−223MX

Coilcraft DT1608C−223

Capacitor Selection

To minimize the output ripple, a low ESR multi−layer ceramic capacitor type X5R or equivalent should be selected. For LED driver applications a 1 μF (min) 25 V is adequate. The NCP5010 can be operated in a voltage mode configuration (see Figure 34) for applications such as OLED power. Under these conditions, C_{OUT} can be increased to 2.2 μF, 25 V or more to reduce the output ripple.

The input needs to be bypassed by a X5R or an equivalent low ESR ceramic capacitor near the V_{IN} pin. A 1 μF, 6.3 V is enough for most applications. However, if the connection between V_{IN} and the battery is too long then a 4.7 μF or higher ceramic capacitor may be needed. Some recommended capacitors include but are not limited to:

TDK C1608X5R1E105MT

TDK C2012X5R1E105MT

TDK C1608X5R0J105MT

TDK C2012X5R1E225MT

Murata GRM185R61A105KE36D

Murata GRM188R60J475KE19D

Murata GRM216R61E105KA12D

Short−Circuit Protection

If V_{OUT} is falls below 50% of V_{IN} then a short−circuit condition is detected. When this event is detected, the PWM circuitry is disabled and the NMOS power switch is not turned on. Power will be supplied to the load through the inductor, rectifier and high side switch. Once V_{OUT} reaches 66% of V_{IN}, then the PWM circuitry is enabled. In normal conditions when the device is enabled by an active high signal on CTRL, the short circuit condition continues until the output capacitor is charged by the limited current up to 66% of V_{IN}.

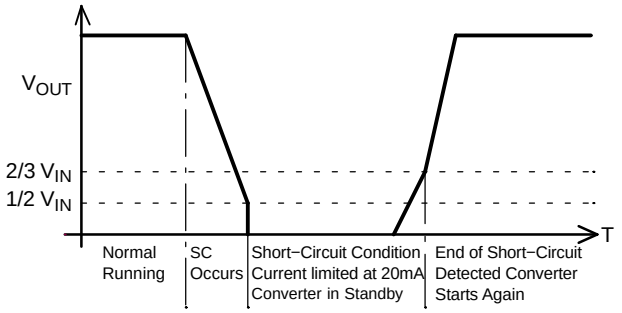


Figure 27. Example of the V_{OUT} Voltage Behavior When Short−Circuit Arises

Overvoltage Protection (OVP)

If there is an open load condition such as a loose connection to the White LED string, the converter will provide current to the C_{out} capacitor and the voltage at the output will rise rapidly. This could cause damage to the part if there was not some external clamping Zener clamping circuit. To eliminate the need for these external components, the NCP5010 incorporates an OVP circuit which monitors the output voltage with a resistive divider network and a comparator and voltage reference. If the output reaches 22 V (nominal), the OVP circuit will detect a fault and inhibit PWM operation. This comparator has 1 V of hysteresis so when the load is reconnected and the voltage drops below 21 V, the PWM operation will resume automatically. The 22 V OVP threshold allows the use of 25 V ceramic capacitors for the output filter capacitor.

Undervoltage Lock Out (UVLO)

To ensure proper operation under all conditions, the device has a built−in undervoltage lock out (UVLO) circuit. During power−up, the device will remain disabled until the input voltage exceeds 2.4 V nominal. This circuit has 200 mV of hysteresis to provide noise immunity to transient conditions.

Layout Recommendations

As with all switching DC/DC converter, care must be observed to the PCB board layout and component placement. To prevent electromagnetic interference (EMI) problems and reduce voltage ripple of the device any copper trace which see high frequency switching path should be optimized. So the input and output bypass ceramic capacitor, C_{IN} and C_{OUT} as depicted Figure 2 must be placed as close as possible the NCP5010 and connected directly between pins and ground plane. In additional, the track connection between the inductor and the switching input, SW pin must be minimized to reduce EMI radiation. Finally it is always good practice to keep way sensitive tracks such as feedback connection from switched signal like SW or VOUT connections. Figure 28 shown an example of optimized PCB layout.

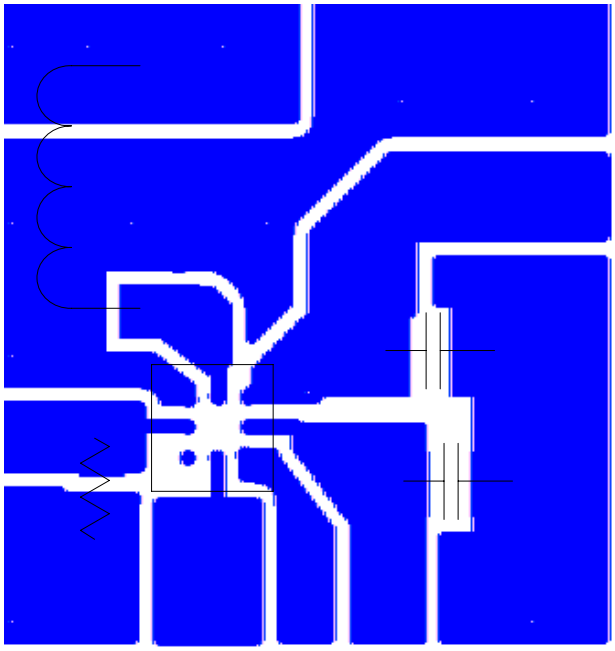


Figure 28. Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

Basic Feedback

Figure 29 is a basic application where a regulated courant is drive in a string of LEDs. A 20.8 mA current is fixed by R1 and LEDs are dim with PWM apply on CTRL pin.

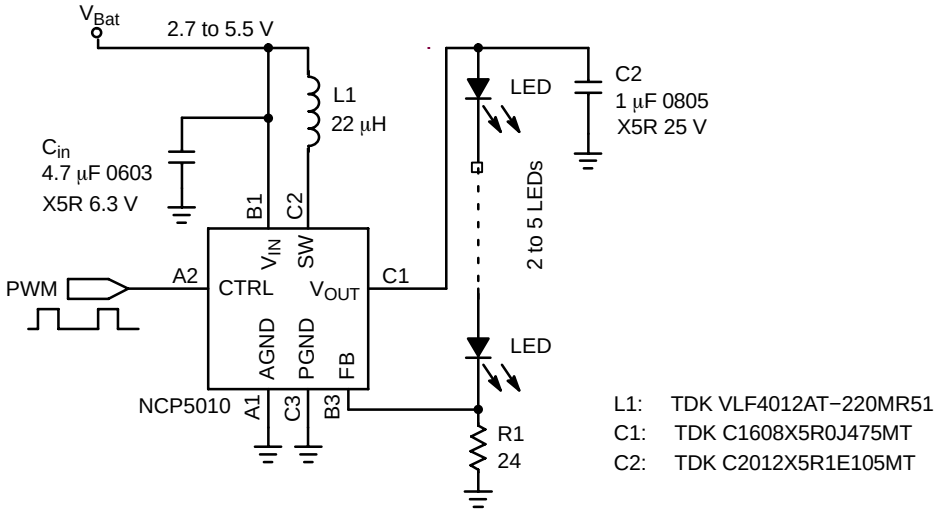


Figure 29. Typical Semi−Pulsed Mode of Operation

Different Supply

The NCP5010 can operate from two different supply: One end of the inductor (V_{BAT}) can be directly connected to a battery like 4 cell alkaline or 2 cell Li−Ion. And V_{IN} pin need a power delivered for example from an LDO. Care must be observed to have always V_{BAT} above V_{IN} and minimum output voltage range will be V_{BAT} voltage.

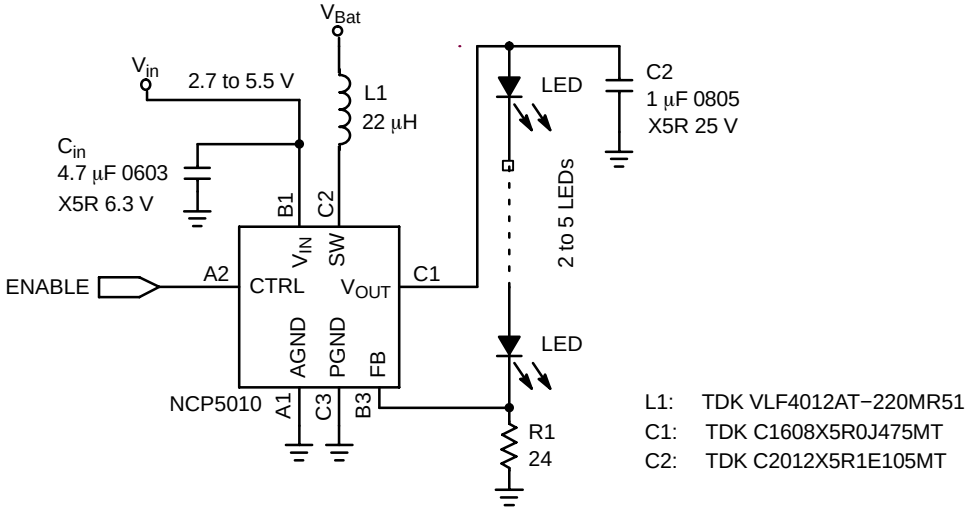


Figure 30. Operate from Different Supply

Multiple LEDs String

Since the output voltage in limited at 22 V (nom.), one can arrange the LEDs in 2 or more string. Figure 31 shows two LEDs branches where the constant current is regulated in primary branch and the secondary branch is selected by Q1. The number of LED in each string have to be the same.

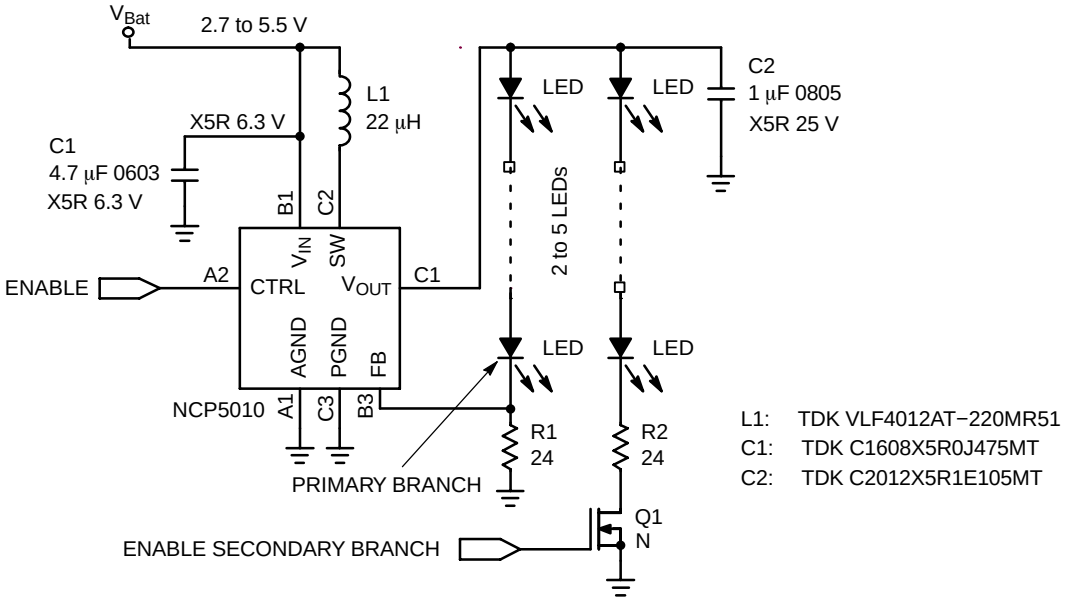


Figure 31. Multiple LED String Application

Matched LEDs Branches

Should one need to control precisely the current in two LEDs branches the schematic Figure 32 can be used. An dual NPN BC847BD is used to form a current mirror Q1 like this the current in the secondary branch I2 equal the current in primary branch I1. Thank to this current mirror the number of LEDs in secondary branch could be lower or equal than primary one.

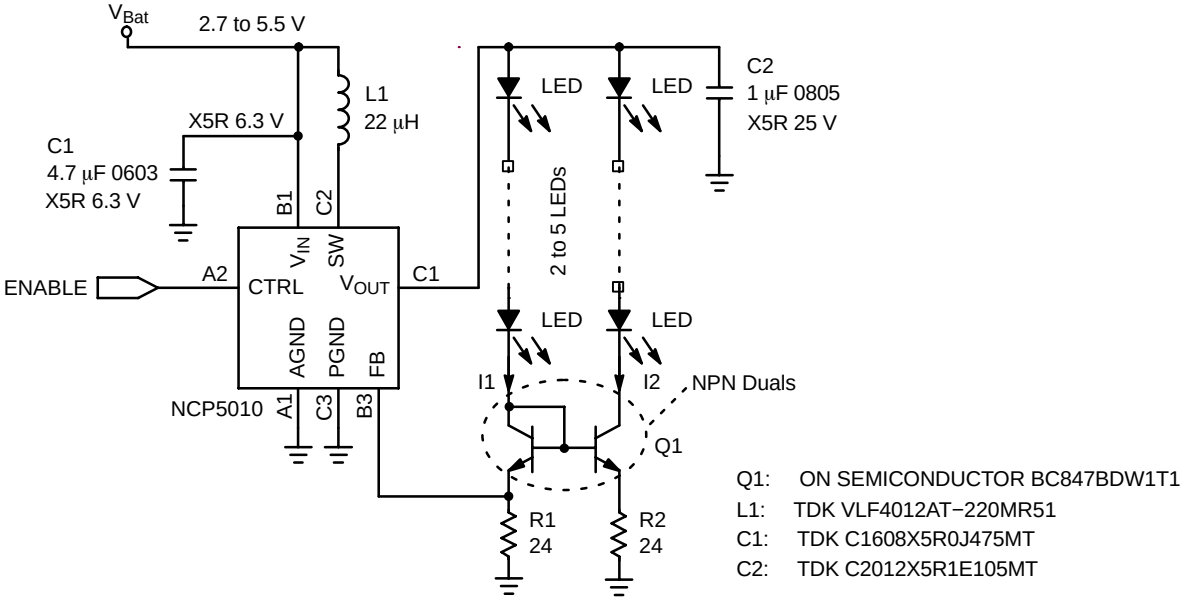


Figure 32. Matched 2 Branches of LEDs

Analog Dimming Control

When the NCP5010 is in steady state the output voltage is controlled in order to have 500 mV to the feedback input (FB pin). The principle of this schematic is bias by a resistive network R2/R3 the feedback voltage. If not any signal is put from outside to R2 there is no voltage drop across R3 and $I_{OUT} = V_{FB}/R4$. When the voltage put to R2 is increasing the loop balance output voltage to get always 500 mV to FB pin. Thereby voltage across R4 decreases like this the current in the string of LEDs.

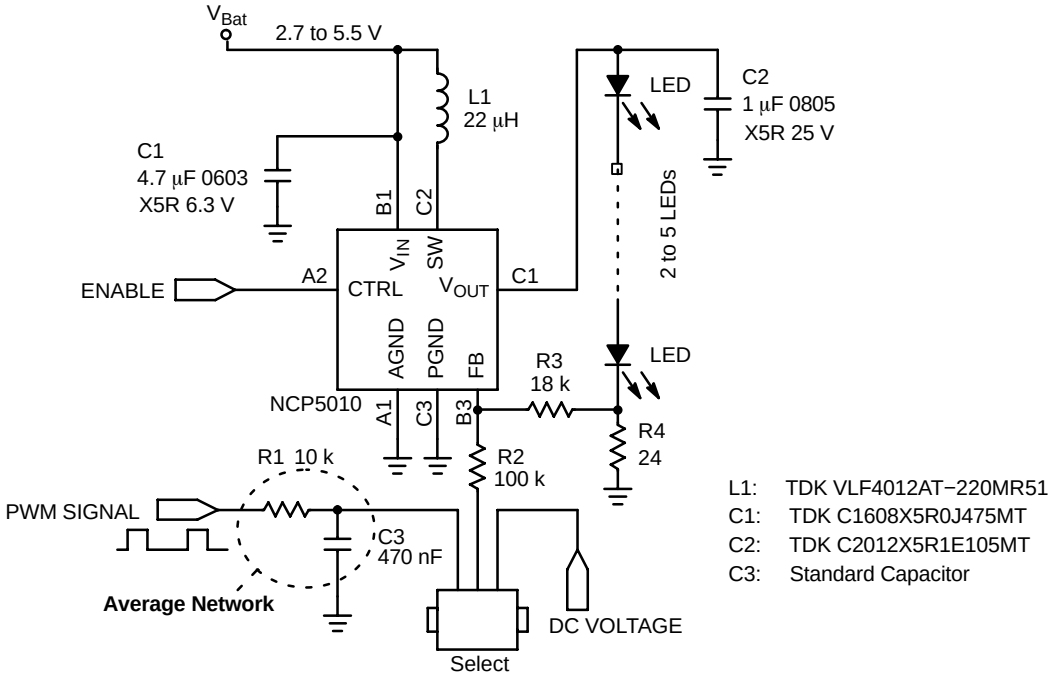


Figure 33. Dimming Control Using a Filtered PWM Signal or a DC Voltage

DC/DC Boost Application

The NCP5010 can be used as DC/DC Boost converter to deliver constant voltage to powering load like OLED or LCD biasing. An external resistive network is connected to sense the output voltage and close the loop.

$$V_{out} = 0.5 \times \left(\frac{R1 + R2}{R1}\right)$$

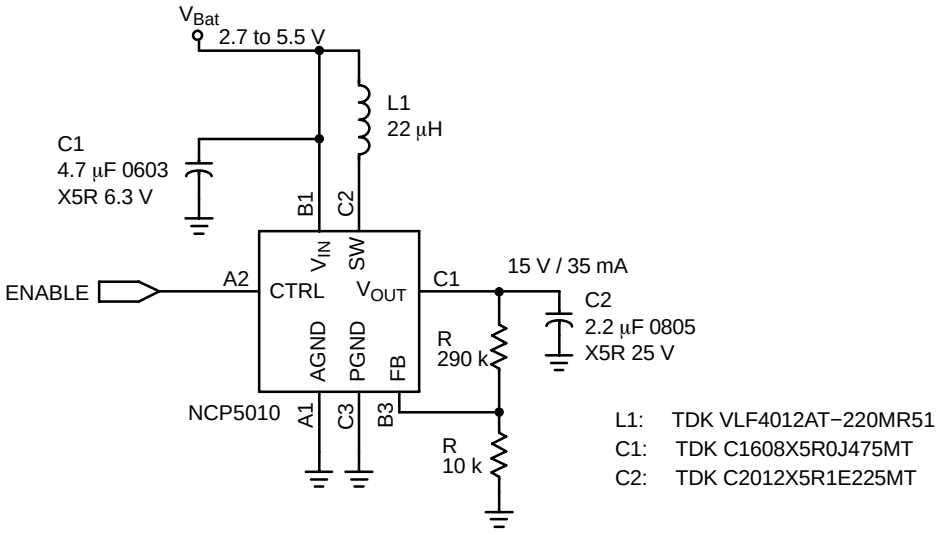


Figure 34. OLED or LCD Bias Supply

ORDERING INFORMATION

Device	Marking	Operating Temperature Range	Package	Shipping†
NCP5010FCT1G	DAX	−40°C to +85°C	8−Pin Flip−Chip CSP (Pb−Free)	3000 Tape and Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

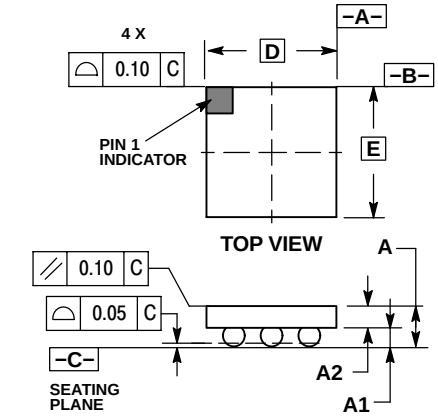
Two type of demo boards available:

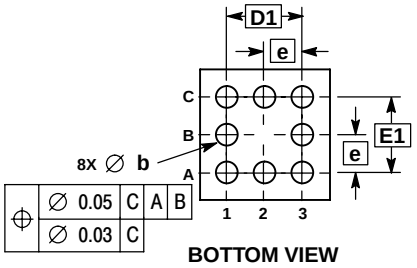
- The NCP5010EVB board which configures the device driving a string of 2−5 White LEDs in series.
- The NCP5010BIASEVB board for applications such as powering an OLED panel or LCD biasing.

Finally in addition to these demo boards, Application Note “ANDXXXX/D” deals with configuring the NCP5010 with a high side sense resistor.

PACKAGE DIMENSIONS

8−PIN FLIP−CHIP
FC SUFFIX
CASE 499AJ−01
ISSUE A

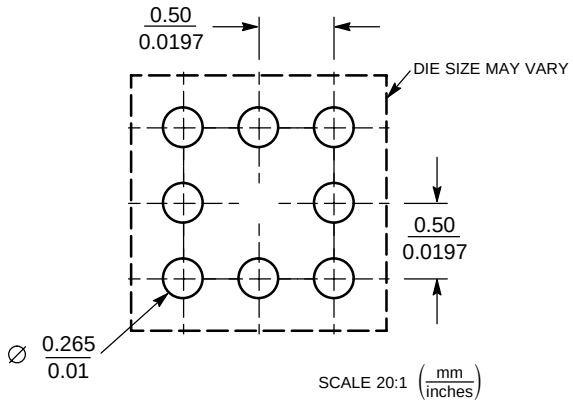




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.6 BSC	
A1	0.210	0.270
A2	0.330	0.390
D	1.70 BSC	
E	1.70 BSC	
b	0.290	0.340
e	0.500 BSC	
D1	1.000 BSC	
E1	1.000 BSC	

SOLDERING FOOTPRINT



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NCP5010/D