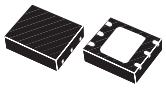
Automotive grade 1 A, low quiescent current, low-noise voltage regulator



DFN6 (3x3 mm)

Features

- AEC-Q100 qualified
- Input voltage from 1.5 to 5.5 V
- Ultra-low dropout voltage (200 mV typ. at 1 A load)
- Very low quiescent current (20 µA typ. at no load, 200 µA typ. at 1 A load, 1 µA max. in off mode)
- Very low-noise with no bypass capacitor (30 µ V_{RMS} at V_{OUT} = 0.8 V)
- Output voltage tolerance: ±2.0% at 25 °C
- 1 A guaranteed output current
- Wide range of output voltages available on request: 0.8 V to 4.5 V with 100 mV step and adjustable from 0.8
- Logic-controlled electronic shutdown
- Stable with ceramic capacitors C_{OUT} = 1 µF
- Internal current and thermal limit
- DFN6 (3x3 mm) package
- Temperature range: -40 °C to 125 °C

Maturity status link
LD39100

Applications

- Printers
- Game consoles
- Computer
- Consumer applications
- Automotive post regulation

Description

The LD39100 provides 1 A maximum current with an input voltage range from 1.5 V to 5.5 V and a typical dropout voltage of 200 mV. The device is stable with ceramic capacitors on the input and output.

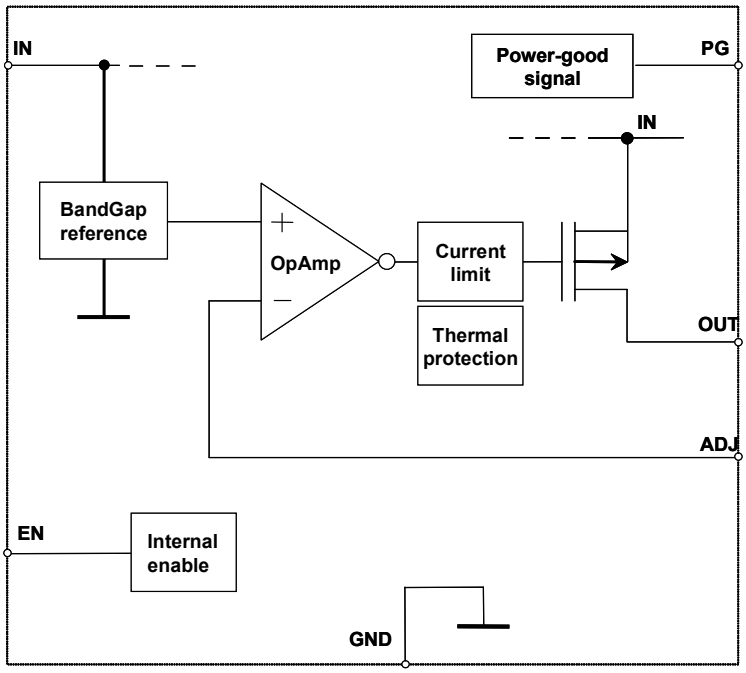
The ultra-low dropout voltage, low quiescent current and low-noise features make it suitable for low power battery-powered applications. Power supply rejection is 70 dB at low frequency and starts to roll off at 10 kHz.

Enable logic control function puts the LD39100 in shutdown mode, allowing a total current consumption lower than 1 µA. The device also includes short-circuit constant current limiting and thermal protection.

LD39100 is available also in AEC-Q100 qualified version, in the DFN6 (3x3 mm) with wettable flank package.

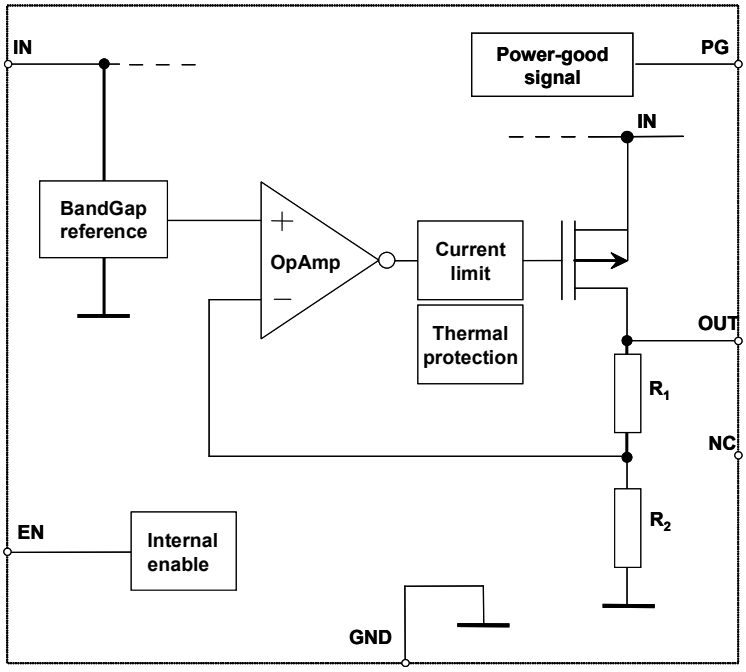
1 Circuit schematics

Figure 1. **LD39100 schematic diagram (adjustable version)**



GIPD010920151332MT

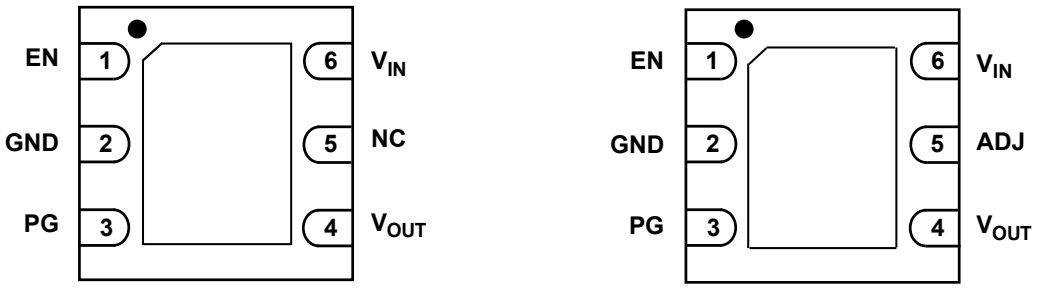
Figure 2. **LD39100 schematic diagram (fixed version)**



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2 Pin configuration

Figure 3. **Pin connection (top view)**



LD39100 (fixed version)

LD39100 (adjustable version)

GIPD010920151334MT

Table 1. **Pin description**

Symbol	Pin		Function
	LD39100 (adjustable version)	LD39100 (fixed version)	
EN	1	1	Enable pin logic input: low = shutdown, high = active
GND	2	2	Common ground
PG	3	3	Power Good
V_{OUT}	4	4	Output voltage
ADJ	5	-	Adjust pin
V_{IN}	6	6	LDO input voltage
NC	-	5	Not connected
GND	Exposed pad		Exposed pad has to be connected to GND

3 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	DC input voltage	-0.3 to 7	V
V_{OUT}	DC output voltage	-0.3 to V_{IN} + 0.3 (7 V max.)	V
EN	Enable pin	-0.3 to 7	V
PG	Power Good pin	-0.3 to 7	V
ADJ	Adjust pin	4	V
I_{OUT}	Output current	Internally limited	
P_D	Power dissipation	Internally limited	
T_{STG}	Storage temperature range	- 65 to 150	°C
T_{OP}	Operating junction temperature range	- 40 to 125	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All values are referred to GND.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	55	°C/W
R_{thJC}	Thermal resistance junction-case	10	°C/W

Table 4. ESD performance

Symbol	Parameter	Test conditions	Value	Unit
ESD	ESD protection voltage	HBM	4	kV
		MM	0.4	kV

4 Electrical characteristics

Table 5. LD39100 electrical characteristics (adjustable version) T_J = 25 °C, V_{IN} = 1.8 V, C_{IN} = C_{OUT} = 1 µF, I_{OUT} = 100 mA, V_{EN} = V_{IN}, unless otherwise specified

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage		1.5		5.5	V
V_{ADJ}	V_{ADJ} accuracy	I_{OUT} = 10 mA T_J = 25 °C	784	800	816	mV
		I_{OUT} = 10 mA -40 °C < T_J < 125 °C	776	800	824	
I_{ADJ}	Adjust pin current				1	µA
ΔV_{OUT}	Static line regulation	V_{OUT} + 1 V ≤ V_{IN} ≤ 5.5 V I_{OUT} = 100 mA		0.01		%/V
ΔV_{OUT}	Transient line regulation	ΔV_{IN} = 500 mV I_{OUT} = 100 mA t_R = 5 µs		10		mVpp
		ΔV_{IN} = 500 mV I_{OUT} = 100 mA t_F = 5 µs		10		
ΔV_{OUT}	Static load regulation	I_{OUT} = 10 mA to 1 A		0.002		%/mA
ΔV_{OUT}	Transient load regulation	I_{OUT} = 10 mA to 1 A t_R = 5 µs		40		mVpp
		I_{OUT} = 1 A to 10 mA t_F = 5 µs		40		
V_{DROP}	Dropout voltage [2]	I_{OUT} = 1 A V_O fixed to 1.5 V -40 °C < T_J < 125 °C		200	400	mV
e_N	Output noise voltage	10 Hz to 100 kHz I_{OUT} = 100 mA V_{OUT} = 0.8 V		30		μV_{RMS}
SVR	Supply voltage rejection V_O = 0.8 V	V_{IN} = 1.8 V+/-V_{RIPPLE} V_{RIPPLE} = 0.25 V frequency = 1 kHz I_{OUT} = 10 mA		70		dB
		V_{IN} = 1.8 V+/-V_{RIPPLE} V_{RIPPLE} = 0.25 V frequency = 10 kHz I_{OUT} = 100 mA		65		
I_Q	Quiescent current	I_{OUT} = 0 mA		20		µA
		I_{OUT} = 0 mA -40 °C < T_J < 125 °C			50	
		I_{OUT} = 0 to 1 A		200		

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_Q	Quiescent current	I_{OUT} = 0 to 1 A -40 °C < T_J < 125 °C			300	µA
		V_{IN} input current in off mode: V_{EN} = GND (3)		0.001	1	
PG	Power good output threshold	Rising edge		0.92* V_{OUT}		V
		Falling edge		0.8* V_{OUT}		
	Power good output voltage low	Isink = 6 mA open drain output			0.4	V
I_{SC}	Short-circuit current	R_L= 0		2.5		A
V_{EN}	Enable input logic low	V_{IN} = 1.5 V to 5.5 V -40 °C < T_J< 125 °C			0.4	V
	Enable input logic high		0.9			V
I_{EN}	Enable pin input current	V_{EN} = V_{IN}		0.1	100	nA
t_{ON}	Turn-on time (4)			30		µs
T_{SHDN}	Thermal shutdown			160		°C
	Hysteresis			20		
C_{OUT}	Output capacitor	Capacitance (see Section 5)	1			µF

1. *All transient values are guaranteed by design, not tested in production.*
2. *Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value. This specification does not apply to output voltages below 1.5 V.*
3. *PG pin floating.*
4. *Turn-on time is time measured between the enable input just exceeding V_{EN} high value and the output voltage just reaching 95% of its nominal value.*

Table 6. LD39100 electrical characteristics (fixed version) T_J = 25 °C, V_{IN} = $V_{OUT(NOM)}$ + 1 V, C_{IN} = C_{OUT} = 1 µF, I_{OUT} = 100 mA, V_{EN} = V_{IN}, unless otherwise specified

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_I	Operating input voltage		1.5		5.5	V
V_{OUT}	V_{OUT} accuracy	V_{OUT} > 1.5 V, I_{OUT} = 10 mA T_J = 25 °C	-2.0		2.0	%
		V_{OUT} > 1.5 V, I_{OUT} = 10 mA -40 °C < T_J < 125 °C	-3.0		3.0	
		V_{OUT} ≤ 1.5 V I_{OUT} = 10 mA		±20		mV
		V_{OUT} ≤ 1.5 V I_{OUT} = 10 mA -40 °C < T_J < 125 °C		±30		
ΔV_{OUT}	Static line regulation	V_{OUT} + 1 V ≤ V_{IN} ≤ 5.5 V I_{OUT} = 100 mA		0.01		%/V
ΔV_{OUT}	Transient line regulation (1)	ΔV_{IN} = 500 mV I_{OUT} = 100 mA, t_R = 5 µs		10		mVpp
		ΔV_{IN} = 500 mV I_{OUT} = 100 mA, t_F = 5 µs		10		
ΔV_{OUT}	Static load regulation	I_{OUT} = 10 mA to 1 A		0.002		%/mA
ΔV_{OUT}	Transient load regulation	I_{OUT} = 10 mA to 1 A t_R = 5 µs		40		mVpp
		I_{OUT} = 1 A to 10 mA t_F = 5 µs		40		
V_{DROP}	Dropout voltage (2)	I_{OUT} = 1 A V_{OUT} > 1.5 V -40 °C < T_J < 125 °C		200	400	mV
e_N	Output noise voltage	10 Hz to 100 kHz I_{OUT} = 100 mA V_{OUT} = 2.5 V		85		μV_{RMS}
SVR	Supply voltage rejection V_{OUT} = 1.5 V	V_{IN} = $V_{OUT(NOM)}$+0.5 V+/-V_{RIPPLE} V_{RIPPLE} = 0.1 V frequency = 1 kHz I_{OUT} = 10 mA		65		dB
		V_{IN} = $V_{OUT(NOM)}$+0.5 V+/-V_{RIPPLE} V_{RIPPLE} = 0.1 V frequency = 10 kHz I_{OUT} = 100 mA		62		
I_Q	Quiescent current	I_{OUT} = 0 mA		20		µA
		I_{OUT} = 0 mA -40 °C < T_J < 125 °C			50	
		I_{OUT} = 0 to 1 A		200		

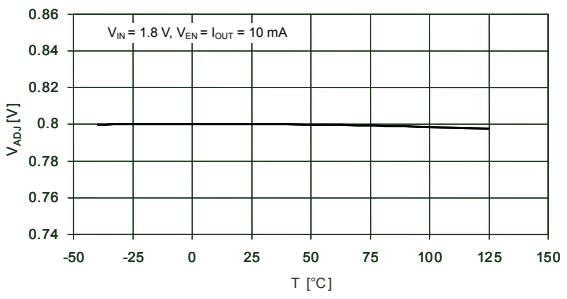
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_Q	Quiescent current	I_{OUT} = 0 to 1 A -40 °C < T_J < 125 °C			300	µA
		V_{IN} input current in OFF mode: (3) V_{EN} = GND		0.001	1	
PG	Power good output threshold	Rising edge		0.92* V_{OUT}		V
		Falling edge		0.8* V_{OUT}		
	Power good output voltage low	Isink = 6 mA open drain output			0.4	V
I_{SC}	Short-circuit current	R_L = 0		2.5		A
V_{EN}	Enable input logic low	V_{IN} = 1.5 V to 5.5 V -40 °C < T_J < 125 °C			0.4	V
	Enable input logic high		0.9			V
I_{EN}	Enable pin input current	V_{EN} = V_{IN}		0.1	100	nA
T_{ON}	Turn-on time (4)			30		µs
T_{SHDN}	Thermal shutdown			160		°C
	Hysteresis			20		
C_{OUT}	Output capacitor	Capacitance (see Section 5)	1			µF

1. *All transient values are guaranteed by design, not tested in production.*
2. *Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value. This specification does not apply to output voltages below 1.5 V.*
3. *PG pin floating.*
4. *Turn-on time is time measured between the enable input just exceeding V_{EN} high value and the output voltage just reaching 95% of its nominal value.*

5 Typical performance characteristics

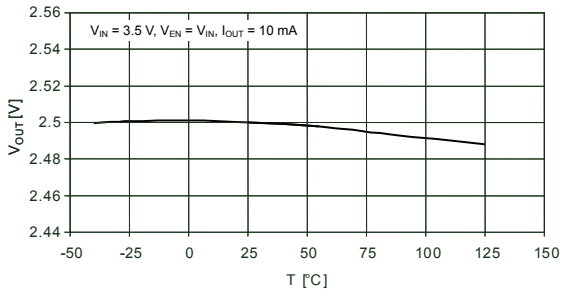
$C_{IN} = C_{OUT} = 1\ \mu F$

Figure 4. V_{ADJ} accuracy



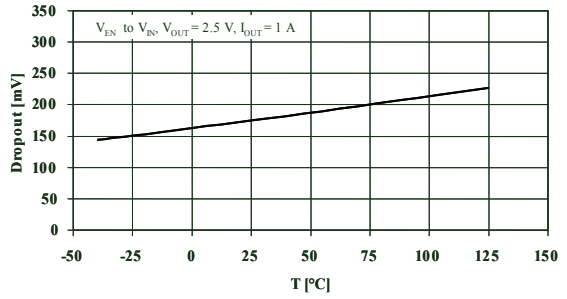
GIPD02092015 1100M T

Figure 5. V_{OUT} accuracy



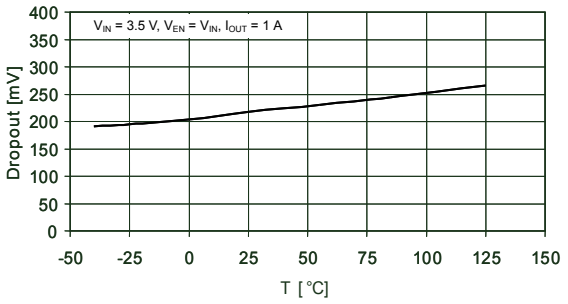
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Figure 6. Dropout voltage vs. temperature (V_{OUT} = 2.5 V)



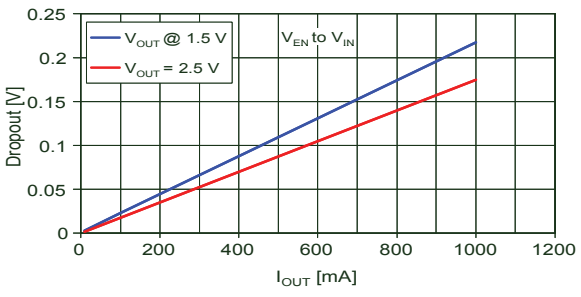
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Figure 7. Dropout voltage vs. temperature (V_{OUT} = 1.5 V)



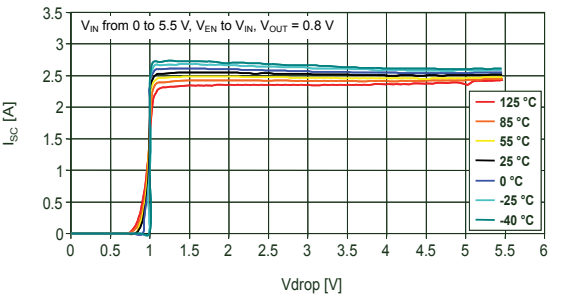
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Figure 8. Dropout voltage vs. output current



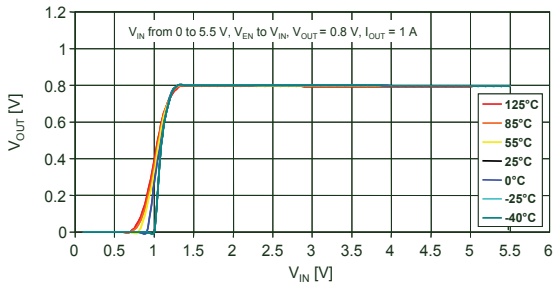
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Figure 9. Short-circuit current vs. drop voltage



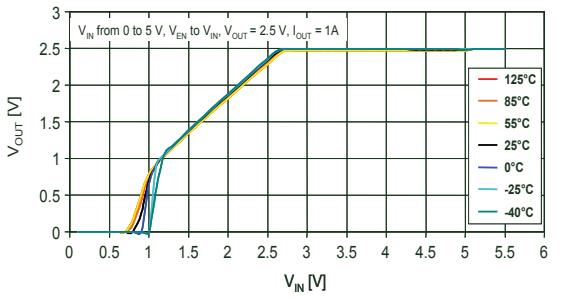
GIPD02092015 1105M T

Figure 10. Output voltage vs. input voltage (V_{OUT} = 0.8 V)



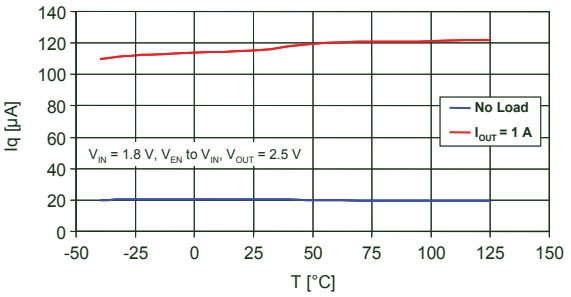
GIPD020920151106MT

Figure 11. Output voltage vs. input voltage (V_{OUT} = 2.5 V)



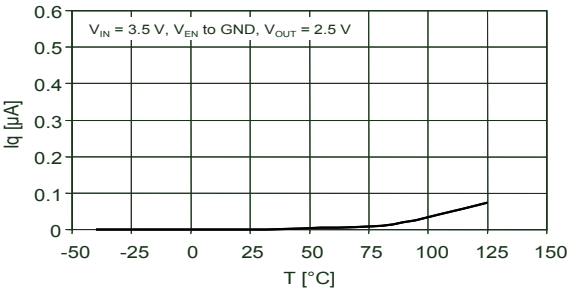
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Figure 12. Quiescent current vs. temperature



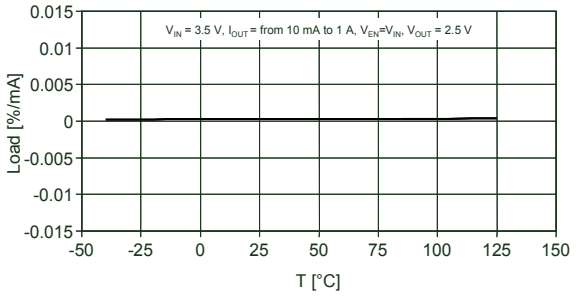
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Figure 13. V_{IN} input current in off mode vs. temperature



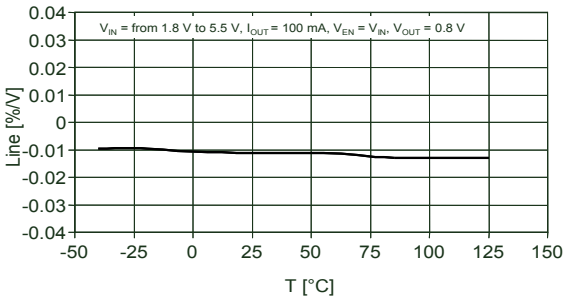
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Figure 14. Load regulation



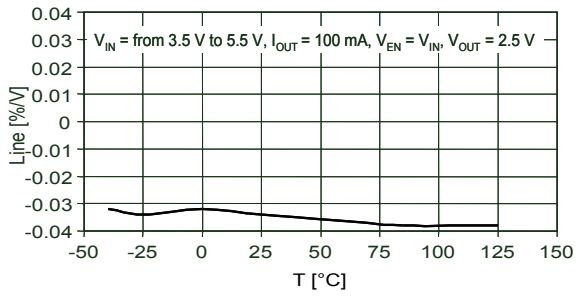
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Figure 15. Line regulation V_{OUT} = 0.8 V



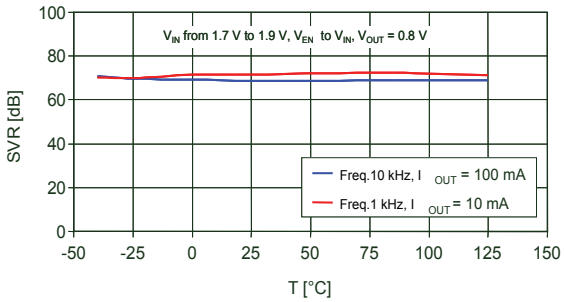
GIPD020920151111MT

Figure 16. Line regulation V_{OUT} = 2.5 V



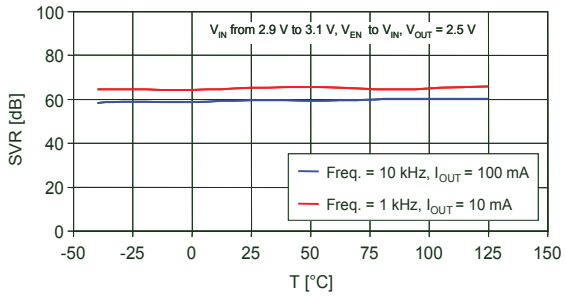
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Figure 17. Supply voltage rejection vs. temperature (V_{OUT} = 0.8 V)



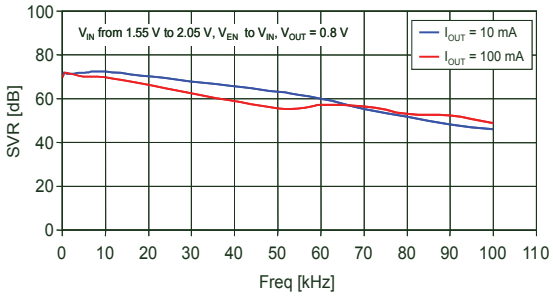
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Figure 18. Supply voltage rejection vs. temperature (V_{OUT} = 2.5 V)



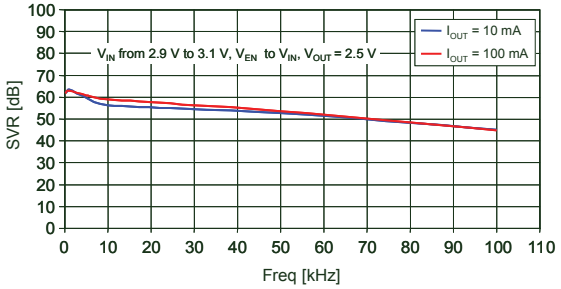
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Figure 19. Supply voltage rejection vs. frequency (V_{OUT} = 0.8 V)



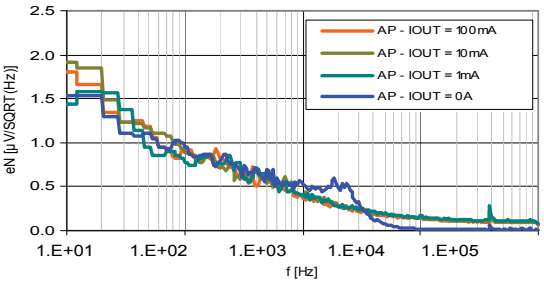
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Figure 20. Supply voltage rejection vs. frequency (V_{OUT} = 2.5 V)



GIPD020920151116MT

Figure 21. Output noise voltage vs. frequency



V_{IN} = 1.8 V, V_{OUT} = 0.8 V, V_{EN} = V_{IN}

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Figure 22. Enable voltage vs. temperature

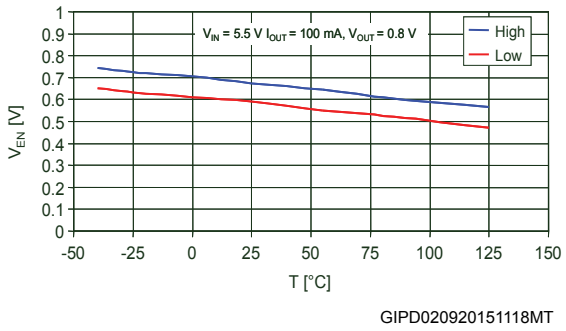
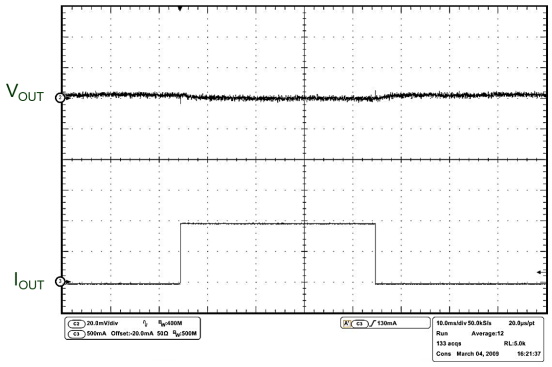
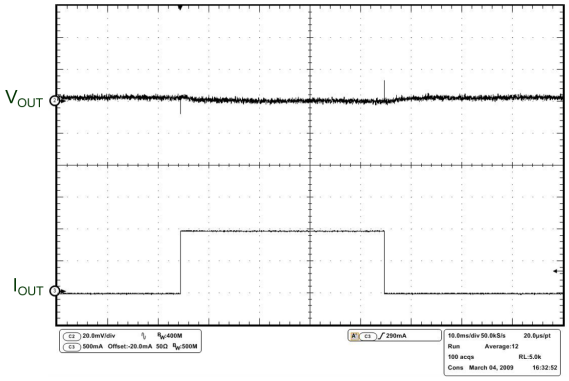


Figure 23. Load Transient (V_{OUT} = 0.8 V, I_{OUT} = from 10 mA to 1 A)



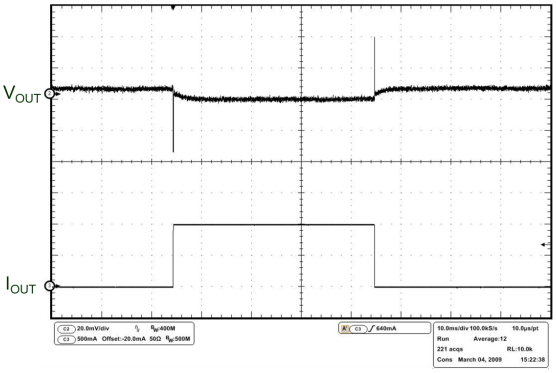
V_{EN} = V_{IN} = 3.5 V, V_{OUT} = 0.8 V, I_{OUT} = from 10 mA to 1 A, t_R = t_F = 5 µs

Figure 24. Load Transient (V_{OUT} = 0.8 V, I_{OUT} = from 100 mA to 1 A)



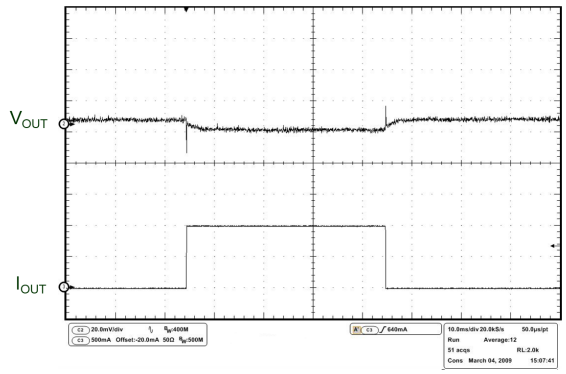
V_{EN} = V_{IN} = 3.5 V, V_{OUT} = 0.8 V, I_{OUT} = from 100 mA to 1 A, t_R = t_F = 5 µs

Figure 25. Load Transient (V_{OUT} = 2.5 V, I_{OUT} = from 10 mA to 1 A)



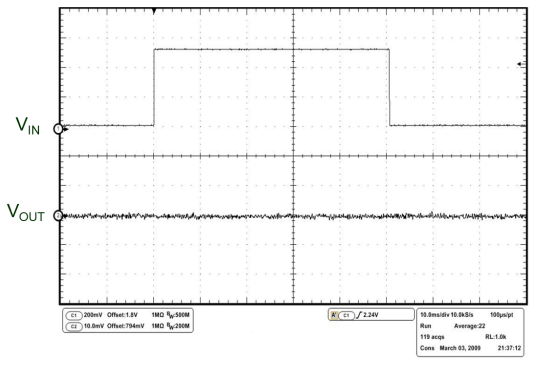
V_{EN} = V_{IN} = 3.5 V, V_{OUT} = 2.5 V, I_{OUT} = from 10 mA to 1A, t_R = t_F = 5 µs

Figure 26. Load Transient (V_{OUT} = 2.5 V, I_{OUT} = from 100 mA to 1 A)



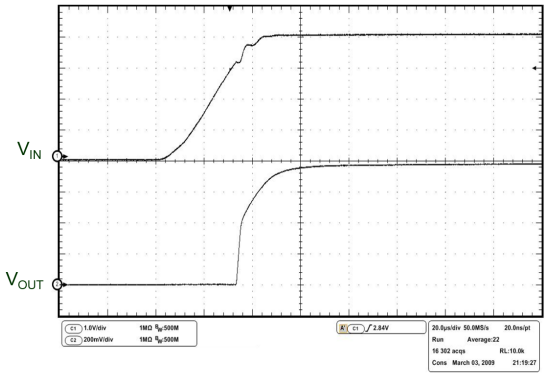
V_{EN} = V_{IN} = 3.5 V, V_{OUT} = 2.5 V, I_{OUT} = from 100 mA to 1A, t_R = t_F = 5 µs

Figure 27. Line transient



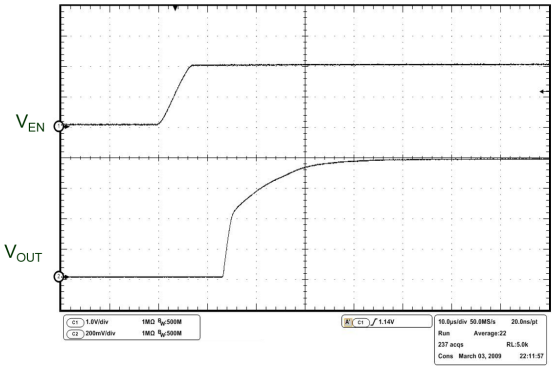
V_{IN} = 1.8 V to 2.3 V, V_{OUT} = 0.8 V, I_{OUT} = from 100 mA, t_R = t_F = 5 µs

Figure 28. Start-up transient



V_{EN} = V_{IN} = 0 V to 4 V, V_{OUT} = 0.8 V, I_{OUT} = 100 mA

Figure 29. Enable transient



V_{EN} = 0 V to 2 V, V_{IN} = 3.5 V, V_{OUT} = 0.8 V, I_{OUT} = 100 mA

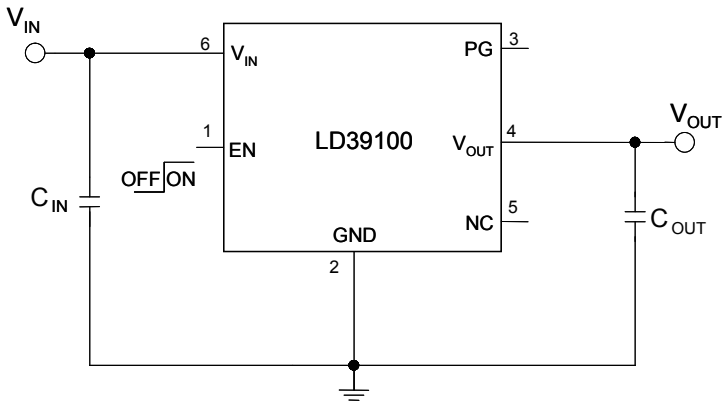
6 Application information

The LD39100 is an ultra low-dropout linear regulator. It provides up to 1 A with a low 200 mV dropout. The input voltage range is from 1.5 V to 5.5 V. The device is available in fixed and adjustable output versions.

The regulator is equipped with internal protection circuitry, such as short-circuit current limiting and thermal protection.

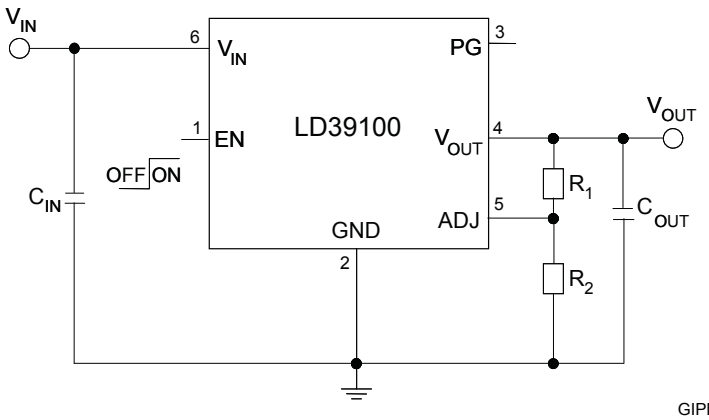
Figure 30. Typical application circuit for fixed output version and Figure 31. Typical application circuit for adjustable version illustrate the typical application schematics:

Figure 30. Typical application circuit for fixed output version



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Figure 31. Typical application circuit for adjustable version



GIPD040920151352MT

Regarding the adjustable version, the output voltage can be adjusted from 0.8 V up to the input voltage, minus the voltage drop across the pass element (dropout voltage), by connecting a resistor divider between ADJ pin and the output, thus allowing remote voltage sensing.

The resistor divider should be selected as follows:

$$V_{OUT} = V_{ADJ}\left(1 + R_1 / R_2\right) with V_{ADJ} = 0.8V\left(typ.\right) \quad (1)$$

Resistors should be used with values in the range from 10 kΩ to 50 kΩ. Lower values can also be suitable, but they increase current consumption.

6.1 External capacitors

The LD39100 voltage regulator requires external low ESR capacitors to assure control loop stability. These capacitors must be selected to meet the requirements of minimum capacitance and equivalent series resistance defined in the following sections.

Input and output capacitors should be located as close as possible to the relevant pins.

6.1.1 Input capacitor

An input capacitor with a minimum value of 1 µF must be located as close as possible to the input pin of the device and returned to a clean analog ground. A good quality, low-ESR ceramic capacitor is suggested. It helps to ensure stability of the control loop, reduces the effects of inductive sources and improves ripple rejection.

A value above 1 µF may be chosen when the application involves fast load transients.

6.1.2 Output capacitor

The LD39100 requires a low-ESR capacitor connected on its output to keep the control loop stable and reduce the risk of ringing and oscillations. The control loop is designed to be stable with any good quality ceramic capacitor (such as X5R/X7R types) with a minimum value of 1 µF and equivalent series resistance in the 0 to 150 mΩ range.

It is important to highlight that the output capacitor must maintain its capacitance and ESR in the stable region over the full operating temperature, load and input voltage ranges to assure stability. Therefore, capacitance and ESR variations must be taken into account in the design phase to ensure the device works in the expected stability region.

If the above conditions are respected, there is no maximum limit to the output capacitance.

6.2 Power dissipation

An internal thermal feedback loop disables the output voltage if the die temperature rises to approximately 160 °C. This feature protects the device from excessive temperature and allows the user to push the limits of the power handling capability of a given circuit board without the risk of damaging the device.

A good PC board layout should be used to maximize power dissipation. The thermal path for the heat generated by the device is from the die to the copper lead frame, through the package leads and exposed pad, to the PC board copper. The PC board copper acts as a heatsink. The footprint copper pads should be as wide as possible to spread and dissipate the heat to the surrounding ambient. Feed-through vias to the inner or backside copper layers are also useful to improve the overall thermal performance of the device.

The device power dissipation depends on the input voltage, output voltage and output current, and is given by:

$$P_D = (V_{IN} - V_{OUT})\, I_{OUT} \quad (2)$$

Junction temperature of the device is:

$$T_{J_MAX} = T_A + R_{thJA} \times P_D \quad (3)$$

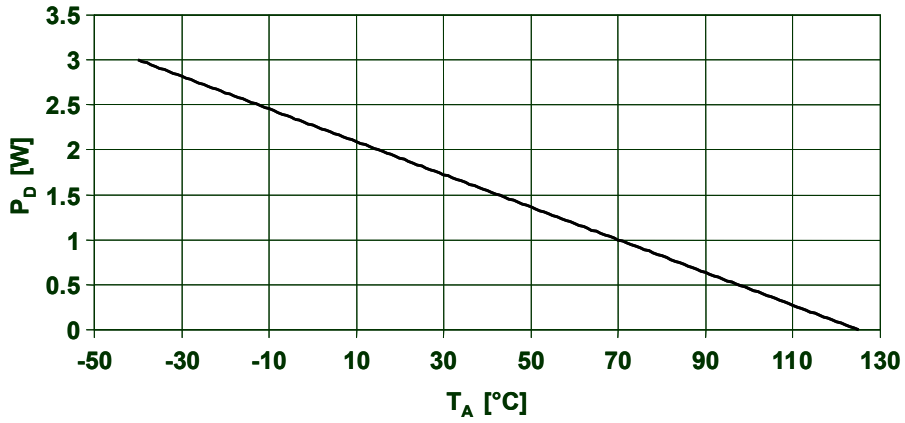
where:

T_{J_MAX} is the maximum junction of the die, 125 °C

T_A is the ambient temperature

R_{thJA} is the thermal resistance junction-to-ambient

Figure 32. **Power dissipation vs. ambient temperature**



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6.3 Enable function

The LD39100 features the enable function. When EN voltage is higher than 0.9 V, the device is ON, and if it is lower than 0.4 V, the device is OFF. In shutdown mode, consumption is lower than 1 µA.

EN pin has not an internal pull-up, so it cannot be left floating if it is not used.

6.4 Power Good function

Some applications require a flag showing that the output voltage is in the correct range.

Power Good threshold depends on the adjust voltage. When it is higher than $0.92*V_{ADJ}$, Power Good (PG) pin goes to high impedance. If it is below $0.80*V_{ADJ}$ PG pin goes to low impedance. If the device works well, Power Good pin is at high impedance. If the output voltage is fixed using an external or internal resistor divider, Power Good threshold is $0.92*V_{OUT}$.

If the device is disabled (EN pin low) the PG signal is set to high impedance.This is done intentionally to avoid pull down current by the PG pin in disabled mode.

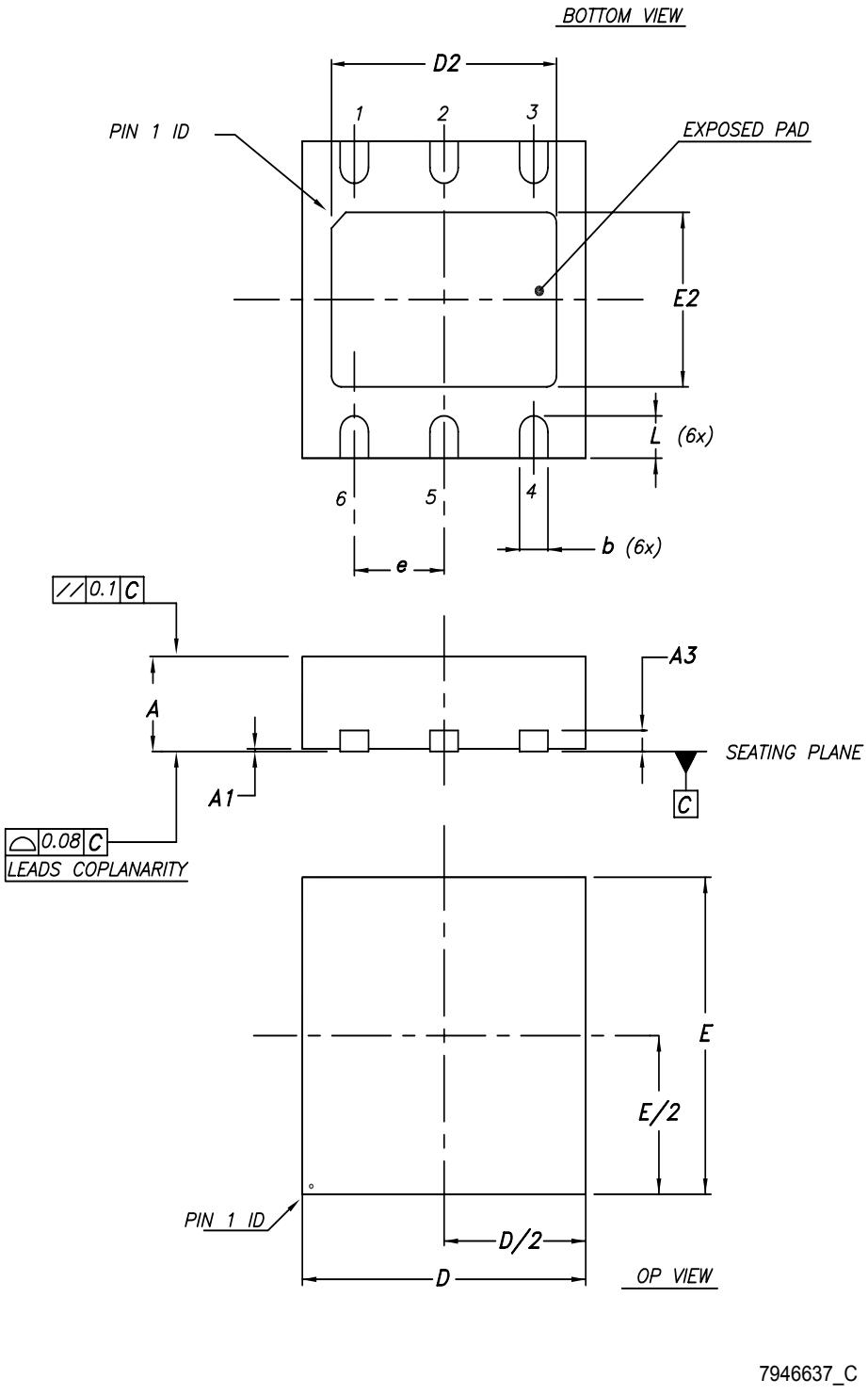
Power Good function requires an external pull-up resistor, which has to be connected between PG pin and V_{IN} or V_{OUT}. PG pin typical current capability is up to 6 mA. A pull-up resistor for PG should be in the range from 100 kΩ to 1 MΩ. If Power Good function is not used, PG pin has to remain floating.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 DFN6 (3x3 mm) package information

Figure 33. **DFN6 (3x3 mm) package outline**

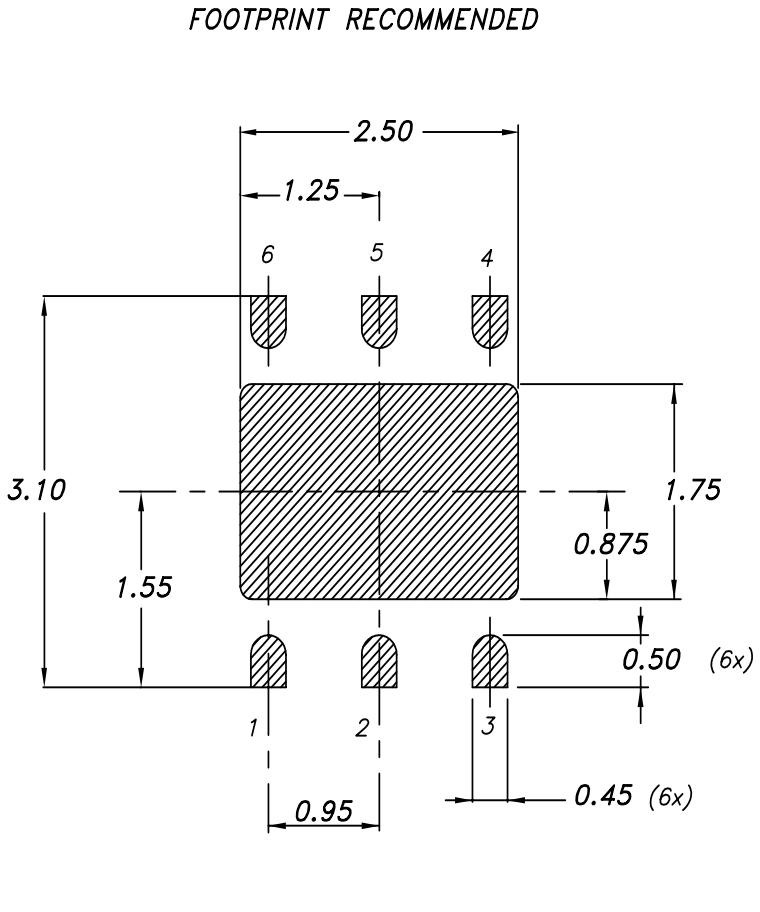


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Table 7. **DFN6 (3x3 mm) mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1
A1	0	0.02	0.05
A3		0.20	
b	0.23		0.45
D	2.90	3	3.10
D2	2.23		2.50
E	2.90	3	3.10
E2	1.50		1.75
e		0.95	
L	0.30	0.40	0.50

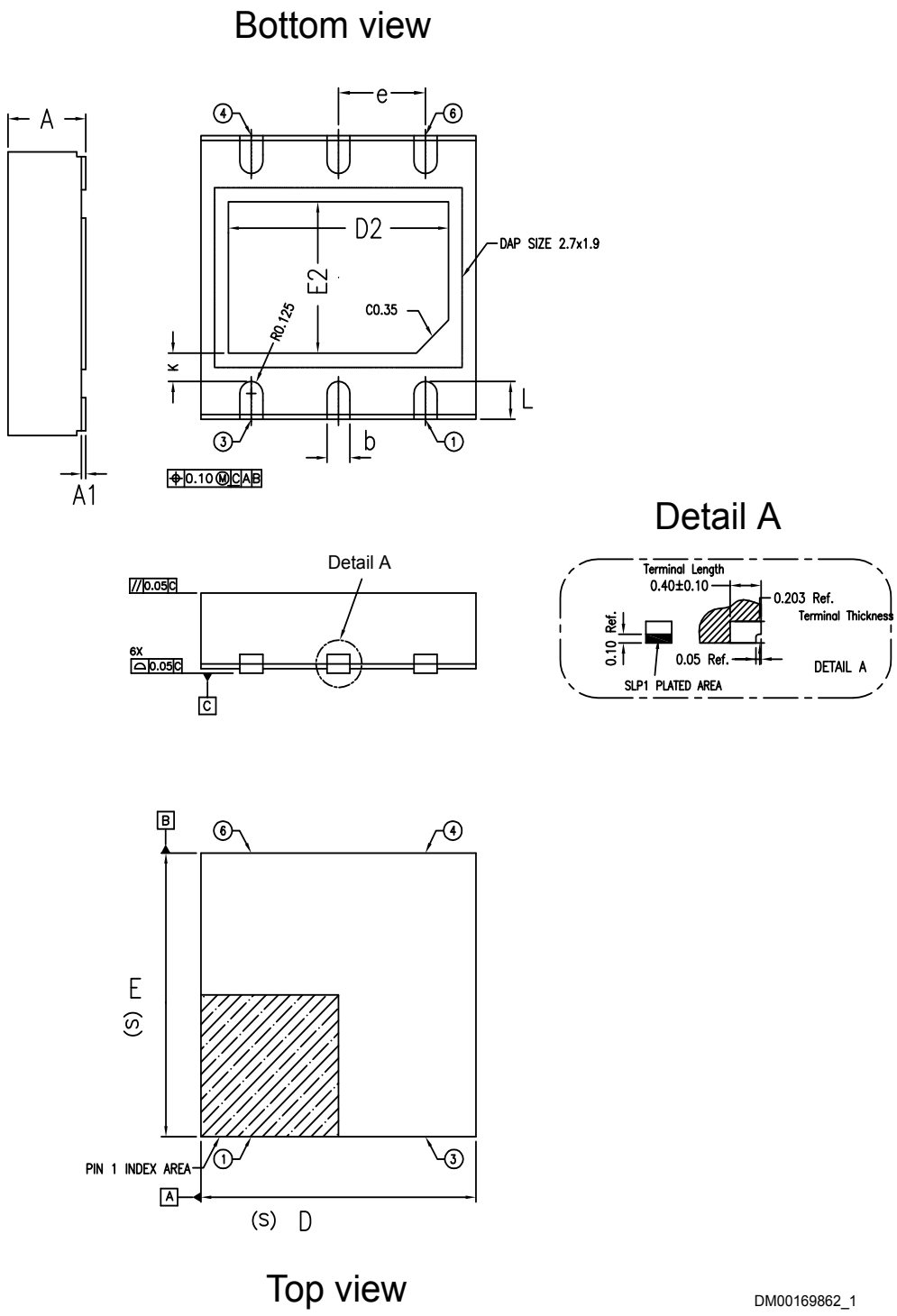
Figure 34. **DFN6 (3x3 mm) recommended footprint**



7946637_C

7.2 DFN6 (3x3 mm) automotive-grade package information

Figure 35. **DFN6 (3x3 mm) automotive-grade package outline**

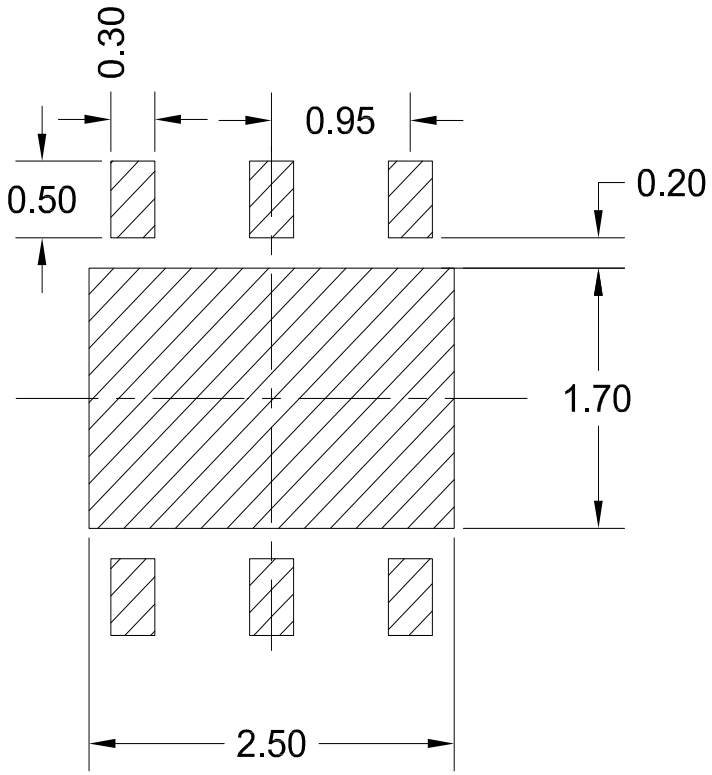


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Table 8. **DFN6 (3x3 mm) automotive-grade mechanical data**

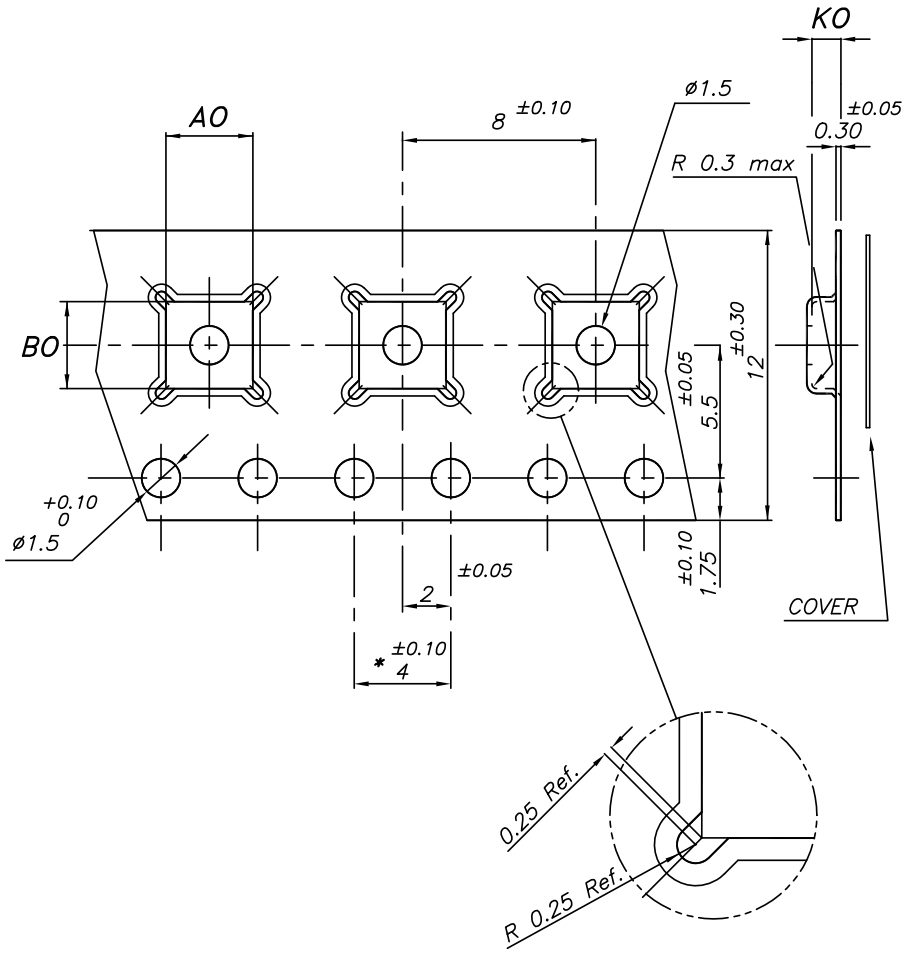
Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.85	0.90
A1	0.0		0.05
b	0.20	0.25	0.30
D	2.95	3.00	3.05
D2	2.30	2.40	2.50
e		0.95	
E	2.95	3.00	3.05
E2	1.50	1.60	1.70
L	0.30	0.40	0.50

Figure 36. **DFN6 (3x3 mm) automotive-grade recommended footprint**



7.3 DFN6 (3x3 mm) packing information

Figure 37. **DFN6 (3x3) tape outline**



– * 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.20

7875978_N

Figure 38. **DFN6 (3x3 mm) reel outline**

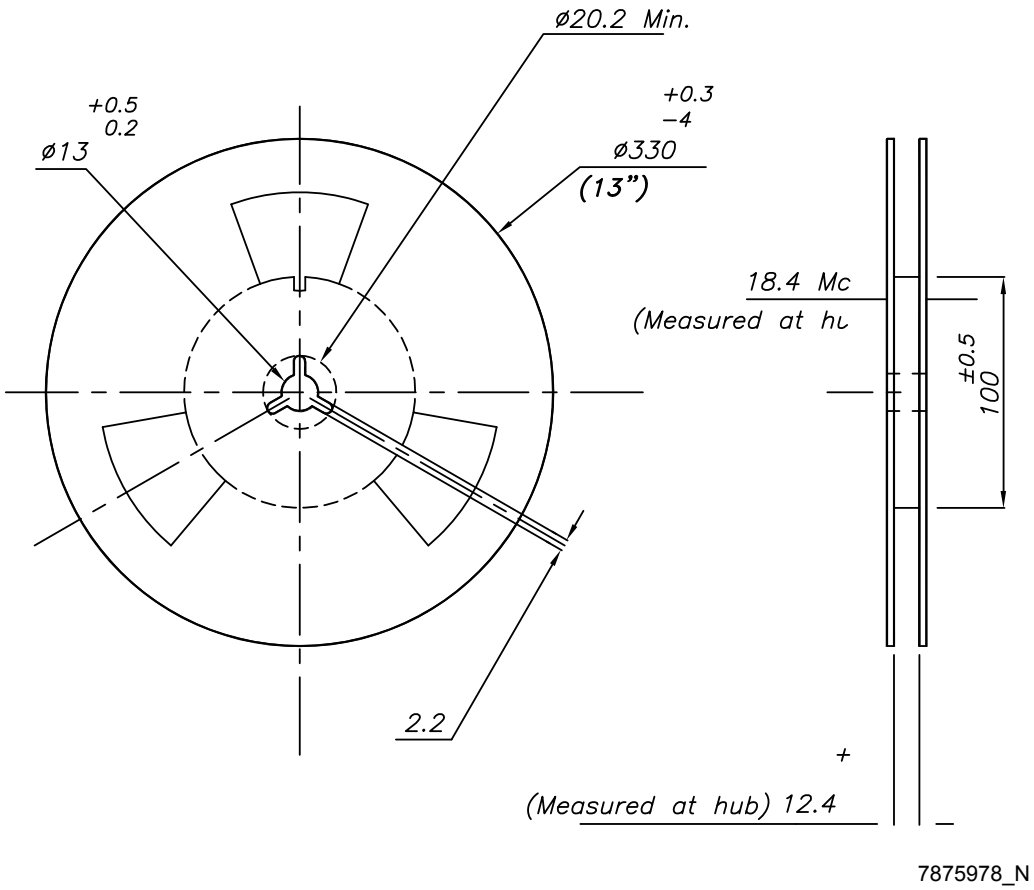


Table 9. **DFN6 (3x3) tape and reel mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A0	3.20	3.30	3.40
B0	3.20	3.30	3.40
K0	1	1.10	1.20

8 Ordering information

Table 10. Order code

Order code		Output voltage
Industrial grade	Automotive grade (1)	
LD39100PUR	LD39100PURY	Adj. from 0.8 V
LD39100PU12R	LD39100PU12RY	1.2 V
LD39100PU18R	LD39100PU18RY	1.8 V
LD39100PU25R	LD39100PU25RY	2.5 V
LD39100PU30R		3.0 V
LD39100PU33R	LD39100PU33RY	3.3 V

1. *Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q002 or equivalent.*

Revision history

Table 11. **Document revision history**

Date	Revision	Changes
29-Jul-2009	1	Initial release.
16-Apr-2010	2	Modified Figure 8 on page 9.
11-Oct-2011	3	Document status promoted from preliminary data to datasheet.
24-Apr-2014	4	Part numbers LD39100xx, LD39100xx12 and LD39100xx25 changed to LD39100. Updated Table 1: Device summary. Updated the description in cover page Section 1: Circuit schematics, Section 2: Pin configuration, Section 4: Electrical characteristics, Section 5: Typical performance characteristics, Figure 32: Typical application circuit for fixed output version, Section 7: Package mechanical data. Deleted previous Section 8: Different output voltage versions of the LD39100xx available on request. Added Section 8: Packaging mechanical data. Minor text changes.
01-Sep-2015	5	Updated Figure 32: Typical application circuit for fixed output version. Minor text changes.
20-Jun-2016	6	Updated features in cover page. Removed Table 1: Device summary. Updated Section 6.2: "Enable function". Added Section 8: "Ordering information" and Section 7.1: "DFN6 (3x3 mm) package information". Minor text changes.
23-Oct-2017	7	In Table 5: "LD39100 electrical characteristics (adjustable version)": - Updated I_{SC} typ. value (was 1.5) Table 6: "LD39100 electrical characteristics (fixed version)": - Updated I_{SC} typ. value (was 1.5) Removed Figure 30: ESR required for stability with ceramic capacitors (V_{OUT} = 0.8 V) Removed Figure 31: ESR required for stability with ceramic capacitors (V_{OUT} = 2.5 V) Updated Section 6: "Application information" Added Section 6.1: "External capacitors"
09-Oct-2019	8	Updated Figure 7. Dropout voltage vs. temperature (V_{OUT} = 1.5 V)
02-Apr-2020	9	Updated EN value in Table 2

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