

# TPS3600D20, TPS3600D25, TPS3600D33, TPS3600D50 BATTERY-BACKUP SUPERVISORS FOR LOW-POWER PROCESSORS

SLVS336B – DECEMBER 2000 – REVISED JANUARY 2007

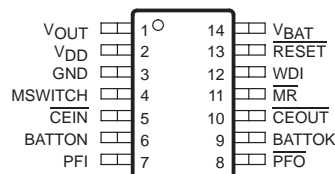
## features

- Supply Current of 40  $\mu$ A (Max)
- Precision Supply Voltage Monitor
  - 2.0 V, 2.5 V, 3.3 V, 5.0 V
  - Other Versions on Request
- Watchdog Timer With 800-ms Time-Out
- Backup-Battery Voltage Can Exceed  $V_{DD}$
- Power-On Reset Generator With Fixed 100-ms Reset Delay Time
- Battery OK Output
- Voltage Monitor for Power-Fail or Low-Battery Monitoring
- Manual Switchover to Battery-Backup Mode
- Chip-Enable Gating –3 ns (at  $V_{DD} = 5$  V)  
Max. Propagation Delay
- Manual Reset
- Battery Freshness Seal
- 14-Pin TSSOP Package
- Temperature Range . . .  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$

## typical applications

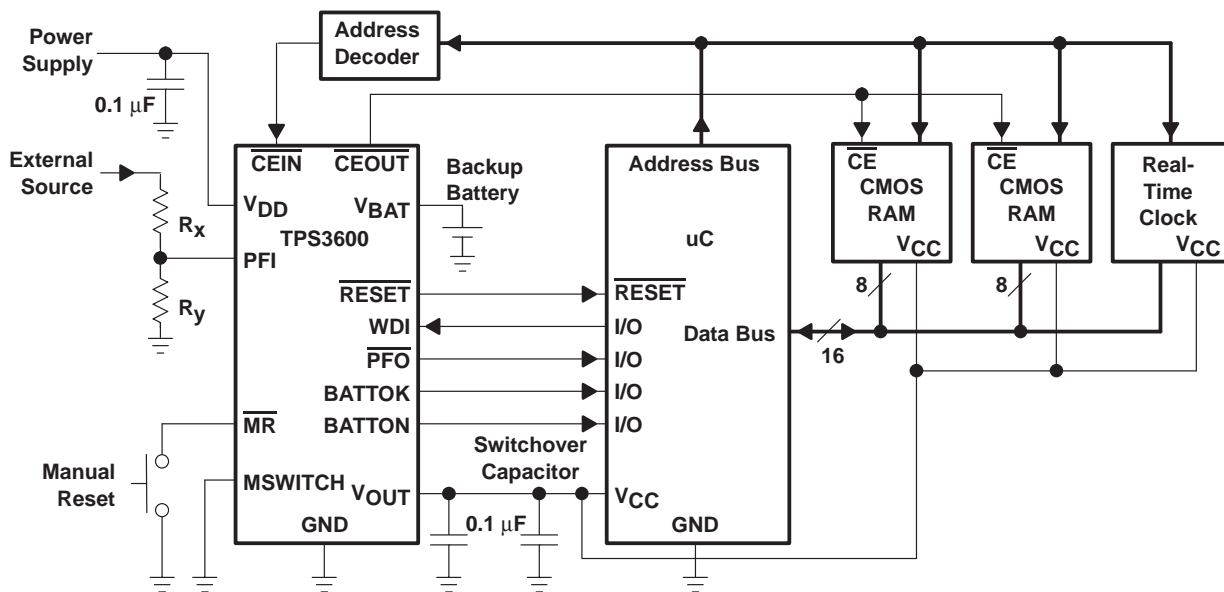
- Fax Machines
- Set-Top Boxes
- Advanced Voice Mail Systems
- Portable Battery Powered Equipment
- Computer Equipment
- Advanced Modems
- Automotive Systems
- Portable Long-Time Monitoring Equipment
- Point of Sale Equipment

TSSOP (PW) Package  
(TOP VIEW)



ACTUAL SIZE  
(5,10mm x 6,60mm)

## typical operating circuit



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# TPS3600D20, TPS3600D25, TPS3600D33, TPS3600D50 BATTERY-BACKUP SUPERVISORS FOR LOW-POWER PROCESSORS

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## description

The TPS3600 family of supervisory circuits monitor and control processor activity. In case of power-fail or brownout conditions, the backup-battery switchover function of TPS3600 allows to run a low-power processor and its peripherals from the installed backup battery without asserting a reset beforehand.

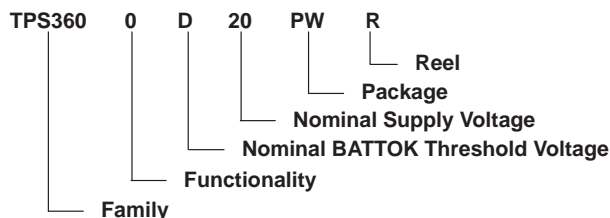
During power on,  $\overline{\text{RESET}}$  is asserted when the supply voltage ( $V_{\text{DD}}$  or  $V_{\text{BAT}}$ ) becomes higher than  $V_{\text{res}}$ . Thereafter, the supply voltage supervisor monitors  $V_{\text{OUT}}$  and keeps  $\overline{\text{RESET}}$  output active as long as  $V_{\text{OUT}}$  remains below the threshold voltage ( $V_{\text{IT}}$ ). An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. This delay timer starts its time-out, after  $V_{\text{OUT}}$  has risen above the threshold voltage ( $V_{\text{IT}}$ ). In case of a brownout or power failure of both supply sources, a voltage drop below the threshold voltage ( $V_{\text{IT}}$ ) get detected and the output becomes active (low) again.

The product spectrum is designed for supply voltages of 2 V, 2.5 V, 3.3 V, and 5 V. The circuits are available in a 14-pin TSSOP package. They are characterized for operation over a temperature range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

### PACKAGE INFORMATION

$T_A$	DEVICE NAME
$-40^{\circ}\text{C}$ to $85^{\circ}\text{C}$	TPS3600D20
	TPS3600D25
	TPS3600D33
	TPS3600D50

## ordering information application specific versions (see Note)



DEVICE NAME	NOMINAL VOLTAGE, $V_{\text{NOM}}$
TPS3600x20 PW	2.0 V
TPS3600x25 PW	2.5 V
TPS3600x33 PW	3.3 V
TPS3600x50 PW	5.0 V

DEVICE NAME	NOMINAL BATOK THRESHOLD VOLTAGE, $V_{\text{BOK}}$
TPS3600Dxx PW	$V_{\text{IT}} + 7\%$
TPS3600Fxx PW <sup>†</sup>	$V_{\text{IT}} + 6\%$
TPS3600Hxx PW <sup>†</sup>	$V_{\text{IT}} + 8\%$
TPS3600Jxx PW <sup>†</sup>	$V_{\text{IT}} + 10\%$

<sup>†</sup> For the application specific versions, please contact the local TI sales office for availability and lead time.

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FUNCTION TABLES

$V_{DD} > V_{SW}$	$V_{OUT} > V_{IT}$	$V_{DD} > V_{BAT}$	MSWITCH	$\overline{MR}$	$V_{OUT}$	BATTON	$\overline{RESET}$	$\overline{CEOUT}$
0	0	0	0	0	$V_{BAT}$	1	0	DIS
0	0	0	0	1	$V_{BAT}$	1	0	DIS
0	0	0	1	0	$V_{BAT}$	1	0	DIS
0	0	0	1	1	$V_{BAT}$	1	0	DIS
0	0	1	0	0	$V_{DD}$	0	0	DIS
0	0	1	0	1	$V_{DD}$	0	0	DIS
0	0	1	1	0	$V_{BAT}$	1	0	DIS
0	0	1	1	1	$V_{BAT}$	1	0	DIS
0	1	0	0	0	$V_{BAT}$	1	0	DIS
0	1	0	0	1	$V_{BAT}$	1	1	EN
0	1	0	1	0	$V_{BAT}$	1	0	DIS
0	1	0	1	1	$V_{BAT}$	1	1	EN
0	1	1	0	0	$V_{DD}$	0	0	DIS
0	1	1	0	1	$V_{DD}$	0	1	EN
0	1	1	1	0	$V_{BAT}$	1	0	DIS
0	1	1	1	1	$V_{BAT}$	1	1	EN
1	1	0	0	0	$V_{DD}$	0	0	DIS
1	1	0	0	1	$V_{DD}$	0	1	EN
1	1	0	1	0	$V_{BAT}$	1	0	DIS
1	1	0	1	1	$V_{BAT}$	1	1	EN
1	1	1	0	0	$V_{DD}$	0	0	DIS
1	1	1	0	1	$V_{DD}$	0	1	EN
1	1	1	1	0	$V_{BAT}$	1	0	DIS
1	1	1	1	1	$V_{BAT}$	1	1	EN

$V_{BAT} > V_{BOK}$	BATTOK
0	0
1	1

CONDITION:  $V_{OUT} > V_{DD(min)}$

$\overline{CEIN}$	$\overline{CEOUT}$
0	0
1	1

CONDITION: Enabled

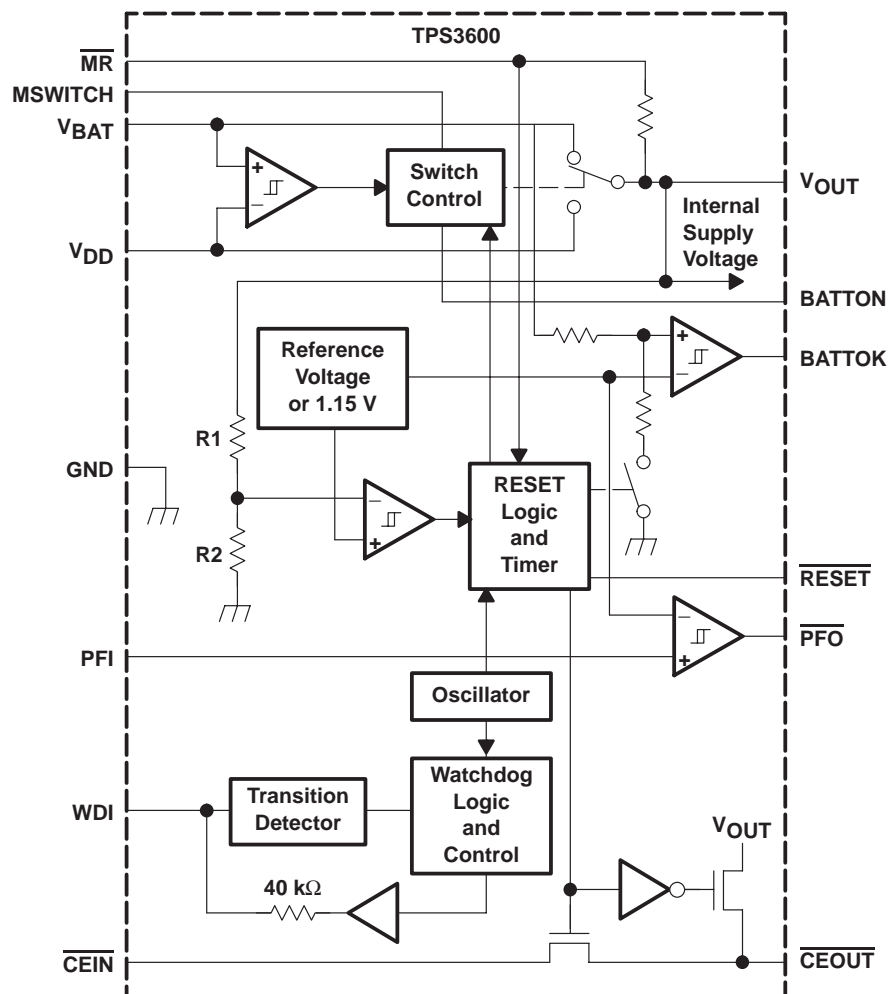
$PFI > V_{PFI}$	$\overline{PFO}$
0	0
1	1

CONDITION:  $V_{OUT} > V_{DD(min)}$

# TPS3600D20, TPS3600D25, TPS3600D33, TPS3600D50 BATTERY-BACKUP SUPERVISORS FOR LOW-POWER PROCESSORS

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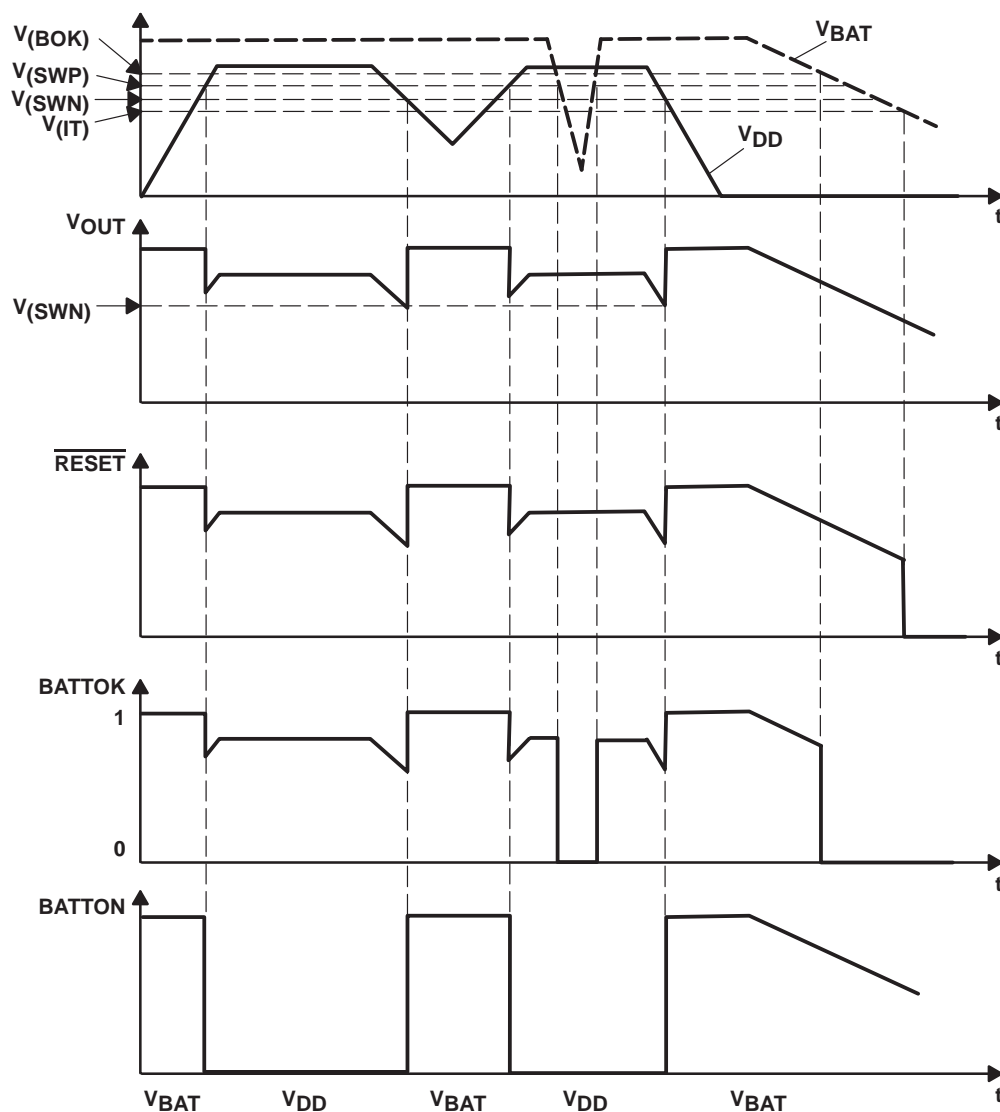
## functional schematic



# TPS3600D20, TPS3600D25, TPS3600D33, TPS3600D50 BATTERY-BACKUP SUPERVISORS FOR LOW-POWER PROCESSORS

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## timing diagram



NOTES: A. MSWITCH = 0,  $\overline{MR}$  = 1

NOTES: B. Timing diagram shown under normal operation, not in freshness seal mode.

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## Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
BATTOK	9	O	Battery status output
BATTON	6	O	Logic output/external bypass switch driver output
$\overline{\text{CEIN}}$	5	I	Chip-enable input
$\overline{\text{CEOUT}}$	10	O	Chip-enable output
GND	3	I	Ground
$\overline{\text{MR}}$	11	I	Manual reset input
MSWITCH	4	I	Manual switch to force device into battery-backup mode (connect to GND if not used)
PFI	7	I	Power-fail comparator input (connect to GND if not used)
$\overline{\text{PFO}}$	8	O	Power-fail comparator output
$\overline{\text{RESET}}$	13	O	Active-low reset output
$\text{VBAT}$	14	I	Backup-battery input
$\text{VDD}$	2	I	Input supply voltage
$\text{VOUT}$	1	O	Supply output
WDI	12	I	Watchdog timer input

## detailed description

### battery freshness seal

The battery freshness seal of the TPS3600 family disconnects the backup battery from the internal circuitry until it is needed. This ensures that the backup battery connected to  $\text{VBAT}$  should be fresh when the final product is put to use. The following steps explain how to enable the freshness seal mode:

1. Connect  $\text{VBAT}$  ( $\text{VBAT} > \text{VBAT}(\text{min})$ )
2. Ground  $\overline{\text{PFO}}$
3. Connect PFI to  $\text{VDD}$  or  $\text{PFI} > \text{V}(\text{PFI})$
4. Connect  $\text{VDD}$  to power supply ( $\text{VDD} > \text{VIT}$ )
5. Ground  $\overline{\text{MR}}$
6. Power down  $\text{VDD}$
7. The freshness seal mode is entered and pins  $\overline{\text{PFO}}$  and  $\overline{\text{MR}}$  can be disconnected.

The battery freshness seal mode is disabled by the positive-going edge of  $\overline{\text{RESET}}$  when  $\text{VDD}$  is applied.

### BATTOK output

This is a logic feedback of the device to indicate the status of the backup battery. The supervisor checks the battery voltage every 200 ms with a voltage divider load of approximately 100 K $\Omega$  and a measure cycle on-time of 25  $\mu\text{s}$ . This measurement cycle starts after the reset is released. If the battery voltage  $\text{VBAT}$  is below the negative-going threshold voltage  $\text{V}_{\text{BOK}}$ , the indicator BATTOK does a high-to-low transition. Otherwise, its status remains to the  $\text{V}_{\text{OUT}}$  level.

Table 1. Typical Values for BATTOK Indication

SUPERVISOR TYPE	$\text{VIT}$ TYP	$\text{V}_{\text{BOK}}$ MIN	$\text{V}_{\text{BOK}}$ TYP	$\text{V}_{\text{BOK}}$ MAX
TPS3600D20	1.78 V	1.84 V	1.91 V	1.97 V
TPS3600D25	2.22 V	2.3 V	2.38 V	2.46 V
TPS3600D33	2.93 V	3.04 V	3.14 V	3.24 V
TPS3600D50	4.40 V	4.56 V	4.71 V	4.86 V

## detailed description (continued)

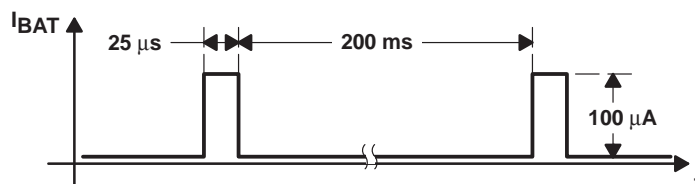


Figure 1. BATTOK Timing

## chip-enable signal gating

The internal gating of chip-enable signals (CE) prevents erroneous data from corrupting CMOS RAM during an under-voltage condition. The TPS3600 use a series transmission gate from  $\overline{\text{CEIN}}$  to  $\overline{\text{CEOUT}}$ . During normal operation (reset not asserted), the CE transmission gate is enabled and passes all CE transitions. When reset is asserted, this path becomes disabled, preventing erroneous data from corrupting the CMOS RAM. The short CE propagation delay from  $\overline{\text{CEIN}}$  to  $\overline{\text{CEOUT}}$  enables the TPS3600 devices to be used with most processors.

The CE transmission gate is disabled and  $\overline{\text{CEIN}}$  is high impedance (disable mode) while reset is asserted. During a power-down sequence when  $V_{DD}$  crosses the reset threshold, the CE transmission gate will be disabled and  $\overline{\text{CEIN}}$  immediately becomes high impedance if the voltage at  $\overline{\text{CEIN}}$  is high. If  $\overline{\text{CEIN}}$  is low during reset is asserted, the CE transmission gate will be disabled same time when  $\overline{\text{CEIN}}$  goes high, or 15  $\mu\text{s}$  after reset asserts, whichever occurs first. This will allow the current write cycle to complete during power down. When the CE transmission gate is enabled, the impedance of  $\overline{\text{CEIN}}$  appears as a resistor in series with the load at  $\overline{\text{CEOUT}}$ . The overall device propagation delay through the CE transmission gate depends on  $V_{OUT}$ , the source impedance of the device connected to  $\overline{\text{CEIN}}$  and the load at  $\overline{\text{CEOUT}}$ . To achieve minimum propagation delay, the capacitive load at  $\overline{\text{CEOUT}}$  should be minimized, and a low-output-impedance driver be used.

During disable mode, the transmission gate is off and an active pullup connects  $\overline{\text{CEOUT}}$  to  $V_{OUT}$ . This pullup turns off when the transmission gate is enabled.

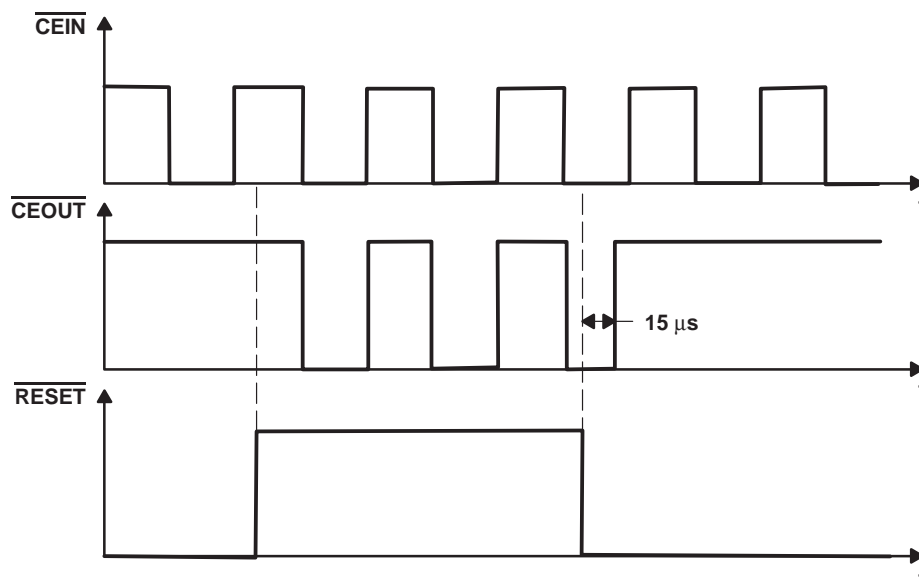


Figure 2. Chip-Enable Timing

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## detailed description (continued)

### power-fail comparator (PFI and $\overline{\text{PFO}}$ )

An additional comparator is provided to monitor voltages other than the nominal supply voltage. The power-fail input (PFI) will be compared with an internal voltage reference of 1.15 V. If the input voltage falls below the power-fail threshold,  $V_{(\text{PFI})}$ , of 1.15 V typical, the power-fail output ( $\overline{\text{PFO}}$ ) goes low. If it goes above  $V_{(\text{PFI})}$  plus about 12-mV hysteresis, the output returns to high. By connecting two external resistors, it is possible to supervise any voltages above  $V_{(\text{PFI})}$ . The sum of both resistors should be about 1 M $\Omega$ , to minimize power consumption and also to ensure that the current in the PFI pin can be neglected compared with the current through the resistor network. The tolerance of the external resistors should be not more than 1% to ensure minimal variation of sensed voltage.

If the power-fail comparator is unused, connect PFI to ground and leave  $\overline{\text{PFO}}$  unconnected.

### BATTON

Most often BATTON is used as a gate drive for an external pass transistor for high-current applications. In addition it can be also used as a logic output to indicate the battery switchover status. BATTON is high when  $V_{\text{OUT}}$  is connected to  $V_{\text{BAT}}$ .

BATTON can be directly connected to the gate of a PMOS transistor (see Figure 3). No current-limiting resistor is required. When using a PMOS transistor, it must be connected backwards from the traditional method (see Figure 3). This method orients the body diode from  $V_{\text{DD}}$  to  $V_{\text{OUT}}$  and prevents the backup battery from discharging through the FET when its gate is high.

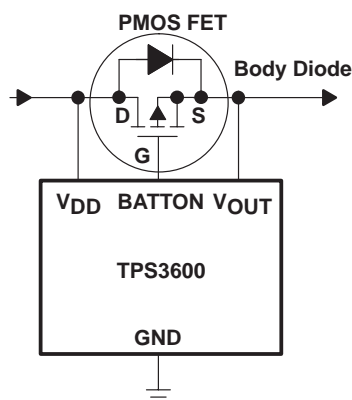


Figure 3. Driving an External MOSFET Transistor With BATTON

### backup-battery switchover

In the event of a brownout or power failure, it may be necessary to keep a processor running. If a backup battery is installed at  $V_{\text{BAT}}$ , the devices automatically connect the processor to backup power when  $V_{\text{DD}}$  fails. In order to allow the backup battery (e.g., a 3.6-V lithium cell) to have a higher voltage than  $V_{\text{DD}}$ , this family of supervisors will not connect  $V_{\text{BAT}}$  to  $V_{\text{OUT}}$  when  $V_{\text{BAT}}$  is greater than  $V_{\text{DD}}$ .  $V_{\text{BAT}}$  only connects to  $V_{\text{OUT}}$  (through a 2- $\Omega$  switch) when  $V_{\text{OUT}}$  falls below  $V_{(\text{SWN})}$  and  $V_{\text{BAT}}$  is greater than  $V_{\text{DD}}$ . When  $V_{\text{DD}}$  recovers, switchover is deferred either until  $V_{\text{DD}}$  crosses  $V_{\text{BAT}}$ , or when  $V_{\text{DD}}$  rises above the threshold  $V_{(\text{SWP})}$ . (See the timing diagram)

$V_{\text{DD}} > V_{\text{BAT}}$	$V_{\text{DD}} > V_{(\text{SW})}$	$V_{\text{OUT}}$
1	1	$V_{\text{DD}}$
1	0	$V_{\text{DD}}$
0	1	$V_{\text{DD}}$
0	0	$V_{\text{BAT}}$



## detailed description (continued)

### manual switchover (MSWITCH)

While operating in the normal mode from  $V_{DD}$ , the device can be manually forced to operate in the battery-backup mode by connecting MSWITCH to  $V_{DD}$ . The table below shows the different switchover modes.

	MSWITCH	STATUS
<b><math>V_{DD}</math> mode</b>	GND	$V_{DD}$ mode
	$V_{DD}$	Switch to battery-backup mode
<b>Battery-backup mode</b>	GND	Battery-backup mode
	$V_{DD}$	Battery-backup mode

If the manual switchover feature is not used, MSWITCH must be connected to ground.

### watchdog

In a microprocessor- or DSP-based system, it is not only important to supervise the supply voltage, it is also important to ensure the correct program execution. The task of a watchdog is to ensure that the program is not stalled in an indefinite loop. The microprocessor, microcontroller, or the DSP have to toggle the watchdog input within typically 0.8 s to avoid a time-out from occurring. Either a low-to-high or a high-to-low transition resets the internal watchdog timer. If the input is unconnected the watchdog is disabled and will be retriggered internally.

#### saving current while using the watchdog

The watchdog input is internally driven low during the first 7/8 of the watchdog time-out period, then momentarily pulses high, resetting the watchdog counter. For minimum watchdog input current (minimum overall power consumption), leave WDI low for the majority of the watchdog time-out period, pulsing it low-high-low once within 7/8 of the watchdog time-out period to reset the watchdog timer. If instead, WDI is externally driven high for the majority of the time-out period, a current of e.g.  $5\text{ V}/40\text{ k}\Omega \approx 125\text{ }\mu\text{A}$  can flow into WDI.

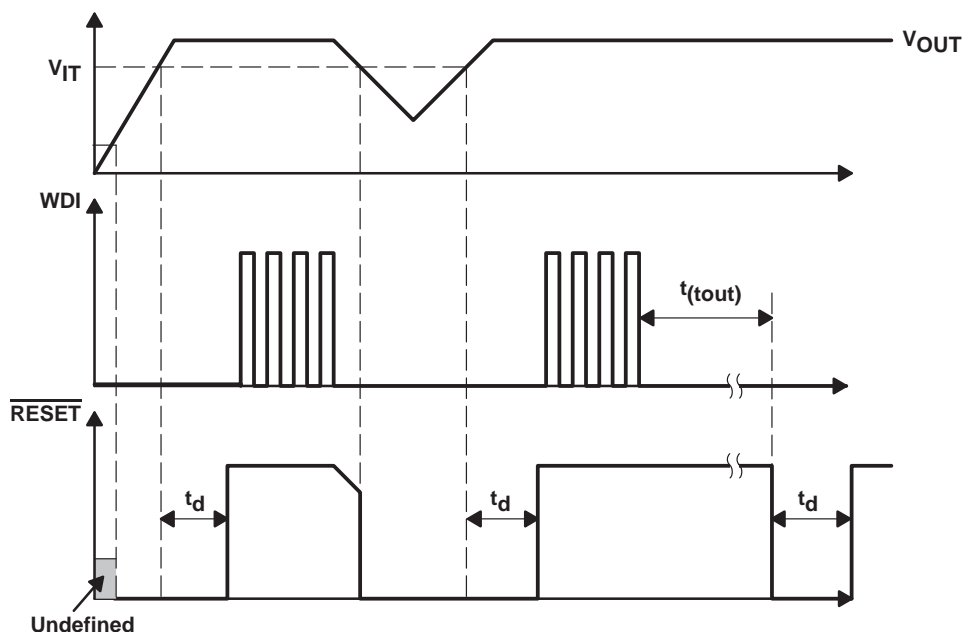


Figure 4. Watchdog Timing

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## absolute maximum ratings over operating free-air temperature (unless otherwise noted)<sup>†</sup>

Supply voltage: $V_{DD}$ (see Note1)	7 V
MR and WDI	–0.3 V to ( $V_{DD} + 0.3$ V)
All other pins (see Note 1)	–0.3 V to 7 V
Continuous output current at $V_{OUT}$ : $I_O$	300 mA
All other pins, $I_O$	±10 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$	–40°C to 85°C
Storage temperature range, $T_{stg}$	–65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds	260°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND. For reliable operation the device must not be operated at 7 V for more than  $t = 1000h$  continuously.

DISSIPATION RATING TABLE

PACKAGE	$T_A < 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
PW	700 mW	5.6 mW/°C	448 mW	364 mW

## recommended operating conditions at specified temperature range

	MIN	MAX	UNIT
Supply voltage, $V_{DD}$	1.65	5.5	V
Battery supply voltage, $V_{BAT}$	1.5	5.5	V
Input voltage, $V_I$	0	$V_{OUT} + 0.3$	V
High-level input voltage, $V_{IH}$	$0.7 \times V_{OUT}$		V
Low-level input voltage, all other pins, $V_{IL}$		$0.3 \times V_{OUT}$	V
Continuous output current at $V_{OUT}$ : $I_O$		200	mA
Input transition rise and fall rate at WDI, MSWITCH, $\Delta t/\Delta V$		100	ns/V
Slew rate at $V_{DD}$ or $V_{BAT}$		34	mV/μs
Operating free-air temperature range, $T_A$	–40	85	°C

# TPS3600D20, TPS3600D25, TPS3600D33, TPS3600D50

## BATTERY-BACKUP SUPERVISORS FOR LOW-POWER PROCESSORS

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### electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT	
V <sub>OH</sub>	High-level output voltage	RESET, BATTOK, BATTON	V <sub>OUT</sub> = 2.0 V, I <sub>OH</sub> = −400 μA	V <sub>OUT</sub> − 0.2 V			V	
			V <sub>OUT</sub> = 3.3 V, I <sub>OH</sub> = −2 mA	V <sub>OUT</sub> − 0.4 V				
			V <sub>OUT</sub> = 5.0 V, I <sub>OH</sub> = −3 mA					
		PFO	V <sub>OUT</sub> = 1.8 V, I <sub>OH</sub> = −20 μA	V <sub>OUT</sub> − 0.3 V				
			V <sub>OUT</sub> = 3.3 V, I <sub>OH</sub> = −80 μA	V <sub>OUT</sub> − 0.4 V				
			V <sub>OUT</sub> = 5.0 V, I <sub>OH</sub> = −120 μA					
		CEOUT Enable mode CEIN = V <sub>OUT</sub>	V <sub>OUT</sub> = 2.0 V, I <sub>OH</sub> = −1 mA	V <sub>OUT</sub> − 0.2 V				
			V <sub>OUT</sub> = 3.3 V, I <sub>OH</sub> = −2 mA	V <sub>OUT</sub> − 0.3 V				
			V <sub>OUT</sub> = 5.0 V, I <sub>OH</sub> = −5 mA					
		CEOUT Disable mode	V <sub>OUT</sub> = 3.3 V, I <sub>OH</sub> = −0.5 mA	V <sub>OUT</sub> − 0.4 V				
V <sub>OL</sub>	Low-level output voltage	RESET, PFO, BATTOK	V <sub>OUT</sub> = 2.0 V, I <sub>OL</sub> = 400 μA	0.2			V	
			V <sub>OUT</sub> = 3.3 V, I <sub>OL</sub> = 2 mA	0.4				
			V <sub>OUT</sub> = 5.0 V, I <sub>OL</sub> = 3 mA					
		BATTON	V <sub>OUT</sub> = 1.8 V, I <sub>OL</sub> = 500 μA	0.2				
			V <sub>OUT</sub> = 3.3 V, I <sub>OL</sub> = 3 mA	0.4				
			V <sub>OUT</sub> = 5.0 V, I <sub>OL</sub> = 5 mA					
		CEOUT Enable mode CEIN = 0 V	V <sub>OUT</sub> = 2.0 V, I <sub>OL</sub> = 1 mA	0.2				
			V <sub>OUT</sub> = 3.3 V, I <sub>OL</sub> = 2 mA	0.3				
			V <sub>OUT</sub> = 5.0 V, I <sub>OL</sub> = 5 mA					
			V <sub>res</sub>	Power-up reset voltage (see Note 2)	V <sub>BAT</sub> > 1.1 V OR V <sub>DD</sub> > 1.4 V, I <sub>OL</sub> = 20 μA	0.4		
V <sub>OUT</sub>	Normal mode		I <sub>O</sub> = 5 mA, V <sub>DD</sub> = 1.8 V	V <sub>DD</sub> − 50 mV			V	
			I <sub>O</sub> = 75 mA, V <sub>DD</sub> = 3.3 V	V <sub>DD</sub> − 150 mV				
			I <sub>O</sub> = 150 mA, V <sub>DD</sub> = 5 V	V <sub>DD</sub> − 250 mV				
	Battery-backup mode		I <sub>O</sub> = 4 mA, V <sub>BAT</sub> = 1.5 V	V <sub>BAT</sub> − 50 mV				
			I <sub>O</sub> = 75 mA, V <sub>BAT</sub> = 3.3 V	V <sub>BAT</sub> − 150 mV				
r <sub>ds(on)</sub>	V <sub>DD</sub> to V <sub>OUT</sub> on-resistance		V <sub>DD</sub> = 3.3 V	1	2	Ω		
	V <sub>BAT</sub> to V <sub>OUT</sub> on-resistance	V <sub>BAT</sub> = 3.3 V	1	2				
V <sub>IT</sub>	Negative-going input threshold voltage (see Notes 3 and 4)	TPS3600x20	T <sub>A</sub> = −40°C to 85°C	1.74	1.78	1.82	V	
		TPS3600x25		2.17	2.22	2.27		
		TPS3600x30		2.57	2.63	2.69		
		TPS3600x33		2.87	2.93	2.99		
		TPS3600x50		4.31	4.40	4.49		
		V(PFI)		PFI	1.13	1.15		1.17
		V(BOK)		TPS3600Dxx	V <sub>IT</sub> + 5.8%	V <sub>IT</sub> + 7.1%		V <sub>IT</sub> + 8.3%
V(SWN)	Battery switch threshold voltage negative-going V <sub>OUT</sub>		V <sub>IT</sub> + 1%	V <sub>IT</sub> + 2%	V <sub>IT</sub> + 3.2%	V		

- NOTES: 2. The lowest supply voltage at which  $\overline{\text{RESET}}$  becomes active.  $t_r(V_{DD}) \geq 15 \mu\text{s/V}$ .  
3. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic,  $0.1 \mu\text{F}$ ) should be placed near the supply terminal.  
4. Voltage is sensed at  $V_{OUT}$

# TPS3600D20, TPS3600D25, TPS3600D33, TPS3600D50

## BATTERY-BACKUP SUPERVISORS FOR LOW-POWER PROCESSORS

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electrical characteristics over recommended operating conditions (unless otherwise noted)  
(continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{hys}$	$V_{IT}$	$1.65\text{ V} < V_{IT} < 2.5\text{ V}$		20		mV
		$2.5\text{ V} < V_{IT} < 3.5\text{ V}$		40		
		$3.5\text{ V} < V_{IT} < 5.5\text{ V}$		50		
	BATTOK	$1.65\text{ V} < V_{(BOK)} < 2.5\text{ V}$		30		
		$2.5\text{ V} < V_{(BOK)} < 3.5\text{ V}$		60		
		$3.5\text{ V} < V_{(BOK)} < 5.5\text{ V}$		100		
	PFI			12		
	$V_{(BSW)}$	$V_{DD} = 1.8\text{ V}$		66		
	$V_{(SWN)}$	$1.65\text{ V} < V_{(SWN)} < 2.5\text{ V}$		85		
		$2.5\text{ V} < V_{(SWN)} < 3.5\text{ V}$		100		
		$3.5\text{ V} < V_{(SWN)} < 5.5\text{ V}$		110		
$I_{IH}$	High-level input current	WDI (see Note 5)	$WDI = V_{DD} = 5\text{ V}$		150	$\mu\text{A}$
		MR	$MR = 0.7 \times V_{DD}$ , $V_{DD} = 5\text{ V}$		-33 -76	
$I_{IL}$	Low-level input current	WDI (see Note 5)	$WDI = 0\text{ V}$ , $V_{DD} = 5\text{ V}$		-150	
		MR	$MR = 0\text{ V}$ , $V_{DD} = 5\text{ V}$		-110 -255	
$I_I$	Input current	PFI, MSWITCH	$V_I < V_{DD}$		-25 25	nA
$I_{OS}$	Short-circuit current	$\overline{PFO}$	$\overline{PFO} = 0\text{ V}$ , $V_{DD} = 1.8\text{ V}$		-0.3	mA
			$\overline{PFO} = 0\text{ V}$ , $V_{DD} = 3.3\text{ V}$		-1.1	
			$\overline{PFO} = 0\text{ V}$ , $V_{DD} = 5\text{ V}$		-2.4	
$I_{DD}$	$V_{DD}$ supply current	$V_{OUT} = V_{DD}$			40	$\mu\text{A}$
		$V_{OUT} = V_{BAT}$			8	
$I_{(BAT)}$	$V_{BAT}$ supply current	$V_{OUT} = V_{DD}$		-0.1	0.1	$\mu\text{A}$
		$V_{OUT} = V_{BAT}$			40	
$I_{lkg}$	CEIN leakage current	Disable mode, $V_I < V_{DD}$			$\pm 1$	$\mu\text{A}$
$C_i$	Input capacitance	$V_I = 0\text{ V to } 5.0\text{ V}$		5		pF

NOTE 5: For details on how to optimize current consumption when using WDI, see the detailed description section.

# TPS3600D20, TPS3600D25, TPS3600D33, TPS3600D50 BATTERY-BACKUP SUPERVISORS FOR LOW-POWER PROCESSORS

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timing requirements at  $R_L = 1\text{ M}\Omega$ ,  $C_L = 50\text{ pF}$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_w$	Pulse width	$V_{IH} = V_{IT} + 0.2\text{ V}$ , $V_{IL} = V_{IT} - 0.2\text{ V}$	5	1		$\mu\text{s}$
	$\overline{\text{MR}}$	$V_{DD} > V_{IT} + 0.2\text{ V}$ , $V_{IL} = 0.3 \times V_{DD}$ , $V_{IH} = 0.7 \times V_{DD}$	100			ns
	$\overline{\text{WDI}}$					

switching characteristics at  $R_L = 1\text{ M}\Omega$ ,  $C_L = 50\text{ pF}$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t <sub>d</sub>	Delay time	V <sub>DD</sub> ≥ V <sub>IT</sub> + 0.2 V, MR ≥ 0.7 × V <sub>DD</sub> , See timing diagram	60	100	140	ms	
t <sub>(tout)</sub>	Watchdog time-out	V <sub>DD</sub> > V <sub>IT</sub> + 0.2 V, See timing diagram	0.48	0.8	1.12	s	
t <sub>PLH</sub>	Propagation (delay) time, low-to-high-level output	50% $\overline{\text{RESET}}$ to 50% $\overline{\text{CEOUT}}$		15		μs	
t <sub>PHL</sub>	Propagation (delay) time, high-to-low-level output	V <sub>DD</sub> to $\overline{\text{RESET}}$		2	5	μs	
		PFI to $\overline{\text{PFO}}$		3	5	μs	
		$\overline{\text{MR}}$ to $\overline{\text{RESET}}$		0.1	1	μs	
		50% $\overline{\text{CEIN}}$ to 50% $\overline{\text{CEOUT}}$ CL = 50 pF only (see Note 6)	V <sub>DD</sub> = 1.8 V		5	15	ns
			V <sub>DD</sub> = 3.3 V		1.6	5	ns
			V <sub>DD</sub> = 5 V		1	3	ns
Transition time	V <sub>DD</sub> to BATTON	V <sub>IL</sub> = V <sub>BAT</sub> – 0.2 V, V <sub>IH</sub> = V <sub>BAT</sub> + 0.2 V, V <sub>(BAT)</sub> < V <sub>IT</sub>			3	μs	

NOTE 6: Ensured by design.

## TYPICAL CHARACTERISTICS

### Table of Graphs

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# TPS3600D20, TPS3600D25, TPS3600D33, TPS3600D50 BATTERY-BACKUP SUPERVISORS FOR LOW-POWER PROCESSORS

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## TYPICAL CHARACTERISTICS

STATIC DRAIN SOURCE ON-STATE RESISTANCE  
( $V_{DD}$  TO  $V_{OUT}$ )  
vs  
OUTPUT CURRENT

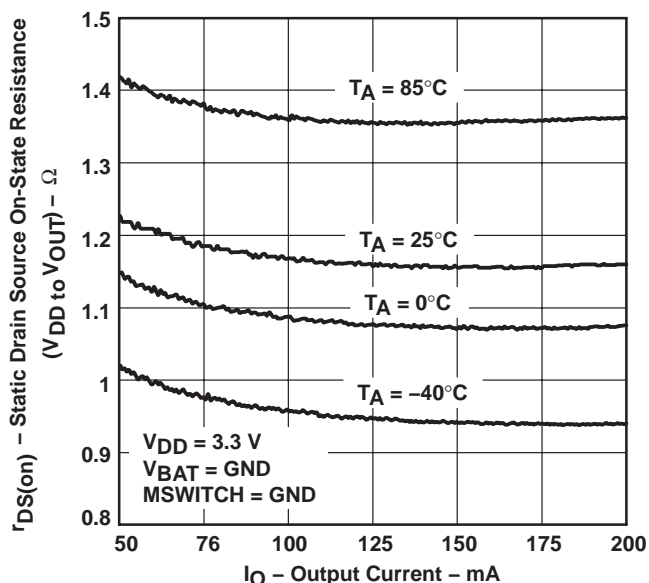


Figure 5

STATIC DRAIN SOURCE ON-STATE RESISTANCE  
( $V_{BAT}$  TO  $V_{OUT}$ )  
vs  
OUTPUT CURRENT

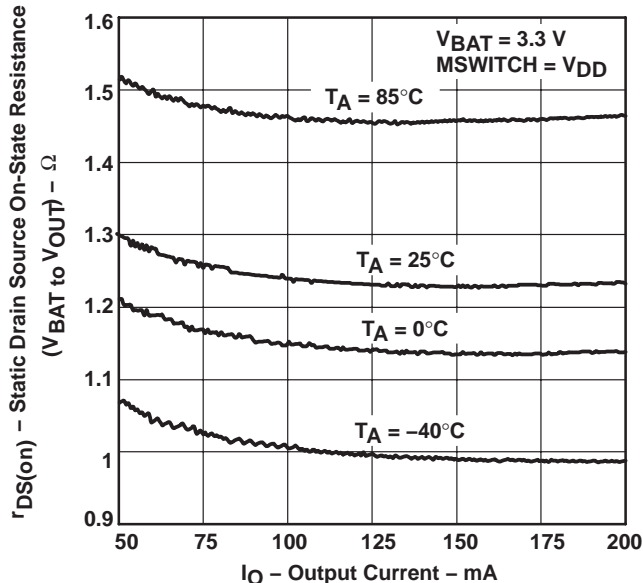


Figure 6

STATIC DRAIN SOURCE ON-STATE RESISTANCE  
( $\overline{CEIN}$  TO  $CEOUT$ )  
vs  
CHIP-ENABLE INPUT VOLTAGE

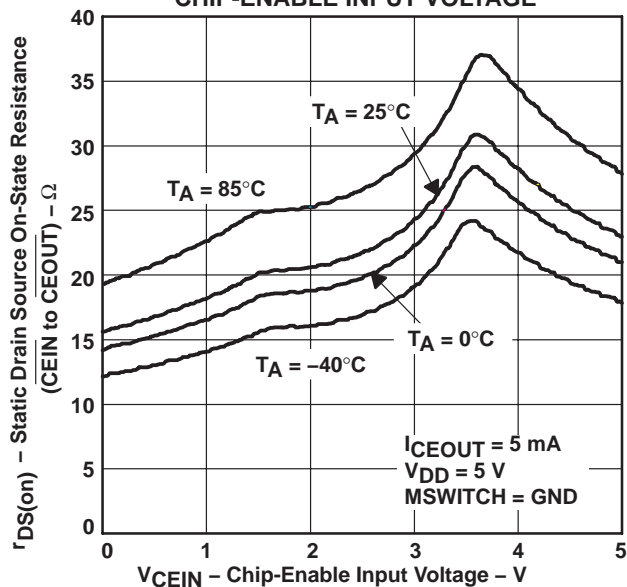


Figure 7

SUPPLY CURRENT  
vs  
SUPPLY VOLTAGE

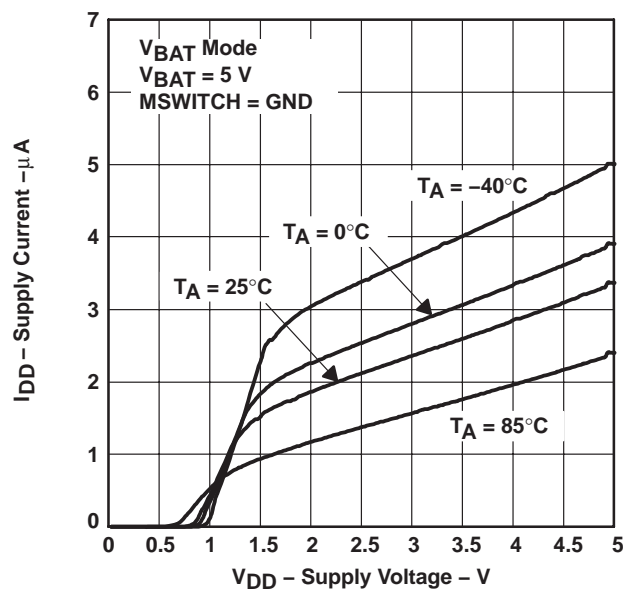
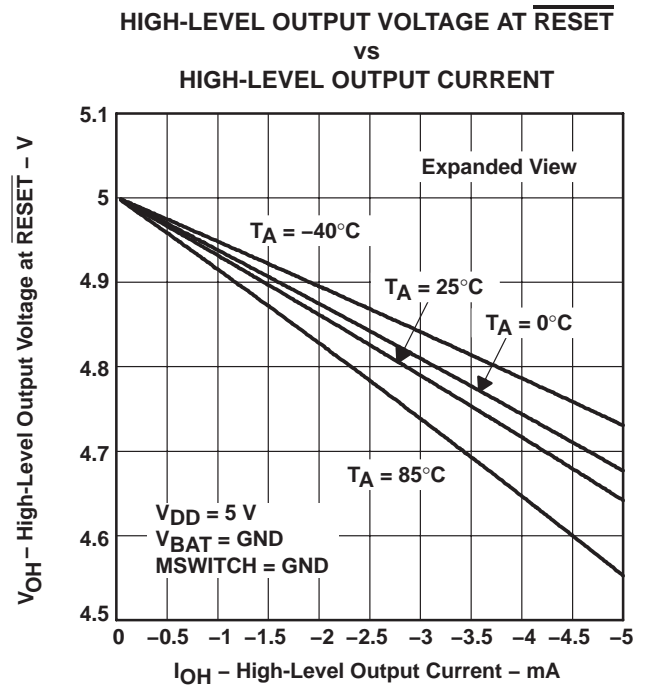
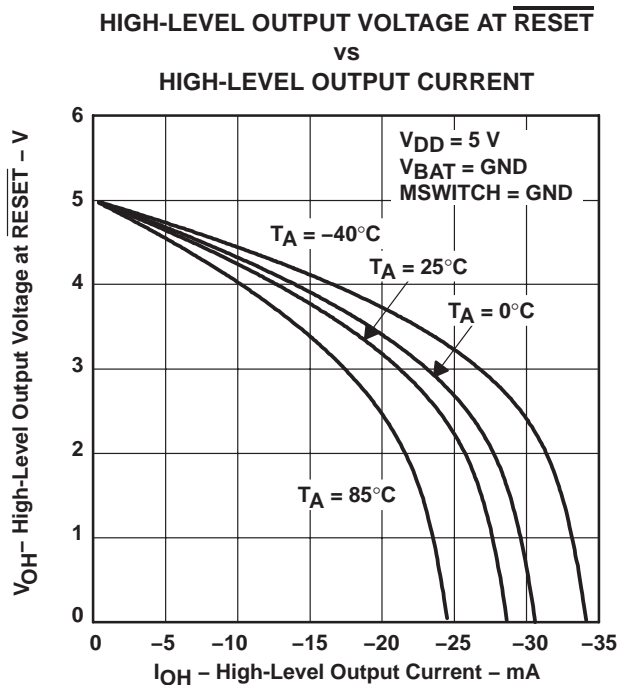
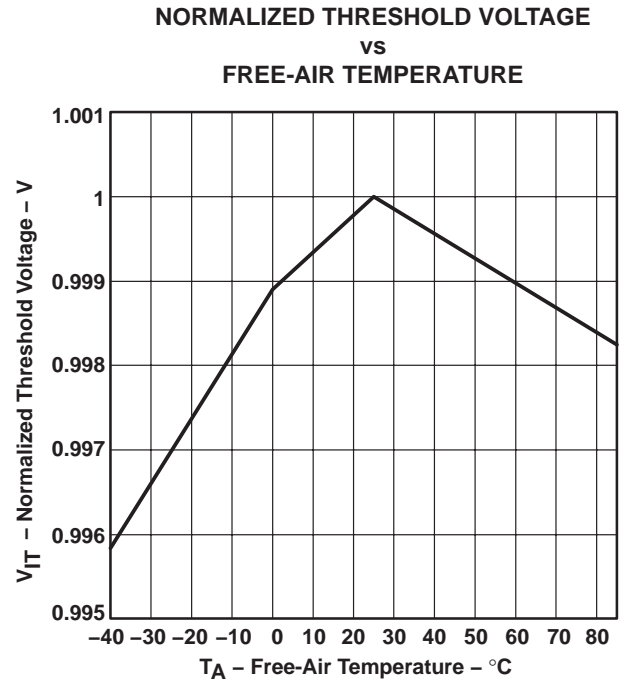
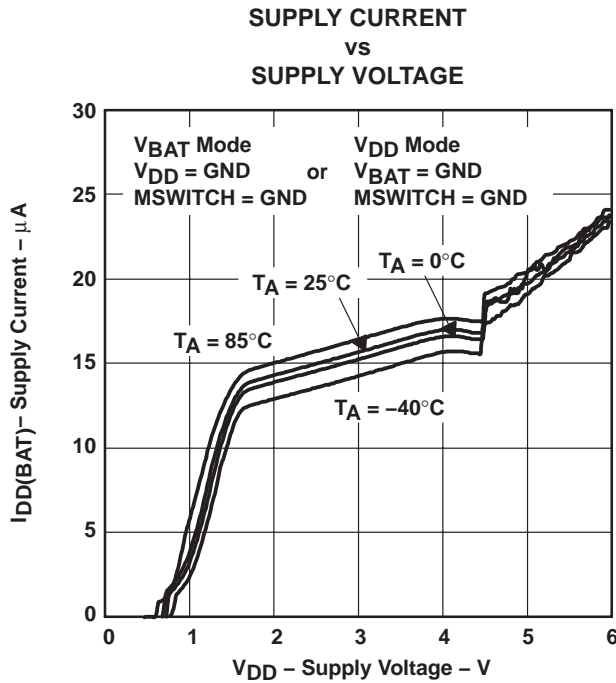


Figure 8

# TPS3600D20, TPS3600D25, TPS3600D33, TPS3600D50 BATTERY-BACKUP SUPERVISORS FOR LOW-POWER PROCESSORS

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## TYPICAL CHARACTERISTICS



# TPS3600D20, TPS3600D25, TPS3600D33, TPS3600D50 BATTERY-BACKUP SUPERVISORS FOR LOW-POWER PROCESSORS

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## TYPICAL CHARACTERISTICS

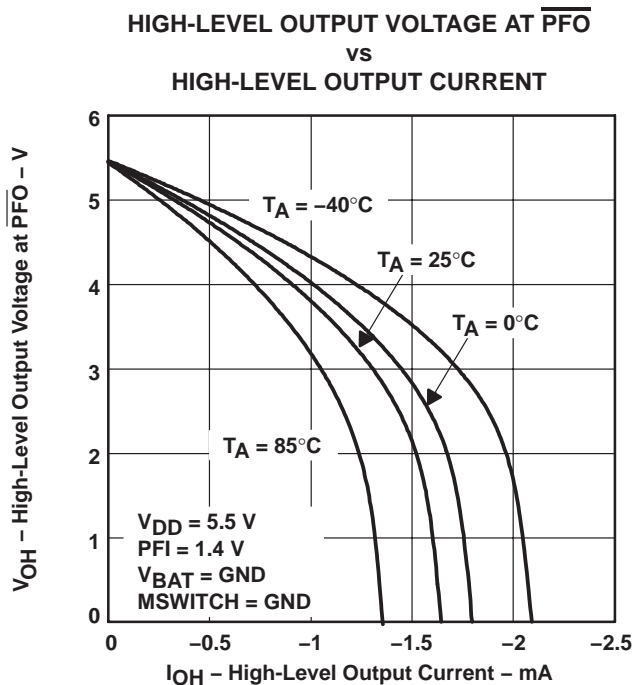


Figure 13

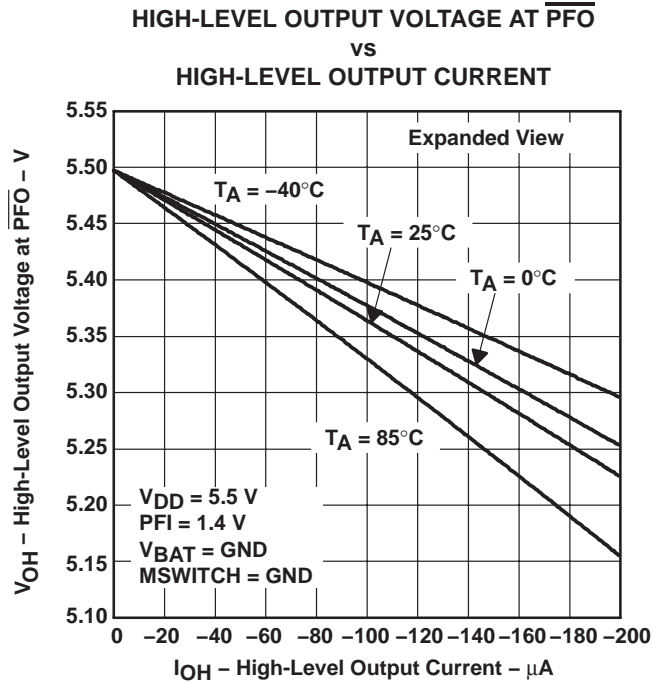


Figure 14

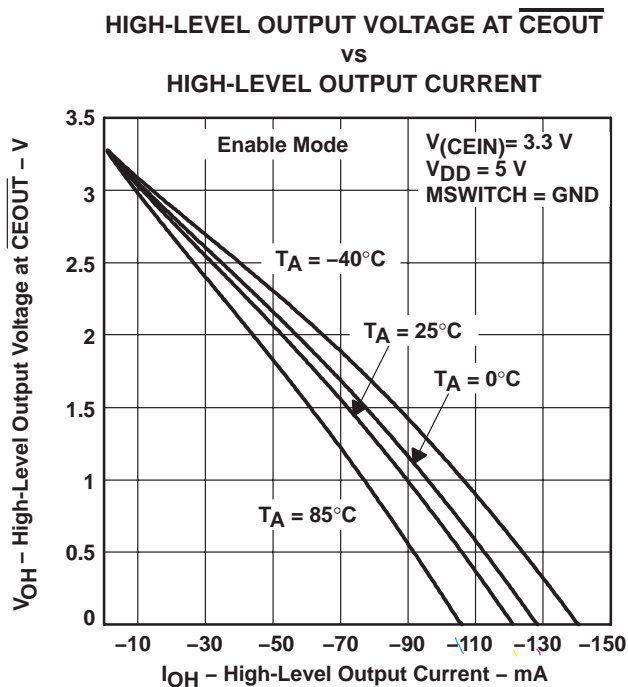


Figure 15

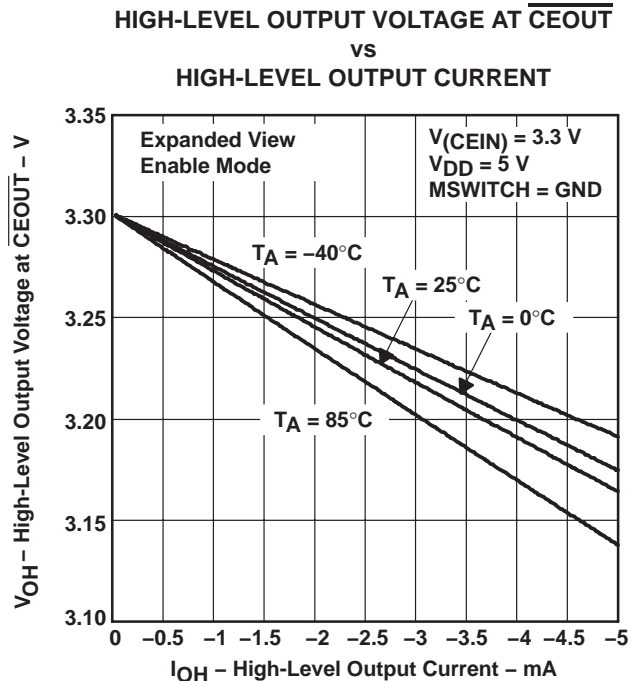
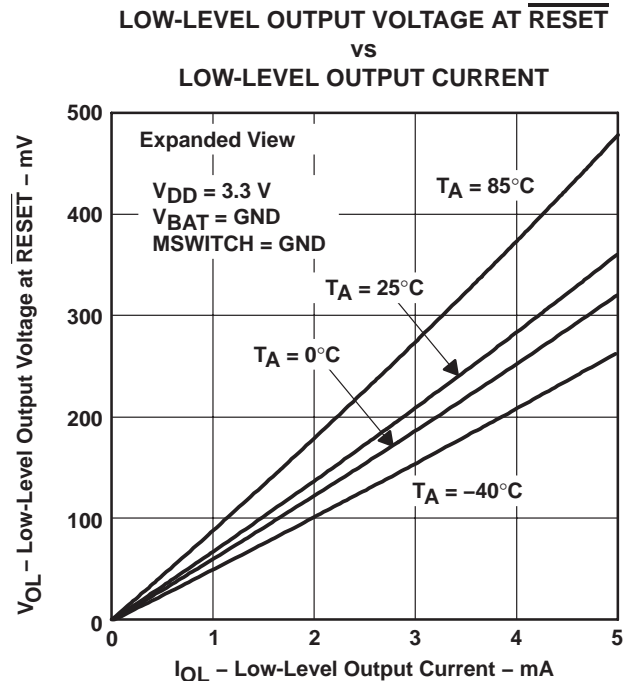
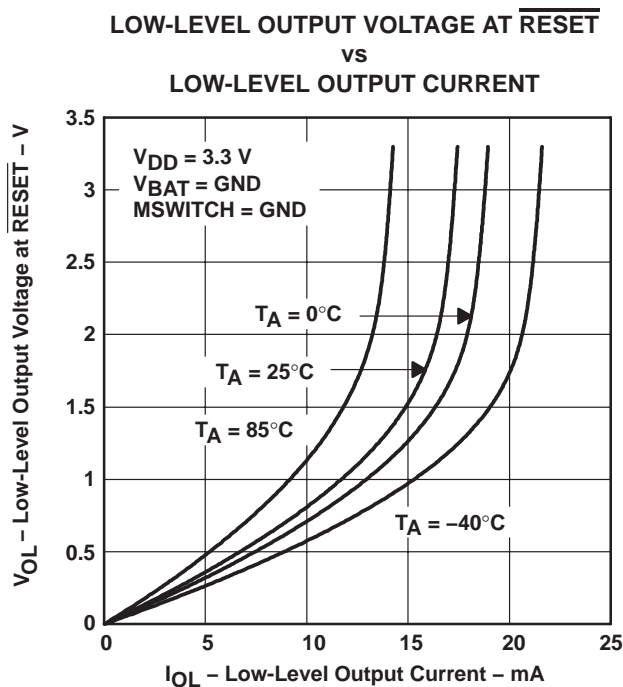
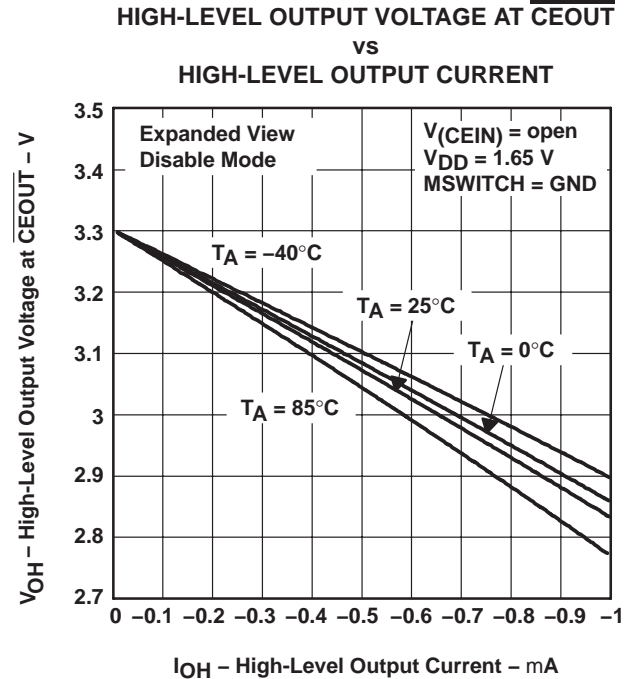
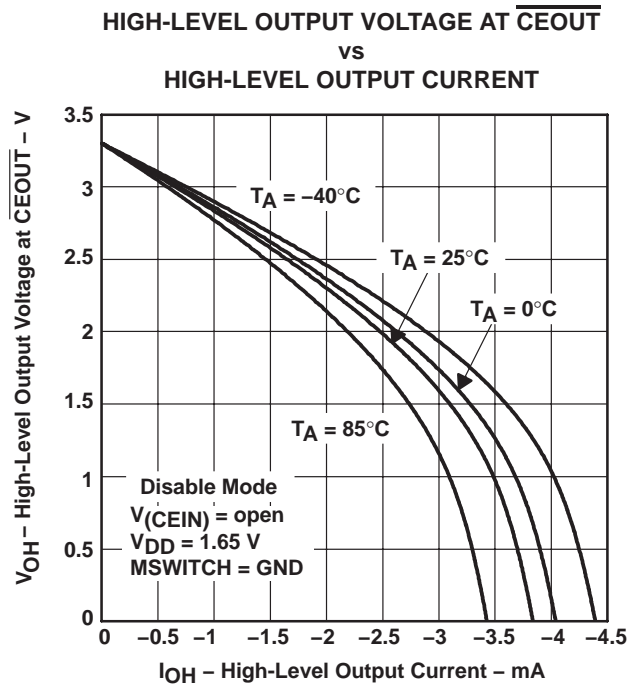


Figure 16



TYPICAL CHARACTERISTICS



# TPS3600D20, TPS3600D25, TPS3600D33, TPS3600D50 BATTERY-BACKUP SUPERVISORS FOR LOW-POWER PROCESSORS

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## TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE AT  $\overline{\text{CEOUT}}$   
vs  
LOW-LEVEL OUTPUT CURRENT

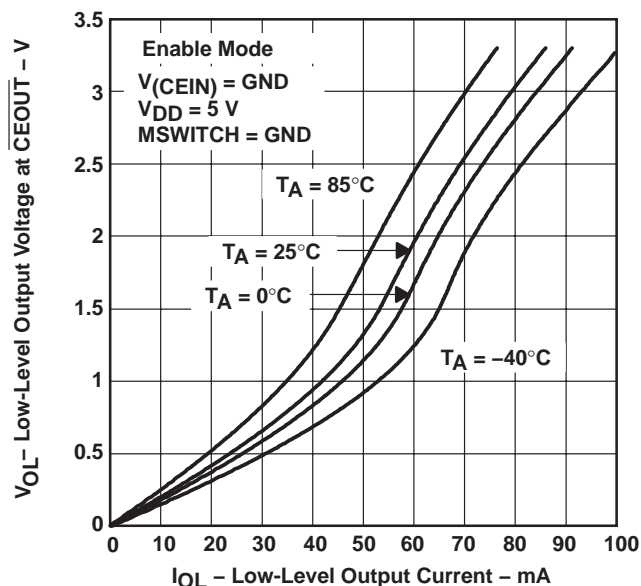


Figure 21

LOW-LEVEL OUTPUT VOLTAGE AT  $\overline{\text{CEOUT}}$   
vs  
LOW-LEVEL OUTPUT CURRENT

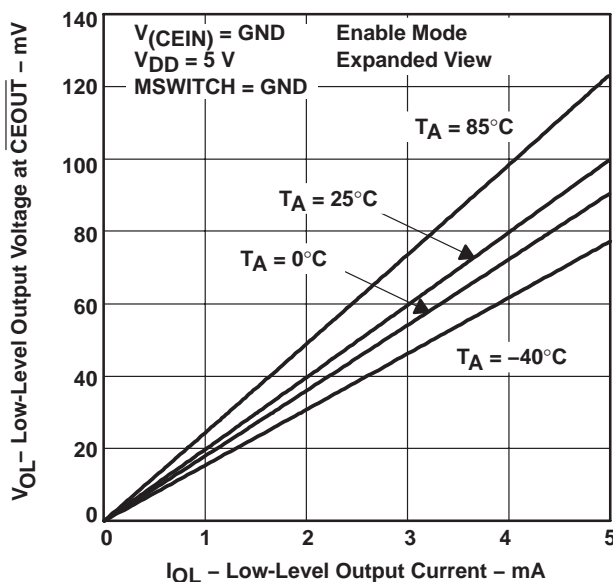


Figure 22

LOW-LEVEL OUTPUT VOLTAGE AT BATTON  
vs  
LOW-LEVEL OUTPUT CURRENT

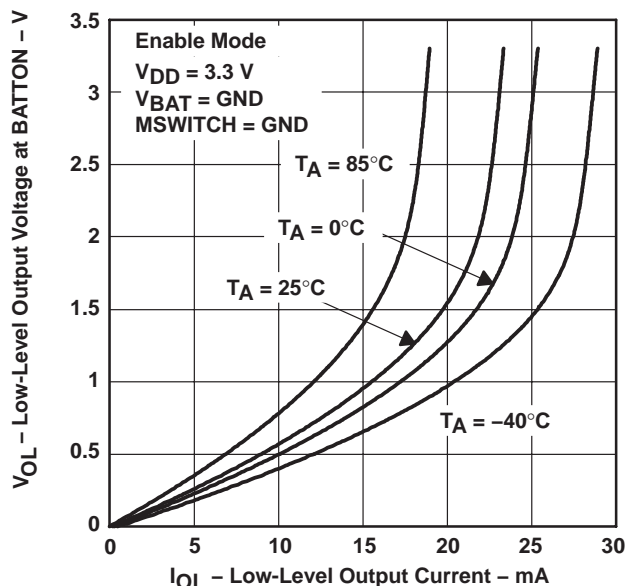


Figure 23

LOW-LEVEL OUTPUT VOLTAGE AT BATTON  
vs  
LOW-LEVEL OUTPUT CURRENT

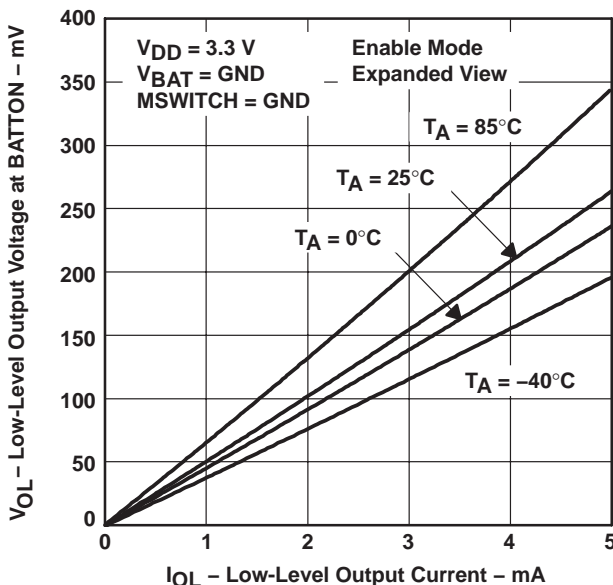


Figure 24

TYPICAL CHARACTERISTICS

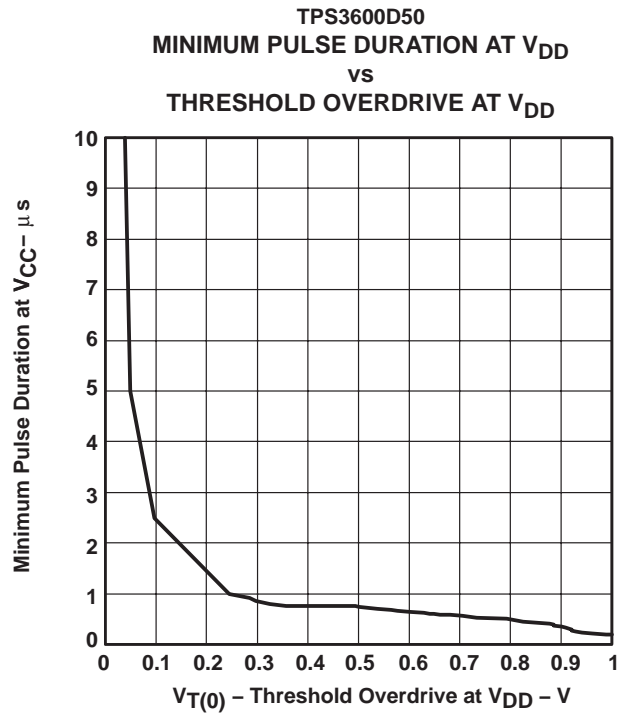


Figure 25

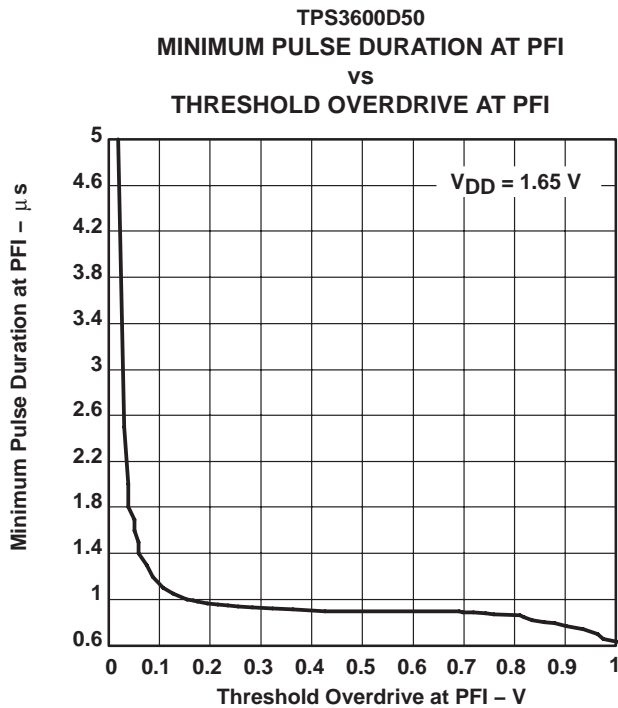


Figure 26

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TPS3600D20PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3600D20PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3600D20PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3600D20PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3600D25PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3600D25PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3600D25PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3600D25PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3600D33PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3600D33PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3600D33PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3600D33PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3600D50PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3600D50PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3600D50PWR	ACTIVE	TSSOP	PW	14		TBD	Call TI	Call TI
TPS3600D50PWRG4	ACTIVE	TSSOP	PW	14		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3600D20PWR	TSSOP	PW	14	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
TPS3600D25PWR	TSSOP	PW	14	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
TPS3600D33PWR	TSSOP	PW	14	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3600D20PWR	TSSOP	PW	14	2000	340.5	338.1	20.6
TPS3600D25PWR	TSSOP	PW	14	2000	340.5	338.1	20.6
TPS3600D33PWR	TSSOP	PW	14	2000	340.5	338.1	20.6

## PW (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153



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DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
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