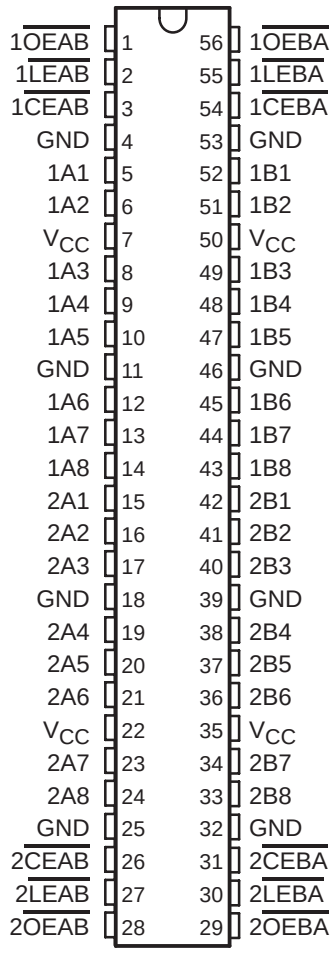
- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Members of the Texas Instruments *Widebus*™ Family**
- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Support Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Support Live Insertion**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54LVT16543 . . . WD PACKAGE
SN74LVT16543 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The ’LVT16543 are 16-bit registered transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{CEAB}$) input must be low in order to enter data from A or to output data from B. If $\overline{CEAB}$ is low and $\overline{LEAB}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

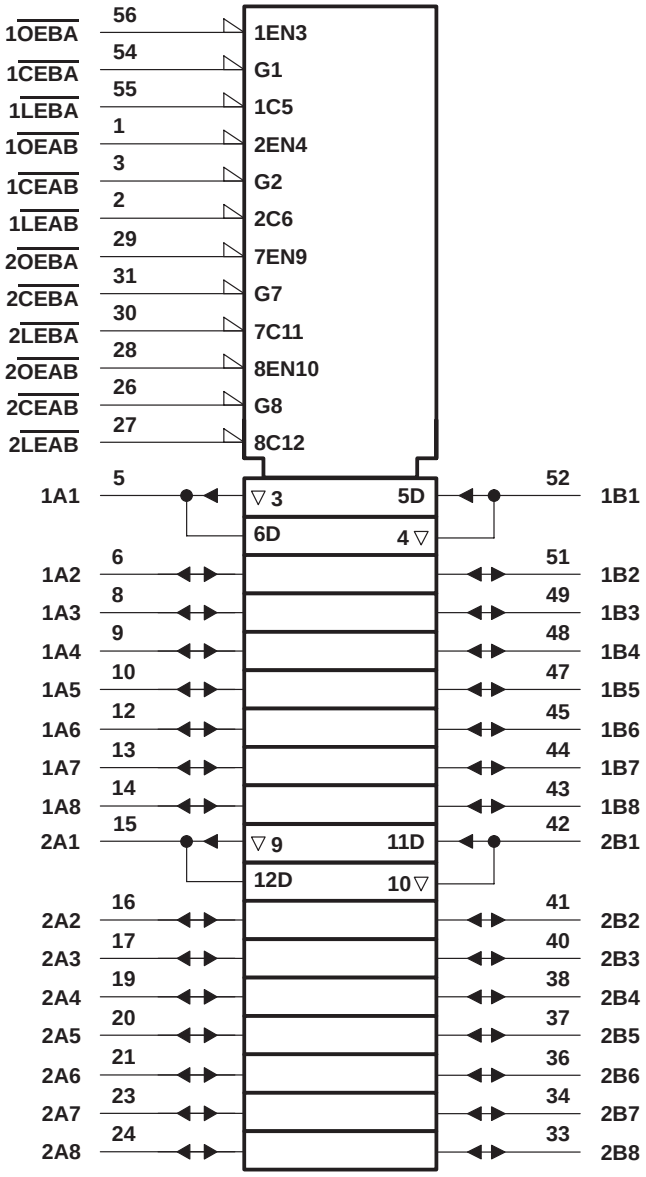
description (continued)

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT16543 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

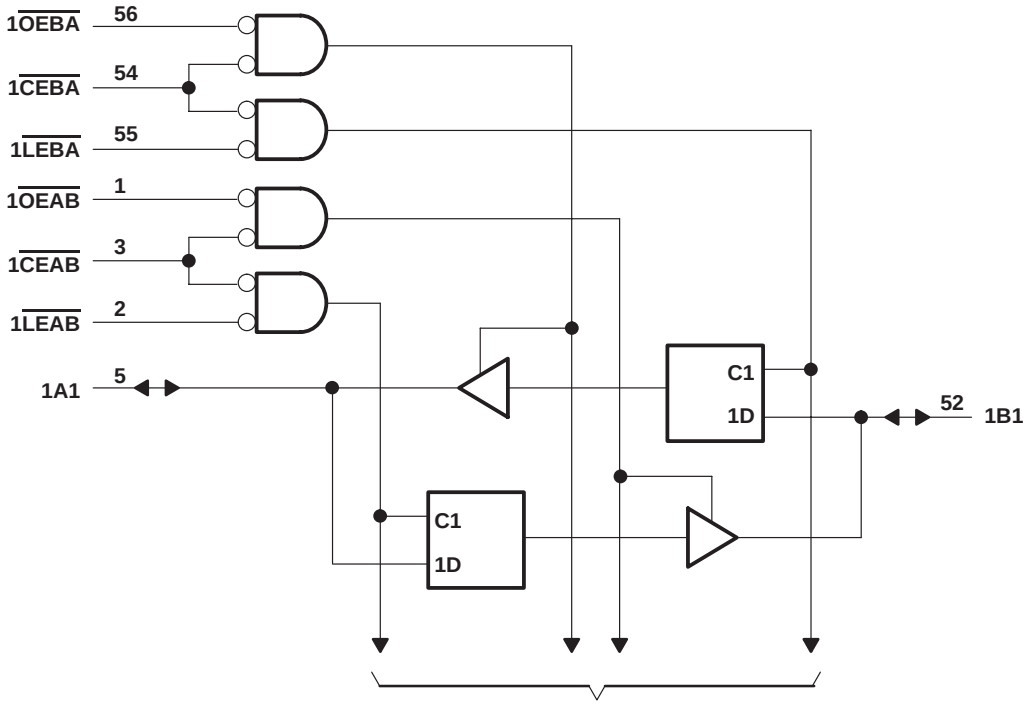
The SN54LVT16543 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LVT16543 is characterized for operation from −40°C to 85°C.

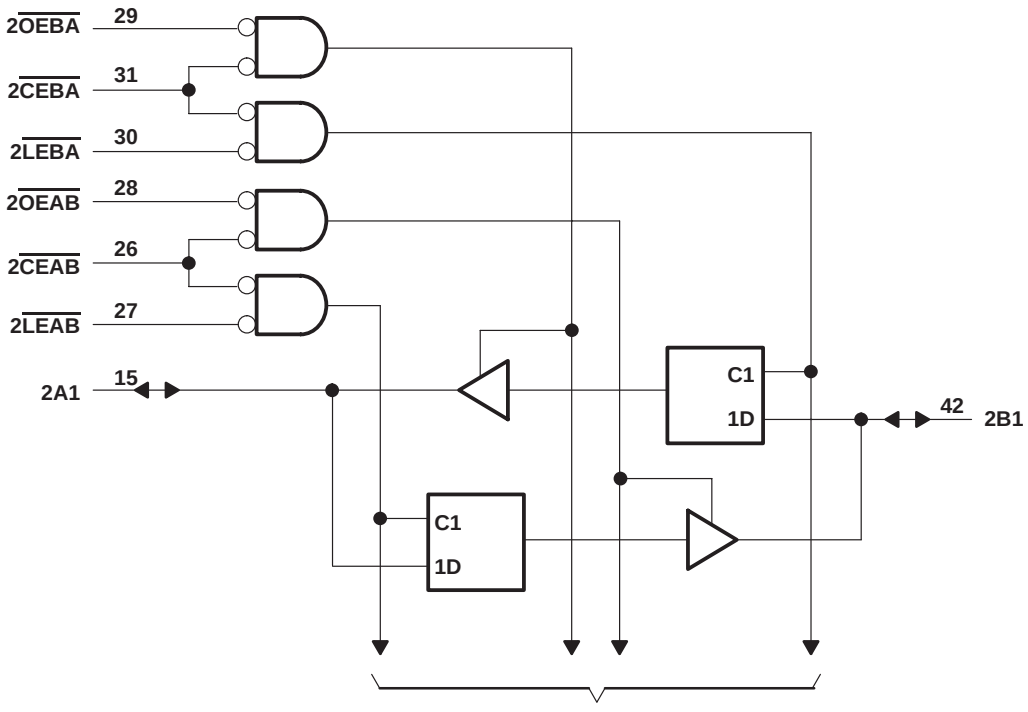
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





FUNCTION TABLE† (each 8-bit section)

INPUTS				OUTPUT
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A	B
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B_0‡
L	L	L	L	L
L	L	L	H	H

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.
‡ Output level before the indicated steady-state input conditions were established

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V_{CC} . . . . . −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . . −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) . . . . −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT16543 . . . . . 96 mA
SN74LVT16543 . . . . . 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT16543 . . . . . 48 mA
SN74LVT16543 . . . . . 64 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . −50 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package . . . . . 1 W
DL package . . . . . 1.4 W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

§ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 4)

			SN54LVT16543		SN74LVT16543		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT16543			SN74LVT16543			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = −100 µA		V_{CC} −0.2			V_{CC} −0.2			V
	V_{CC} = 2.7 V,	I_{OH} = − 8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = − 24 mA		2						
		I_{OH} = −32 mA					2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA				0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control inputs			±1			±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V	Control inputs			10			10	
	V_{CC} = 3.6 V	V_I = 5.5 V	A or B ports§			20			20	
		V_I = V_{CC}	A or B ports§			5			5	
		V_I = 0	A or B ports§			−10			−10	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			75			µA
		V_I = 2 V	A or B ports	−75			−75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				−1			−1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			0.12			0.12	mA
			Outputs low			5			5	
			Outputs disabled			0.12			0.12	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				0.2			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_{io}	V_O = 3 V or 0				13			13		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

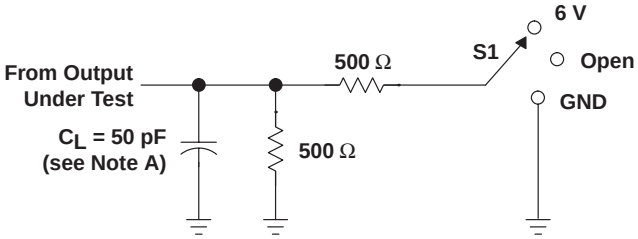
				SN54LVT16543				SN74LVT16543				UNIT
				V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, $\overline{LEAB}$ or $\overline{LEBA}$ low			3.3		3.3		3.3		3.3		ns
t_{su}	Setup time	A or B before $\overline{LEAB}$↑ or $\overline{LEBA}$↑	Data high	0.8		0.5		0.8		0.5		ns
			Data low	1.5		1.9		1.5		1.9		
		A or B before $\overline{CEAB}$↑ or $\overline{CEBA}$↑	Data high	0.7		0.4		0.7		0.4		ns
			Data low	1.6		1.9		1.6		1.9		
t_h	Hold time	A or B after $\overline{LEAB}$↑ or $\overline{LEBA}$↑	Data high	0.8		0		0.8		0		ns
			Data low	1.2		1.3		1.2		1.3		
		A or B after $\overline{CEAB}$↑ or $\overline{CEBA}$↑	Data high	0.8		0		0.8		0		ns
			Data low	1.3		1.4		1.3		1.4		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT16543				SN74LVT16543					UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.4	5		5.8	1.4	2.7	4.6		5.5	ns
t_{PHL}			1.3	4.7		5.9	1.3	2.9	4.6		5.8	
t_{PLH}	$\overline{LE}$	A or B	1.3	6.8		8.5	1.7	3.7	6.3		8.1	ns
t_{PHL}			1.5	6.5		8.3	1.9	3.7	6		7.8	
t_{PZH}	$\overline{OE}$	A or B	1.4	6		7.7	1.5	3.3	5.8		7.6	ns
t_{PZL}			1.6	6.3		8.4	1.6	3.3	6.2		8.2	
t_{PHZ}	$\overline{OE}$	A or B	2	6.7		7.3	2	4.1	6.5		7.1	ns
t_{PLZ}			2.7	6		6.2	2.7	3.9	5.8		5.9	
t_{PZH}	$\overline{CE}$	A or B	1.4	6.2		7.7	1.5	3.3	6		7.6	ns
t_{PZL}			1.6	6.6		8.5	1.7	3.3	6.4		8.3	
t_{PHZ}	$\overline{CE}$	A or B	2	6.6		7.2	2	4.1	6.4		7.1	ns
t_{PLZ}			2.6	5.6		5.9	2.6	4	5.4		5.6	

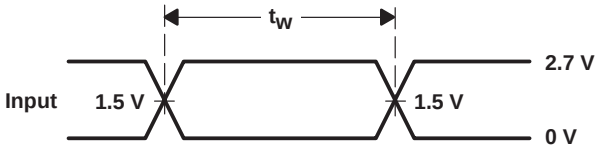
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

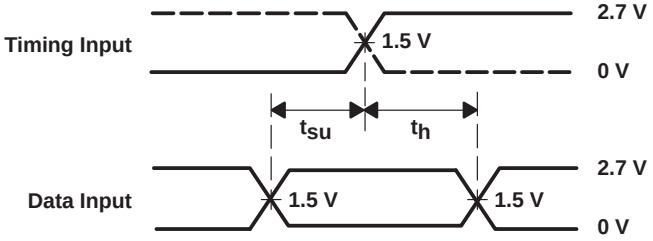


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

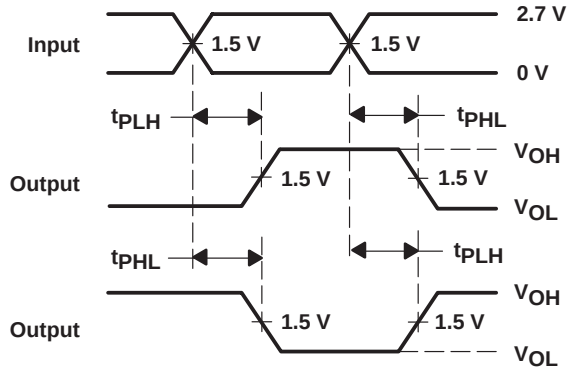
LOAD CIRCUIT FOR OUTPUTS



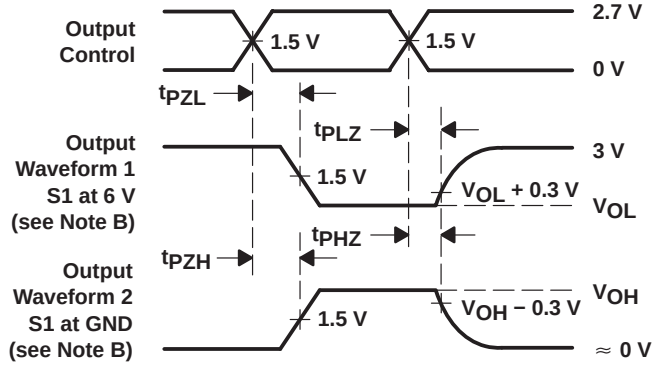
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVT16543DGGR	Active	Production	TSSOP (DGG) | 56	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT16543
SN74LVT16543DGGR.B	Active	Production	TSSOP (DGG) | 56	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT16543
SN74LVT16543DGGRG4	Active	Production	TSSOP (DGG) | 56	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT16543
SN74LVT16543DGGRG4.B	Active	Production	TSSOP (DGG) | 56	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT16543
SN74LVT16543DL	Active	Production	SSOP (DL) | 56	20 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT16543
SN74LVT16543DL.B	Active	Production	SSOP (DL) | 56	20 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT16543
SN74LVT16543DLG4	Active	Production	SSOP (DL) | 56	20 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT16543
SN74LVT16543DLG4.B	Active	Production	SSOP (DL) | 56	20 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT16543
SN74LVT16543DLR	Active	Production	SSOP (DL) | 56	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT16543
SN74LVT16543DLR.B	Active	Production	SSOP (DL) | 56	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT16543

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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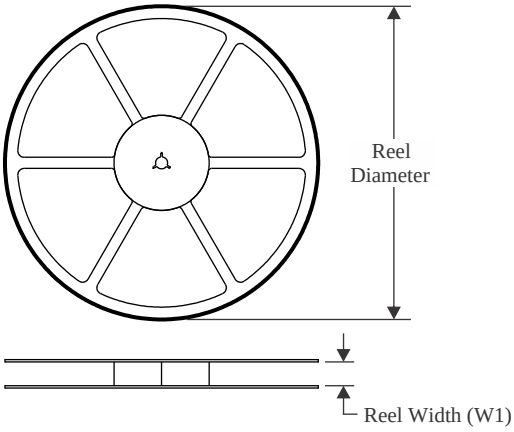
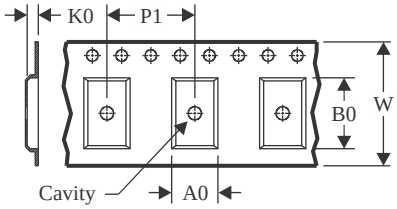
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

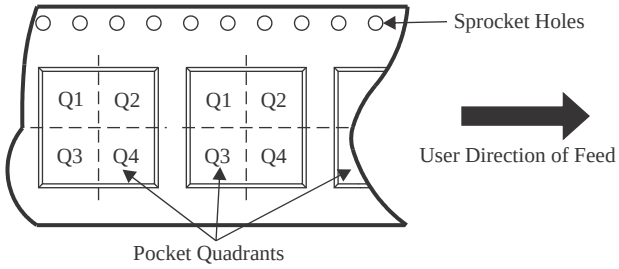


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

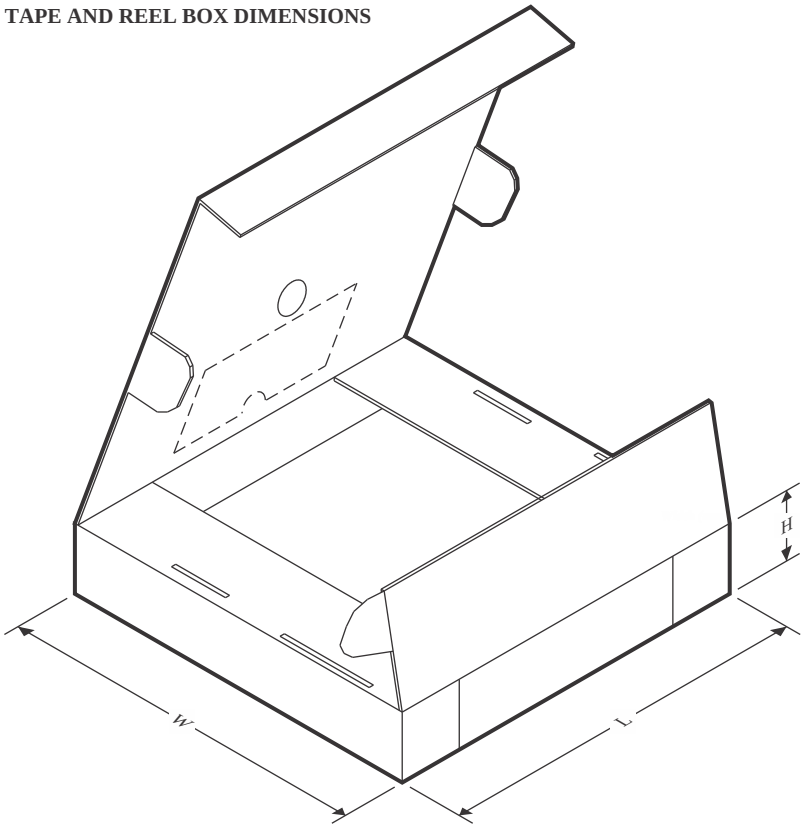
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVT16543DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1
SN74LVT16543DGGRG4	TSSOP	DGG	56	2000	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1
SN74LVT16543DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

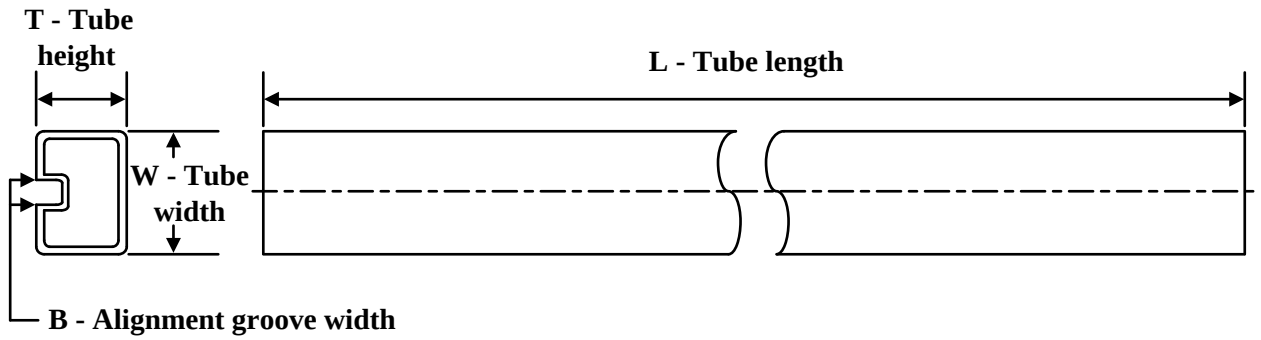
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVT16543DGGR	TSSOP	DGG	56	2000	356.0	356.0	45.0
SN74LVT16543DGGRG4	TSSOP	DGG	56	2000	356.0	356.0	45.0
SN74LVT16543DLR	SSOP	DL	56	1000	356.0	356.0	53.0

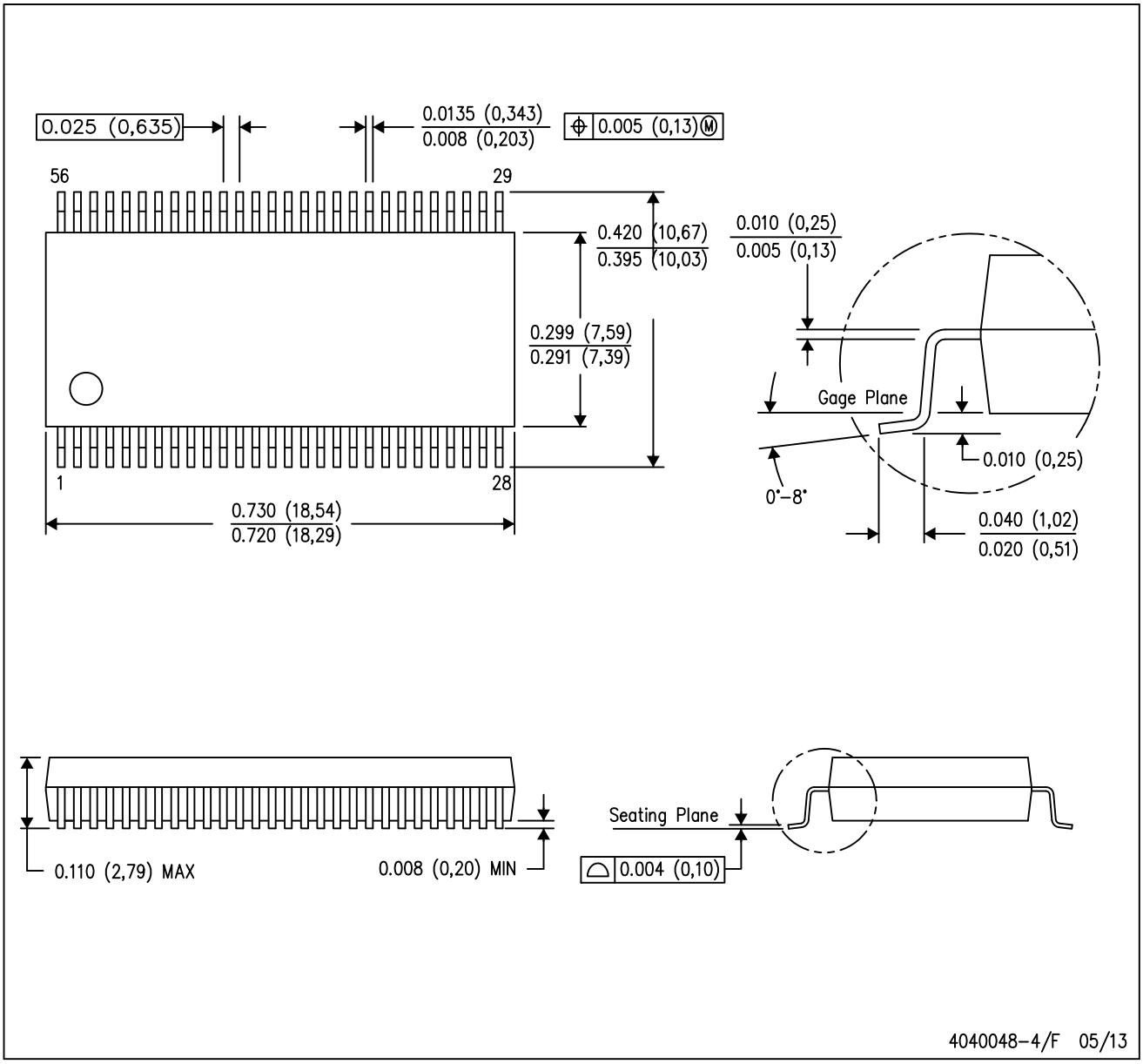
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LVT16543DL	DL	SSOP	56	20	473.7	14.24	5110	7.87
SN74LVT16543DL.B	DL	SSOP	56	20	473.7	14.24	5110	7.87
SN74LVT16543DLG4	DL	SSOP	56	20	473.7	14.24	5110	7.87
SN74LVT16543DLG4.B	DL	SSOP	56	20	473.7	14.24	5110	7.87

DL (R–PDSO–G56) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

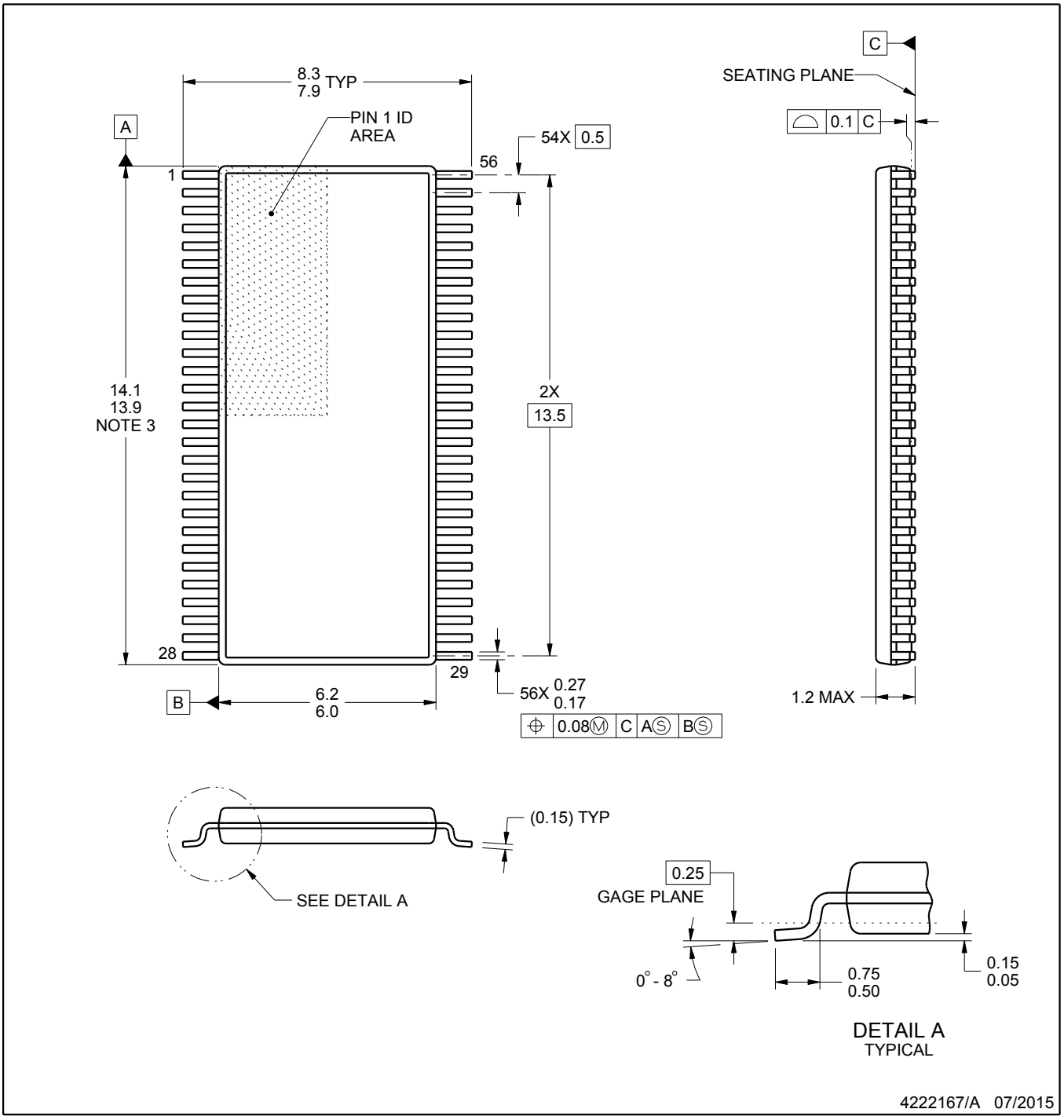
PowerPAD is a trademark of Texas Instruments.

PACKAGE OUTLINE

DGG0056A

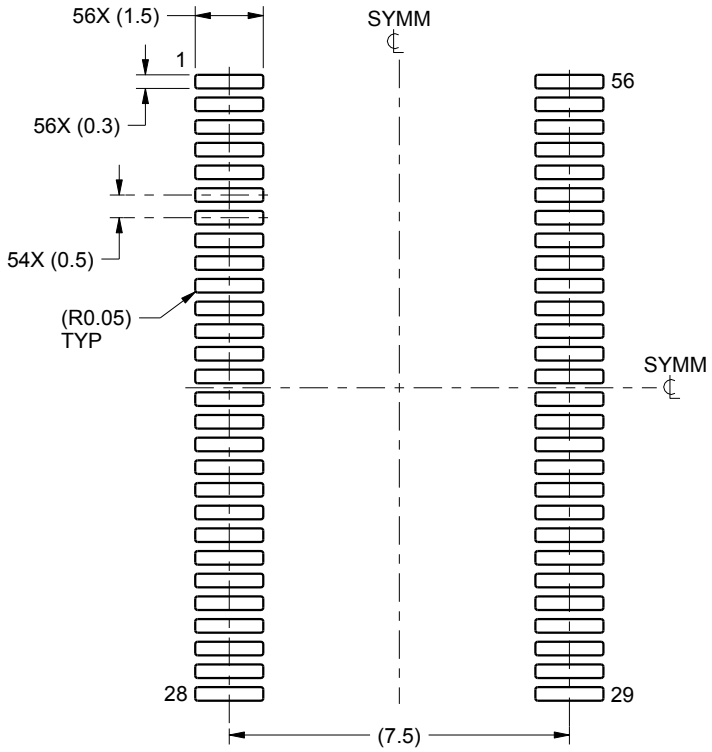
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

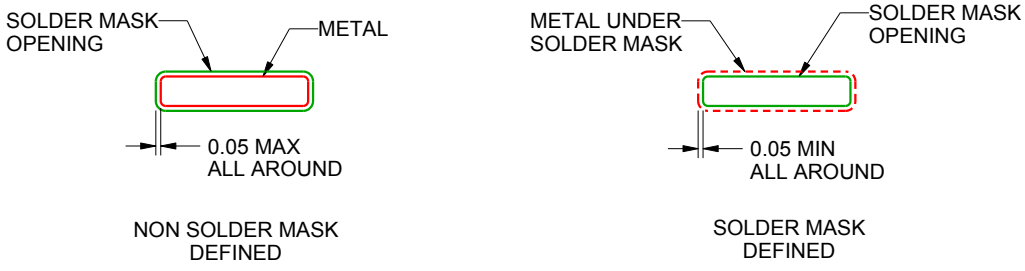


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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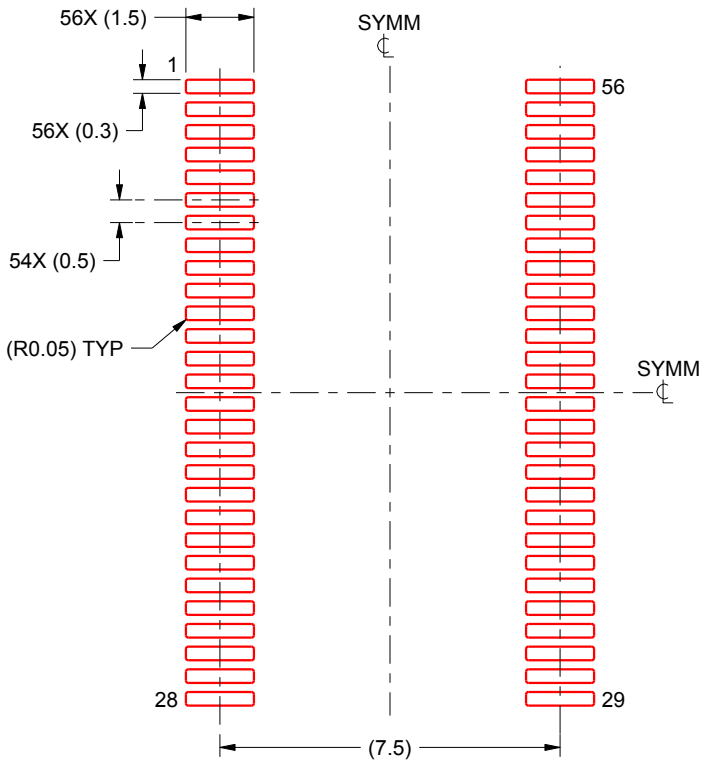
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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