TPS68000EVM-202 Dual Lamp Evaluation Module

This user's guide describes the characteristics, operation, and use of the TPS68000EVM evaluation module (EVM). This EVM is designed to help the user easily evaluate and test the operation and functionality of the TPS68000. The document includes setup instructions for the hardware, a schematic diagram, a bill of materials, and PCB layout drawings for the evaluation module.

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1 Introduction

The Texas Instrument TPS68000EVM-202 evaluation module (EVM) helps designers evaluate the operation and performance of the TPS68000 cold cathode fluorescent lamp (CCFL) controller. The TPS68000EVM-202 is a fully functional DC/AC inverter module used to drive two CCFL lamps from a single controller. This EVM operates from an input supply of 10 V to 20 V and generates up to 600 Vrms at 6 mArms. The EVM drives two CCFL lamps with a 6-mArms constant current each. The EVM's output voltage is determined by the CCFL lamp characteristics. The typical output voltage is 600 Vrms for a 300-mm length CCFL lamp like the JKL Components BF3300-208 lamp.

> **Note:** As with all CCFL inverters, high AC voltages are present on the outputs, and therefore care should be taken to avoid shock hazards and equipment damage.

1.1 Related Documentation From Texas Instruments

TPS68000, Highly Efficient Phase Shift Full Bridge CCFL Controller data sheet (SLVS524)

1.2 Background

The TPS68000EVM-202 uses the TPS68000 configured to drive two transformers and lamps. The advantages of this configuration are improved lamp strike and current regulation. With each lamp powered from its own transformer, strike of one lamp does not load the second transformer and reduce voltage on the un-ignited lamp.

Lamp current is diode-ORed together, and the greater current is used for regulation. Another option is to sum both lamp currents together in a common lamp return resistor for regulation.

Overcurrent (OCP) and overvoltage (Vsen) detection from each circuit are also diode-ORed together for protection.

Although the TPS68000 is capable of operating from an 8-V to 30-V input range, this EVM is only designed to operate from a 10-V to 20-V input range.

Additional lower input voltage configurations are also possible. Output voltage and current are a function of transformer and circuit design.

1.3 Performance Specification

Table 1-1 provides a summary of the TPS68000EVM-202 performance specifications. All specifications are given for an ambient temperature of 25°C.

Table 1. Performance Specification Summary

Specification	Min	Typ	Max	Unit
Input voltage	10	15	20	V
Input current		700		mA
Output current		5.7		mArms
Output voltage		720		Vrms
Efficiency		80%		
Strike voltage		1300		Vrms
Open lamp delay		1.6		S
Operating frequency		56		kHz
Burst dimming frequency		100		Hz
Burst dimming range	0		2	V
Analog dimming range	0		3.3	V

1.4 Modifications

No modifications are provided for this unit.

1.4.1 Analog Dimming Adjustment

R2 adjusts the analog dimming of U1 to increase or decrease brightness. With analog dimming, the lamp current regulation point is changed to vary the lamp brightness. R14 or R15 initially sets the lamp current to 6 mArms. Full counterclockwise setting of R2 sets the lamp current to the maximum brightness level of 6 mArms. Full clockwise setting of R8 adjusts the lamp to minimum brightness. ABR voltage can be monitored at J5. Dimming voltage range is 3.3 V to 0 V. Note that typically when the lamp current is reduced below 3 mArms, performance is degraded; this is a lamp characteristic not an IC characteristic.

An external ABR voltage can be applied to J5 to control the lamp current. If this feature is used, then R2 should be set to midrange ~1.65 V. The range of the external ABR voltage should be 3.3 V to 0 V.

1.4.2 Internal Burst Dimming Adjustment

The TPS68000 internal burst dimming feature (BBR) is adjusted using R1. A voltage of 2 V to 0 V changes the PWM duty cycle of the lamps to change brightness. For example, 2 V at the BBR pin corresponds to 100% duty cycle, whereas 0 V corresponds to a 0% duty cycle. This voltage can be monitored at J3 connector. Turn R1 clockwise to reduce brightness and duty cycle and counterclockwise to increase brightness and duty cycle.

Burst dimming frequency is set by the capacitor at the BF pin. The EVM uses a 0.47-µF capacitor for a frequency of 100 Hz. See the data sheet (SLVS524) for the equation.

A voltage can be applied at J3 to externally control BBR, but R1 should be set for midrange (2.5 V) before applying the external voltage. The range of the external BBR voltage should be 2 V to 0 V.

For proper operation of the external burst dimming (BC) function, set R1 fully counterclockwise which applies +5 V at BBR.

1.4.3 External Burst Dimming Adjustment

The EVM can be configured for external burst dimming by using the BC input at J4. A digital signal can be applied at this input to PWM-dim all the lamps. The BC pin detects the input transition and automatically switches to external burst dimming. A 0-V signal turns the lamps off, and voltage greater than 1.4 V turns the lamps on. A burst dimming frequency of 100 HZ to 200 HZ is recommended.

For proper operation of the external burst dimming (BC) function, R1 should be set fully counterclockwise which applies +5 V at BBR.

2 Setup and Results

This section describes how to properly use the TPS68000EVM-202.

2.1 Input/Output Connector and Header Descriptions

Table 2. I/O for Unit

Signal		Connector
Vin	Power supply positive input	J1
GND	Power supply return input	J2
EN	Enable input, OFF and ON setting; no jumper is ON	JP1
BBR	Internal burst dimming monitor or input; set by R1 active range 2 V to 0 V	J3
BC	Burst dimming input signal	J4
ABR	Analog burst dimming voltage; set by R2 from 3.3 V to 0 V.	J5
FAULT	Fault output bus signal, open-collector signal	J6

Table 3. I/O for Lamp 1 and Lamp 2 Sections

Signal Name	Lamp 1 Section	Lamp 2 Section
High-voltage AC output to lamp	TP16	TP11
High-voltage return from lamp	TP17	TP12
Overcurrent protection test point (OCP), transformer primary current	TP9	TP10
Current sense test point (Csen), lamp return current sense resistor	TP18	TP13
Voltage sense test point (Vsen), output voltage divider sample voltage	TP15	TP14

Table 4. Test Points Unit

Signal		Test Point
Sync	Sync out of U1, digital signal at operating freq set by R7	TP3
GND	For sync test point	TP2
Sum OCP	Overcurrent sum from lamp 1 and lamp 2	TP5
Sum VSEN	Voltage sense sum from lamp 1 and lamp 2	TP4
Sum CSEN	Current sense sum from lamp 1 and lamp 2	TP6
GND	For TP4, TP5, and TP6	TP1
SA	H-bridge output to transformers	TP7
SC	H-bridge output to transformers	TP8

2.2 Setup

> **CAUTION**
>
> High AC voltage is present at output terminals when input voltage is applied. Make all connections with the input supply OFF.

Do not place the EVM or lamp on a conductive surface. Do not run output leads across EVM or input voltage leads.

Minimum connections:

- J1/J2 power supply input
- Lamp 1 connected at TP16 (HV) and TP17 (RTN)
- Lamp 2 connected at TP11(HV) and TP12 (RTN)
- Set R1 and R2 fully counterclockwise.
- JP1 install shorting jumper in OFF position, after applying power remove jumper to turn unit ON.

2.3 Output Voltage and VSEN Test Point

Output voltage can be monitored at the low-voltage VSEN test points TP14 and TP15, without special equipment. VSEN is a divided-down sample of the output voltage used by the TPS68000 for voltage monitoring and regulation. Divide ratio is 1:1000.
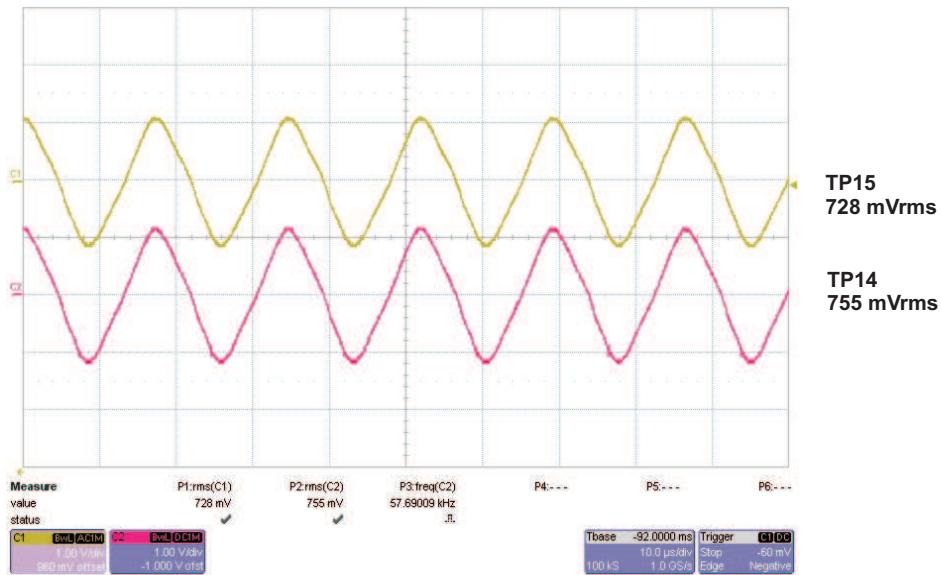
Figure 1. Lamp 1 and Lamp2 VSEN Test Points
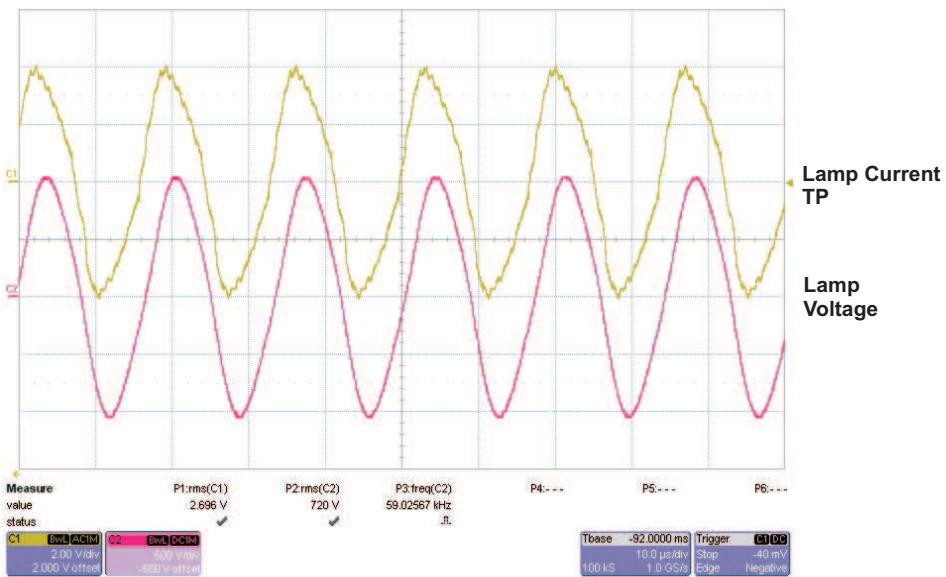
Figure 2. Lamp 1 VSEN Test Point and Lamp 1 Voltage

2.4 Output Current and CSEN Test Point

Output current can be monitored at the CSEN test points TP18 and TP13, without special equipment. CSEN is an input to the TPS68000 for regulating output current. Divide ratio for both lamp 1 and lamp 2 are 0.45 V to 1 mA. During normal operation, the CSEN sum test point TP6 is regulating at 2.4 Vrms. Figure 3 shows lamp current measured using an external current probe versus CSEN test point.
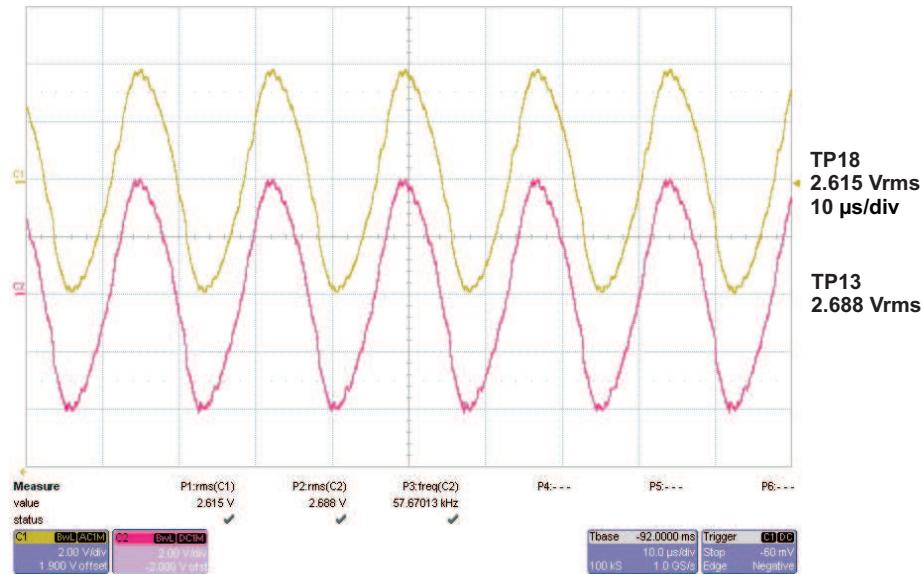
Figure 3. Lamp 1 and Lamp 2 CSEN Test Point
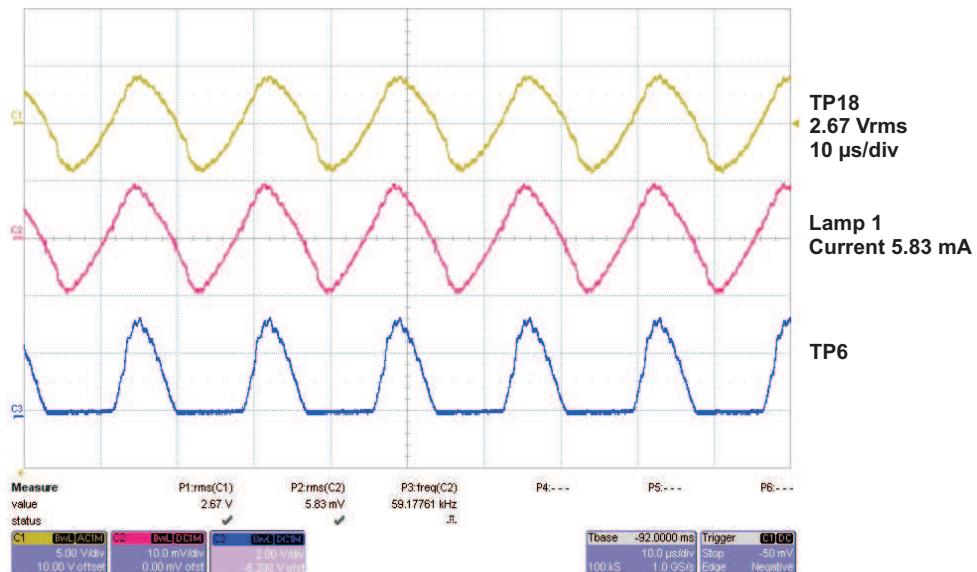
Figure 4. Lamp 1 CSEN Test Point, Lamp 1 Current, and CSEN SUM Test Point

2.5 Power Up

During power up, the lamp strikes, and then goes into a current regulation mode. During lamp strike, the lamp has high resistance because no gas is being ionized. The voltage required to strike the lamp is typically twice the voltage required for normal operation. After the lamp strikes, current flows through the lamp, and the TPS68000 transitions to a current regulation mode.
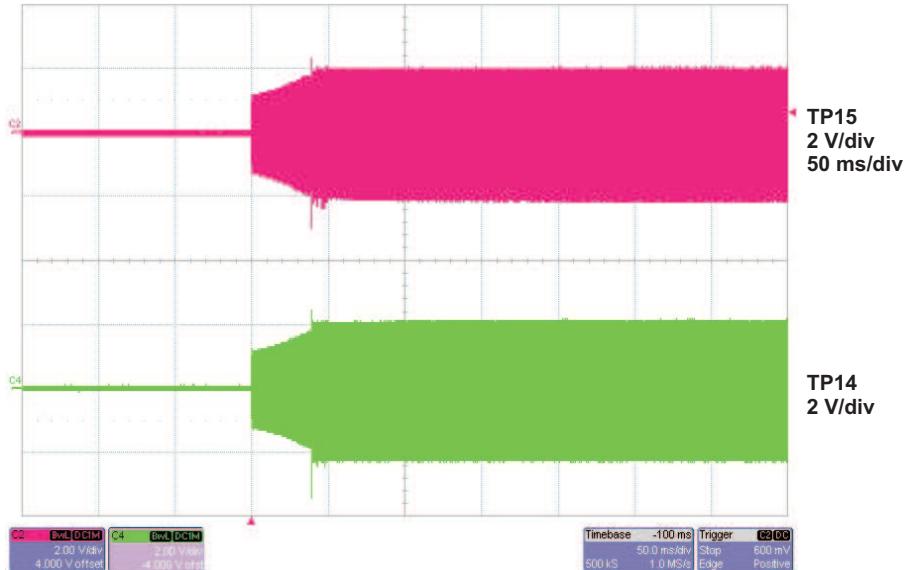
Figure 5. Lamp 1 and Lamp 2 VSEN Test Point Lamp Strike (Turn ON)

2.6 Burst Dimming

R1 controls burst dimming. The adjustment range is 2 V to 0 V. Figure 4 shows the lamp current when R1 sets at 1 V to produce a 50% duty cycle burst dimming waveform. Note the reduced soft start at turn on.
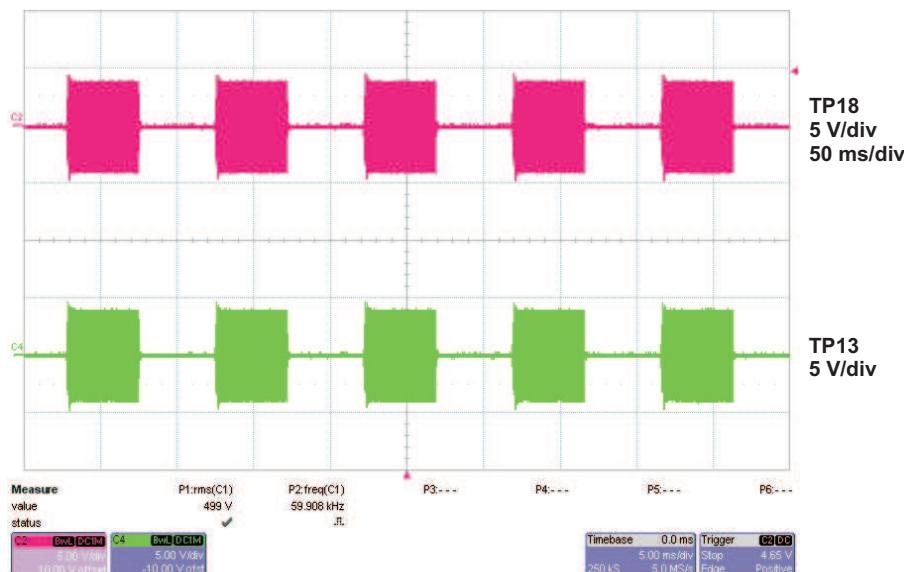
Figure 6. Internal Burst Dimming 50%, BBR Pin at 1 V

2.7 Open-Lamp Shutdown and Voltage Regulation

The VSEN is used to detect an open-lamp condition and protect the inverter from overvoltage. If one of the lamps is disconnected or damaged, the circuit is open and voltage could be very high, damaging the transformer and circuit board. Output voltage is monitored and regulated by VSEN input. See the data sheet (SLVS524) for the set point. For this unit, it is set to 1300 Vrms.

Also, the open-lamp condition could be due to a cold lamp or a hard to strike lamp; for those conditions, the open-lamp voltage is held on for a set time. This time is set by C7 for 1.6 seconds. See the data sheet for calculations.
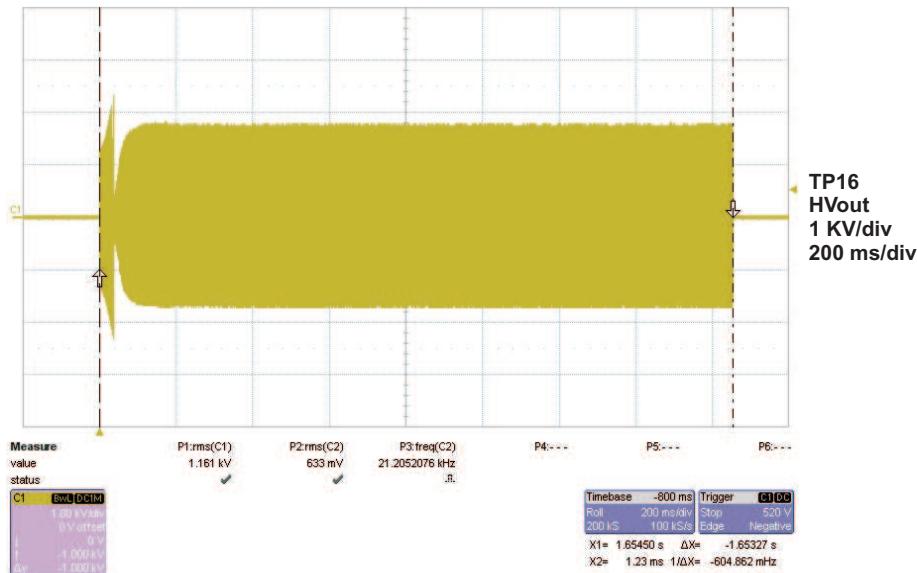
Figure 7. Open-Lamp Shutdown, Time 1.65 Seconds, Lamp 1 Voltage
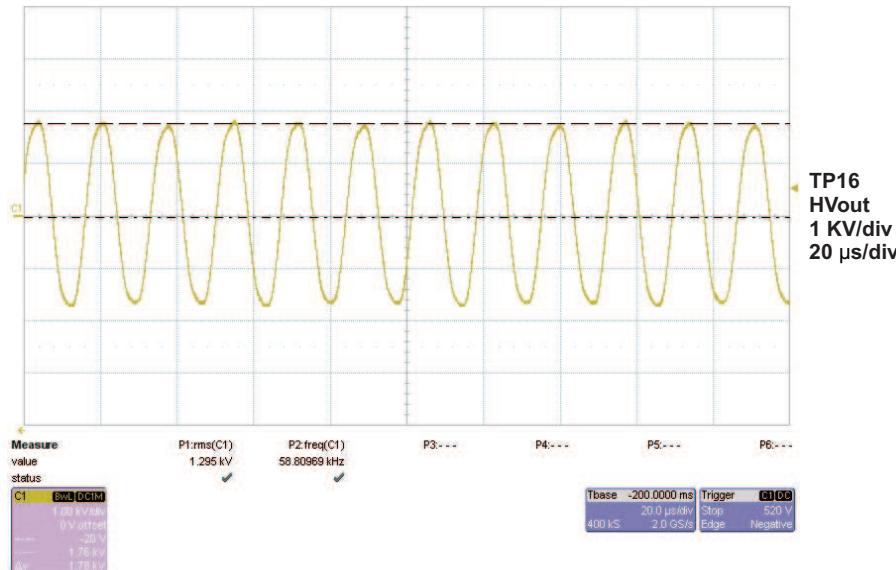
Figure 8. Open-Lamp Voltage Regulation, 1295 Vrms

3 Board Layout

This section provides the TPS68000EVM-202 board layout and illustrations.

3.1 Layout

Figure 9 though Figure 11 show the board layout for the TPS68000EVM-202 printed-circuit board.
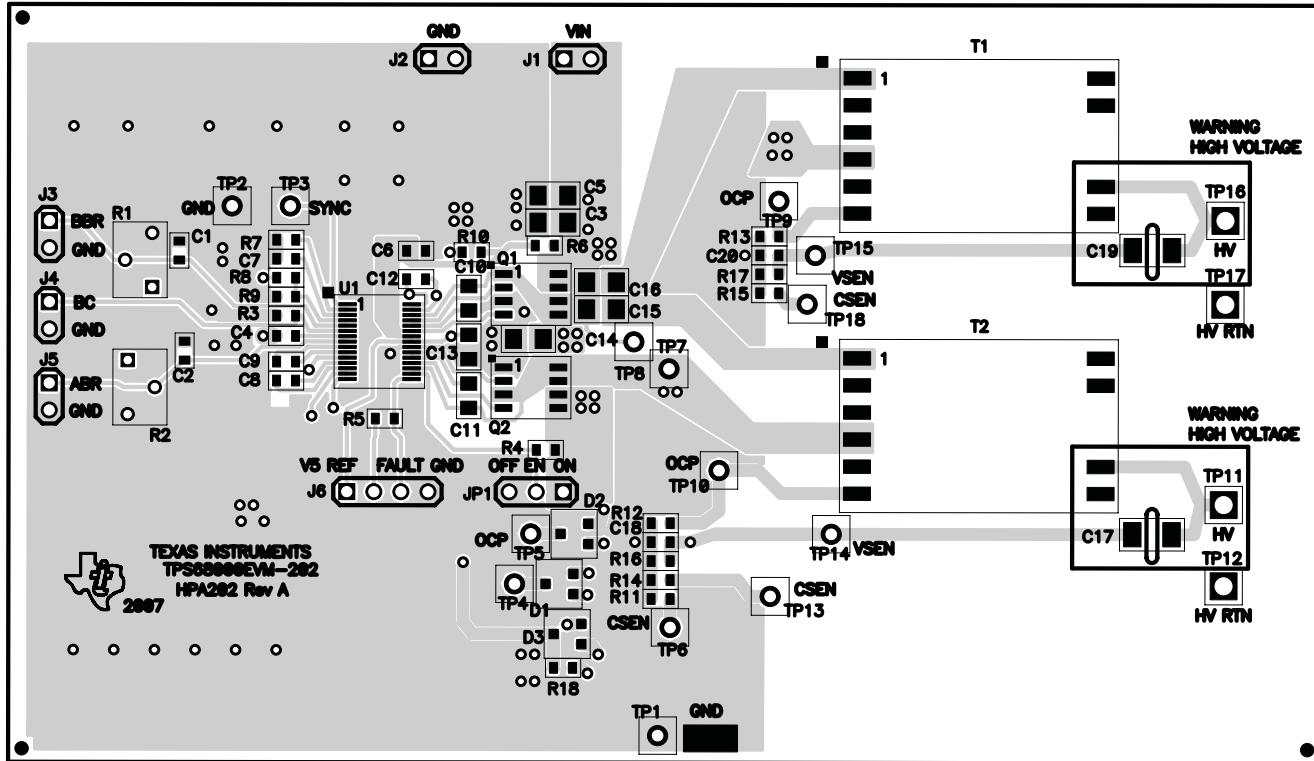
Figure 9. Assembly Layer
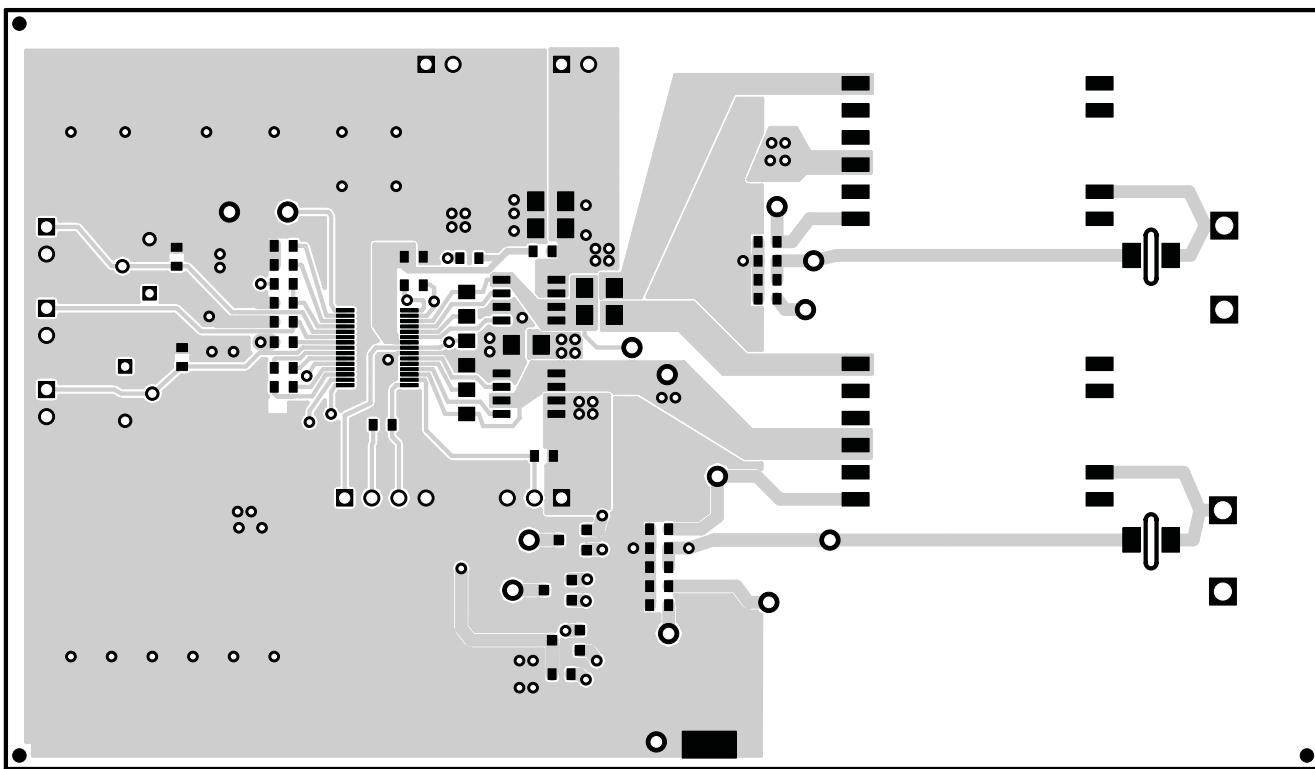
Figure 10. Top Layer Routing
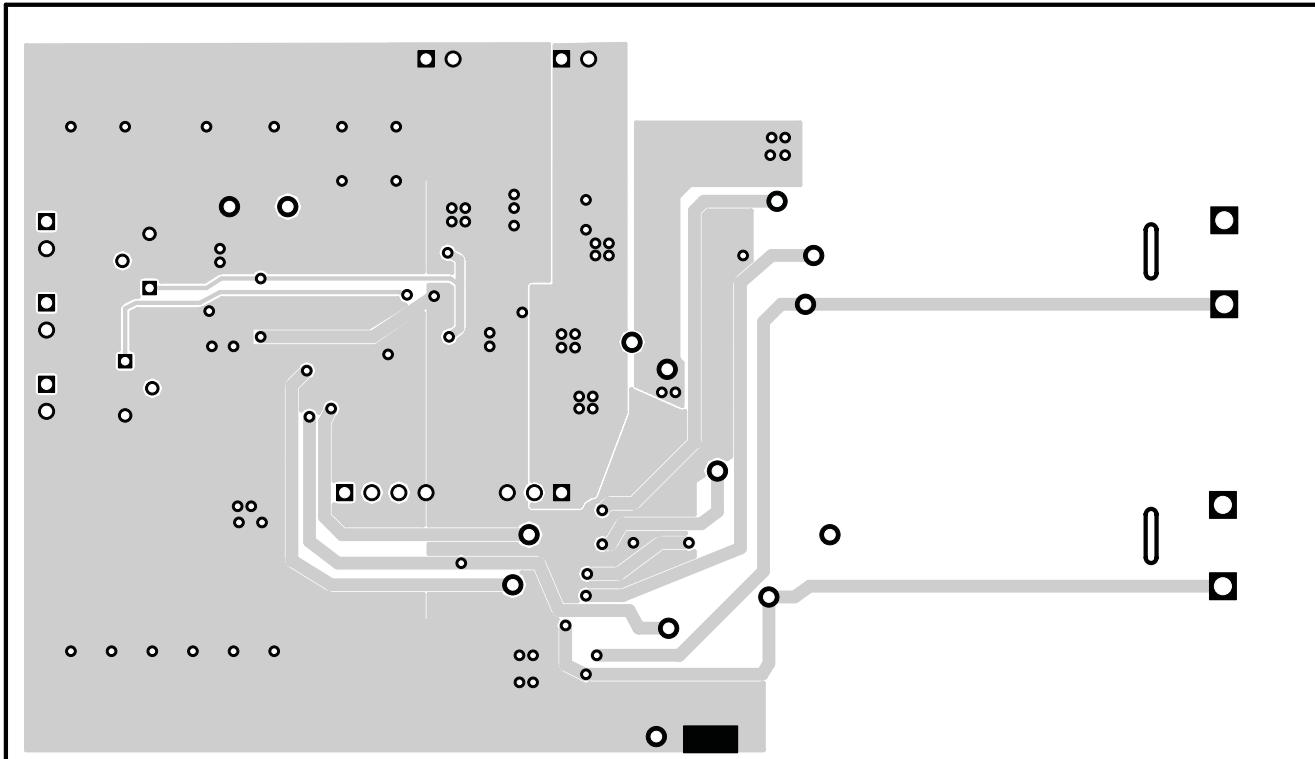
Figure 11. Bottom Layer Routing

4 Schematic and Bill of Materials

This section provides the TPS68000EVM-202 schematic and bill of materials.

4.1 Schematic
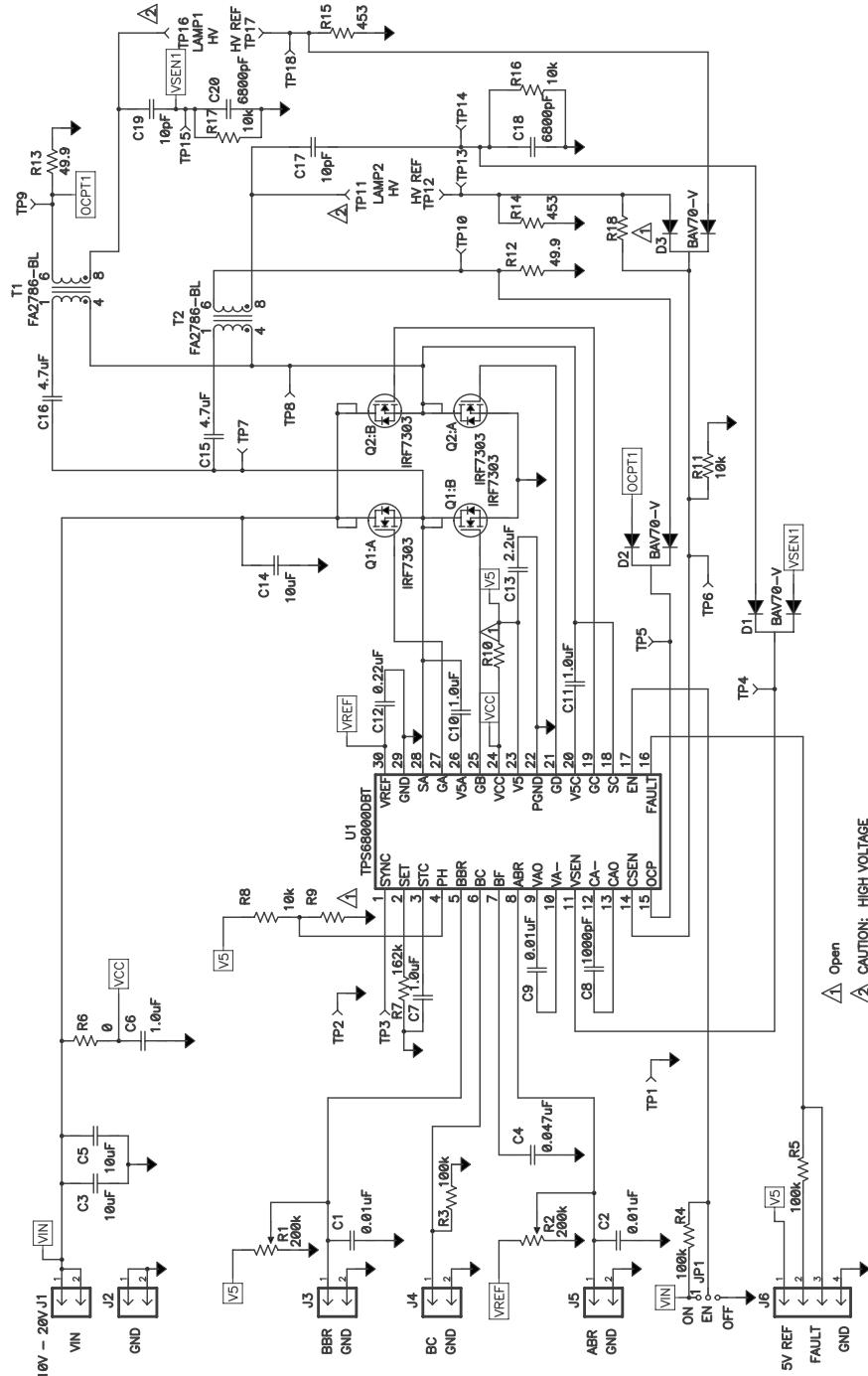
Figure 12. TPS68000EVM-202 Schematic

4.2 Bill of Materials

Table 5. TPS68000EVM-202 Bill of Materials

COUNT	RefDes	Value	Description	Size	Part Number	MFR
3	C1, C2, C9	0.01 µF	Capacitor, Ceramic, 25V, X5R, 10%	0603	C1608X5R1E103KB	TDK
2	C10, C11	1.0 µF	Capacitor, Ceramic, 25V, X7R, 10%	0805	C2012X7R1E105K	TDK
1	C12	0.22 µF	Capacitor, Ceramic, 16V, X5R, 10%	0603	C1608X5R1C224KB	TDK
1	C13	2.2 µF	Capacitor, Ceramic, 25V, X5R, 10%	0805	C2012X5R1E225K	TDK
2	C15, C16	4.7 µF	Capacitor, Ceramic, 25V, X5R, 10%	1206	GRM319R61E475KA12D	Murata
2	C17, C19	10 pF	Capacitor, 3kV, C0G, ±1pF	0.110 × 0.110	C4520C0G3F100F	TDK
2	C18, C20	6800 pF	Capacitor, Ceramic, 25V, C0G, 5%	0603	C1608C0G1E682J	TDK
3	C3, C5, C14	10 µF	Capacitor, Ceramic, 25V, X5R, 10%	1206	C3216X5R1E106K	TDK
1	C4	0.047 µF	Capacitor, Ceramic, 50V, X7R, 10%	0603	C1608X7R1H473KB	TDK
2	C6, C7	1.0 µF	Capacitor, Ceramic, 25V, X5R, 10%	0603	C1608X5R1E105K	TDK
1	C8	1000 pF	Capacitor, Ceramic, 50V, X7R, 10%	0603	C1608X7R1H102K	TDK
3	D1–D3		Diode, Switching, Dual, 70V, 250mA	SOT23	BAV70-V	Zetex
5	J1–J5		Header, 2 pin, 100mil spacing, (36-pin strip)	0.100 × 2	PTC36SAAN	Sullins
1	J6		Header, 4 pin, 100mil spacing, (36-pin strip)	0.100 × 4	PTC36SAAN	Sullins
1	JP1		Header, 3 pin, 100mil spacing, (36-pin strip)	0.100 × 3	PTC36SAAN	Sullins
2	Q1, Q2		MOSFET, Dual Nch, 30 V, 4.9A, 50milliohm	SO8	IRF7303	IR
2	R1, R2	200k	Potentiometer, 1/4 Cermet	12-Turn	3266W-1-204	Bourns
2	R12, R13	49.9	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R14, R15	453	Resistor, Chip, 1/16W, 1%	0603	Std	Std
3	R3–R5	100k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R6	0	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R7	162k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
4	R8, R11, R16, R17	10k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	R9, R10, R18	Open	Resistor, Chip, 1/16W, 1%	0603		
2	T1, T2		Transformer,	0.965 × 0.610	FA2786-BL	Coilcraft
2	TP1, TP2		Test Point, Black, Thru Hole Color Keyed	0.100 × 0.100	5001	Keystone
2	TP11, TP16		Test Point, Red, Thru Hole Compact Style	0.125 × 0.125	5005	Keystone
2	TP12, TP17		Test Point, Black, Thru Hole Compact Style	0.125 × 0.125	5006	Keystone
12	TP3–TP10, TP13– TP15, TP18		Test Point, Red, Thru Hole Color Keyed	0.100 × 0.100	5000	Keystone
1	U1		IC, High Efficient Phase Shift Full Bridge CCFL Controller	TSSOP-30	TPS68000DBT	TI
1	—		PCB, 4.85 In x 2.8 In x 0.062 In		HPA202	Any
1	—		Shunt, 100mil, Black	0.100	929950-00	3M

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 10 V to 20 V and the output voltage range of 300 VAC to 1300 VAC.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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