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NTE1641
Integrated Circuit
1024 Stage BBD for Audio Signal Delays

Description:

The NTE1641 is a 1024–stage long delay low noise BBD that provides a signal delay of up to 51.2msec. This device is suitable for use as the reverberation effect of an electronic musical instrument, or in stereo equipment, due to its long delay times.

Features:

- Variable delay time of audio signal: 5.12ms to 51.2ms.
- Clock component cancellation capability.
- No insertion loss: L_i = 0dB typ.
- Wide dynamic range: S/N ≅ 80dB typ.
- Wide frequency response: $f_i \le 12kH_Z$.
- Low distortion: THD = 0.5% typ. ($V_i = 0.78V_{rms}$)
- Clock frequency range: 10 to $100kH_Z$.
- P channel silicon gate process.
- 8–Lead DIP plastic package.

Applications:

- Reverberation effect echo for P.A. and stereo equipment.
- Chorus effect in electronic musical instruments.
- Variable or fixed delay of analog signals
- Telephone time compression and delay line for voice communication systems, etc.

Absolute Maximum Ratings: (T_A = +25°C unless otherwise specified)

Pin Voltage, V_{DD}, V_{GG}, V_{CP}, V_I . . . . . –18V to +0.3V

Output Voltage, V_O . . . . . –18V to +0.3V

Operating Ambient Temperature Range, T_{opr} . . . . . –20° to +60°C

Storage Temperature Range, T_{stg} . . . . . –55° to +125°C

Operating Conditions: (T_A = +25°C unless otherwise specified)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Drain Supply Voltage	V_{DD}		–14	–15	–16	V
Gate Supply Voltage	V_{GG}		–	V_{DD}+1	–	V
Clock Voltage “H” Level	V_{CPH}		0	–	–1	V
Clock Voltage “L” Level	V_{CPL}		–	V_{DD}	–	V
Clock Frequency	f_{CP}		10	–	100	kH_Z
Clock Pulse Width	$t_{W(CP)}$[2]				0.5T[1]	–
Clock Rise Time	$t_{r(CP)}$[2]		–	–	500	μs
Clock Fall Time	$t_{f(CP)}$[2]		–	–	500	ns
Clock Input Capacitance	C_{CP}		–	–	700	V
Clock Cross Point	V_X[2]		0	–	–3	V
Input DC Bias Voltage	V_{Bias}		–5	–	–10	V

Electrical Characteristics: (T_A = +25°C, V_{DD} = V_{CPL} = –15V, V_{CPH} = 0V, V_{GG} = –14V, R_L = 100kΩ)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Signal Delay Time	t_D		5.12	–	51.2	ms
Input Singal Frequency	f_i	f_{CP} = 40kHz, V_i = 1.5Vrms, 3dB down (0dB at f_i = 1kH_Z)	12	–	–	kH_Z
Input Voltage Amplitude	υi	f_{CP} = 40kH_Z, fi = 1kH_Z, THD = 2.5%	1.5	–	–	V_{rms}
Insertion Loss	Li	f_{CP} = 40kH_Z, fi = 1kH_Z, V_i = 1.5V_{rms}	–4	0	4	dB
Total Harmonic Distortion	THD	f_{CP} = 40kH_Z, fi = 1kH_Z, V_i = 0.78V_{rms}	–	0.5	2.5	%
Output Noise Voltage	V_{no}	f_{CP} = 100kH_Z, Weighted by “A” curve	–	–	0.3	mV_{rms}
Signal to noise ratio	S/N		–	80	–	dB

Note 1. T = 1/f_{cp} (Clock Period)
Note 2. Clock pulse waveforms

Pin Connection Diagram